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Graphene Bridge Heterostructure Devices for Negative Differential Transconductance Circuit Applications

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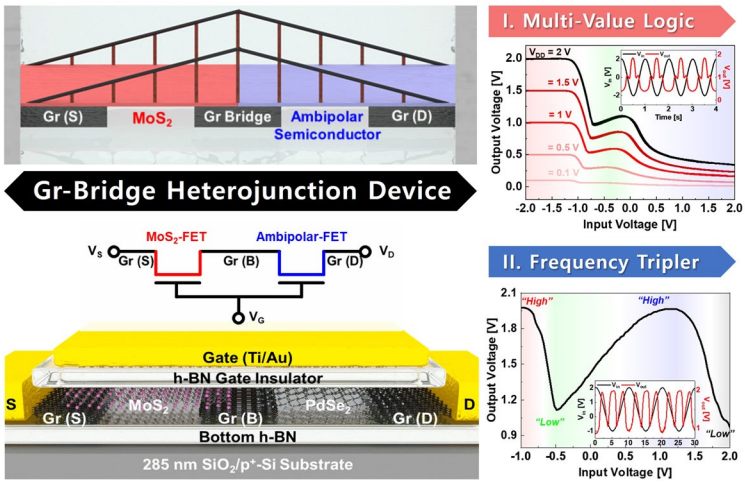
HIGHLIGHTS

- Graphene (Gr)-bridge heterostructure, consisting of a laterally series-connected (cascade) ambipolar/Gr/*n*-type 2D van der Waals channel materials for ambipolar semiconductor-based high-end application devices was developed.
- Non-classical transfer characteristics (humped curve) in FET operation and negative differential transconductances were observed.
- Gr-bridge heterostructure device with $PdSe_2$ (narrow bandgap) allows multi-value logic operation while WSe_2 (wide bandgap) enables frequency tripler circuit operation.

ABSTRACT Two-dimensional van der Waals (2D vdW) material-based heterostructure devices have been widely studied for high-end electronic applications owing to their heterojunction properties. In this study, we demonstrate graphene (Gr)-bridge heterostructure devices consisting of laterally series-connected ambipolar semiconductor/Gr-bridge/*n*-type molybdenum disulfide as a channel material for field-effect transistors (FET). Unlike conventional FET operation, our Gr-bridge devices exhibit non-classical transfer characteristics (humped transfer curve), thus possessing a negative differential transconductance. These phenomena are interpreted as the operating behavior in two series-connected FETs, and they result from the gate-tunable contact capacity of the Gr-bridge layer. Multi-value logic inverters and frequency tripler circuits are successfully demonstrated using ambipolar semiconductors with narrow- and



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wide-bandgap materials as more advanced circuit applications based on non-classical transfer characteristics. Thus, we believe that our innovative and straightforward device structure engineering will be a promising technique for future multi-functional circuit applications of 2D nanoelectronics.

KEYWORDS Graphene bridge; Heterostructure device; Non-classical transfer characteristics; Multi-value logic inverter; Frequency tripler

1 Introduction

Two-dimensional van der Waals (2D vdW) nanomaterials have provided intriguing opportunities for various applications in nanoelectronics. For example, graphene (Gr) is a versatile material owing to its excellent carrier mobility and compatibility with various applications; however, the absence of a bandgap limits its use as a semiconductor channel beyond silicon-based electronics [1, 2]. Thus, it can be considered as a conductor material in future electronic devices, and several research groups have used exfoliated Gr as source (S), drain (D), and gate (G) electrodes to achieve all-2D material-based field-effect transistor (FET) applications [3–6]. The Gr S/D electrodes can effectively overcome the Schottky barrier, generally observed between 2D vdW semiconductors and metal contacts [7–10], owing to its gate-dependent Fermi level (E_F) modulation [4, 11]. Because of this advantage, Gr electrodes are widely used in 2D vdW materials-based advanced electronic devices, thereby providing an innovative device structure and excellent device performance.

The 2D vdW semiconductors, such as transition metal dichalcogenides (TMDs) and 2D Xenes, have emerged because of their unique electrical properties since the discovery of Gr. Among these, tungsten diselenide (WSe_2) and molybdenum ditelluride ($MoTe_2$) possess strong gate-dependent characteristics; essentially, they exhibit ambipolar properties in FET applications [12, 13]. The tunable bandgap of WSe_2 and $MoTe_2$ is investigated as 1.22 (bulk) to 1.64 eV (monolayer) [14, 15] and 0.9 (bulk) to 1.1 eV (monolayer) [16, 17], respectively. In contrast, black phosphorus (BP) and palladium diselenide ($PdSe_2$), which have narrower bandgaps, exhibit stronger ambipolar properties than WSe_2 and $MoTe_2$ active channels; therefore, they allow the realization of high-performance device applications. The tunable bandgap of BP and $PdSe_2$ is reported as 0.3 (bulk) to 1.0 eV (monolayer) [18–20] and near-zero (bulk) to 1.3 eV (monolayer) [21–25], respectively.

These 2D vdW ambipolar semiconductors are expected to open new horizons for future nanoelectronics by developing new functionalized device applications, such as frequency doublers [26–30], reconfigurable homojunction diodes [31–34], and security circuits [35]. In advanced studies on 2D vdW semiconductors, heterostructure devices constructed using various 2D vdW materials as lego-like building blocks have been explored by numerous research groups to fabricate creative device architectures and investigate their unique junction properties [36–39]. A representative assembled device is a vertically stacked heterojunction diode consisting of two 2D vdW semiconductors for photodiodes [40–43], light-emitting diodes [44, 45], Esaki diodes [46–48], and extraordinary applications [49, 50].

In this study, a laterally series-connected ambipolar semiconductor/Gr/*n*-type molybdenum disulfide (MoS_2) cascade channel device, called a Gr-bridge heterostructure, was studied beyond heterostructure junction device applications. Each active channel part exhibits distinct transport characteristics, such as ambipolar ($PdSe_2$ or WSe_2), mostly metallic (Gr-bridge), and unipolar (MoS_2) properties. However, the series-connected cascade channel combines the transport characteristics of each part, thereby obeying the largest resistance among the channel materials, i.e., the total resistance of the Gr-bridged cascade channel. The Gr-bridge reduces the potential barrier height between the ambipolar semiconductor and *n*-type MoS_2 junction region owing to its metallic and gapless energy band properties. Using this approach, the Gr-bridge allows the realization of unique switching devices and advanced application methods. We successfully demonstrated a multi-value logic inverter circuit and a frequency tripler for advanced electronic applications. Thus, we believe that the Gr-bridge heterojunction structure will open the gate for future electronics by designing device architectures and blending electrical properties toward high-end applications.

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2 Experimental Section

2.1 Device Fabrication

The 285 nm SiO_2/p^+-Si substrate was ultrasonically cleaned in acetone, methyl alcohol, and isopropyl alcohol for 15 min each. To construct the Gr-bridge structure, polydimethylsiloxane (PDMS) stamps were used to exfoliate and transfer 2D vdW nanomaterials onto the substrate through the direct imprinting method. Next, a lift-off process was employed to form the top-gate electrode and the extended S/B/D pad electrodes. E-beam lithography and evaporation were, respectively, used for patterning and depositing metal electrodes at the 3D Convergence Center of Inha University.

2.2 Electrical Characterization

All transfer, output, and VTC characteristics were measured using a semiconductor parameter analyzer (4156B, Agilent) in a dark probe station at room temperature (300 K). To demonstrate the dynamic performance of the WGM-FET, sinusoidal and ramp waveform signals were generated from a function generator (AFG31022, Tektronix).

3 Results and Discussion

3.1 2D Ambipolar Semiconductor and Gr-Bridge Heterostructure Device

Figure 1a shows the transfer characteristics of $PdSe_2$ (narrow bandgap, ~ 0.01 eV) and WSe_2 (wide bandgap, ~ 1.3 eV) channel-based conventional FET devices [15, 24]. The hexagonal boron nitride (h-BN) sandwich structure and Gr S/D electrodes were adopted to investigate their fundamental ambipolar transfer characteristics (I_D–V_G) (see Fig. S1 for the cross-sectional device schematics and optical microscopy (OM) images of the two ambipolar-FET devices). The WSe_2-FET exhibits both lower drain ON ($I_{D,p}$ and $I_{D,n}$) and OFF I_D ($I_{D,off}$) current levels; however, the ON/OFF I_D ratio (I_{ON}/I_{OFF}) is higher than that of the $PdSe_2$-FET. The narrow-bandgap materials typically have good electron and hole carrier mobilities; therefore, they bring a higher ON I_D value in FET devices but poor OFF I_D in general. These distinct transfer characteristics are due to their energy bandgap properties, as shown in Fig. 1b.

In 2D vdW ambipolar semiconductors, the gate voltage (V_G) can electrostatically control the carrier concentration in the active channel of FET devices, namely the electrostatic doping effect [51]. A positive V_G over the threshold voltage of the *n*-type region ($V_{th,n}$) causes E_F to reach the conduction-band edge (E_c), whereas a negative V_G near the V_{th} of the *p*-type region ($V_{th,p}$) enables E_F to reach the valence-band edge (E_v) of ambipolar semiconductor channel materials [24, 52, 53]. Consequently, a wider bandgap will result in a larger valley-like transfer characteristic curve because it needs a stronger V_G (gate field) to modulate the E_F from the intrinsic Fermi level (E_i) to E_c for the *n*-type transition (or the E_F from E_i to E_v for *p*-type transition) with a higher I_{ON}/I_{OFF} ratio. E_G values of the ambipolar channel materials can be easily estimated by using the V_{th} difference ($\Delta V_{th} = V_{th,n}\text{-}V_{th,p}$) and the average subthreshold slopes [$SS_{avg} = (SS_n + SS_p)/2$] of the *n*-type and *p*-type regions by Eq. (1), where q is the electron charge and SS_{60} is the ideal SS value of 60 mV dec^{-1} [24, 35, 52, 53].

$$E_g = \frac{q\Delta V_{th}}{SS_{avg}/SS_{60}} \quad (1)$$

Figure 1c shows the schematic of a typical top-gate transistor device and the expected valley-like transfer characteristic model of ambipolar FETs. The narrow bandgap of the active channel implies that even a small change in V_G leads to a large number of carriers in the active channel with $V_{th,n}$ and $V_{th,p}$ near the transition point (center of the valley-like transfer curve), thereby resulting in a high I_{ON}, high I_{OFF}, and low I_{ON}/I_{OFF} ratio. Although a narrow-bandgap ambipolar semiconductor typically exhibits high-performance FET behavior, the inevitably high I_{OFF} renders it difficult to use for digital logic circuit applications with better switching characteristics, as compared to wide-bandgap ambipolar semiconductors [35]. Based on the ambipolar properties of $PdSe_2$ (narrow bandgap) and WSe_2 (wide bandgap) active channel materials, Gr-bridge heterostructure devices have been studied to achieve advanced electronic applications, such as multi-value logic inverters and frequency tripler circuits.

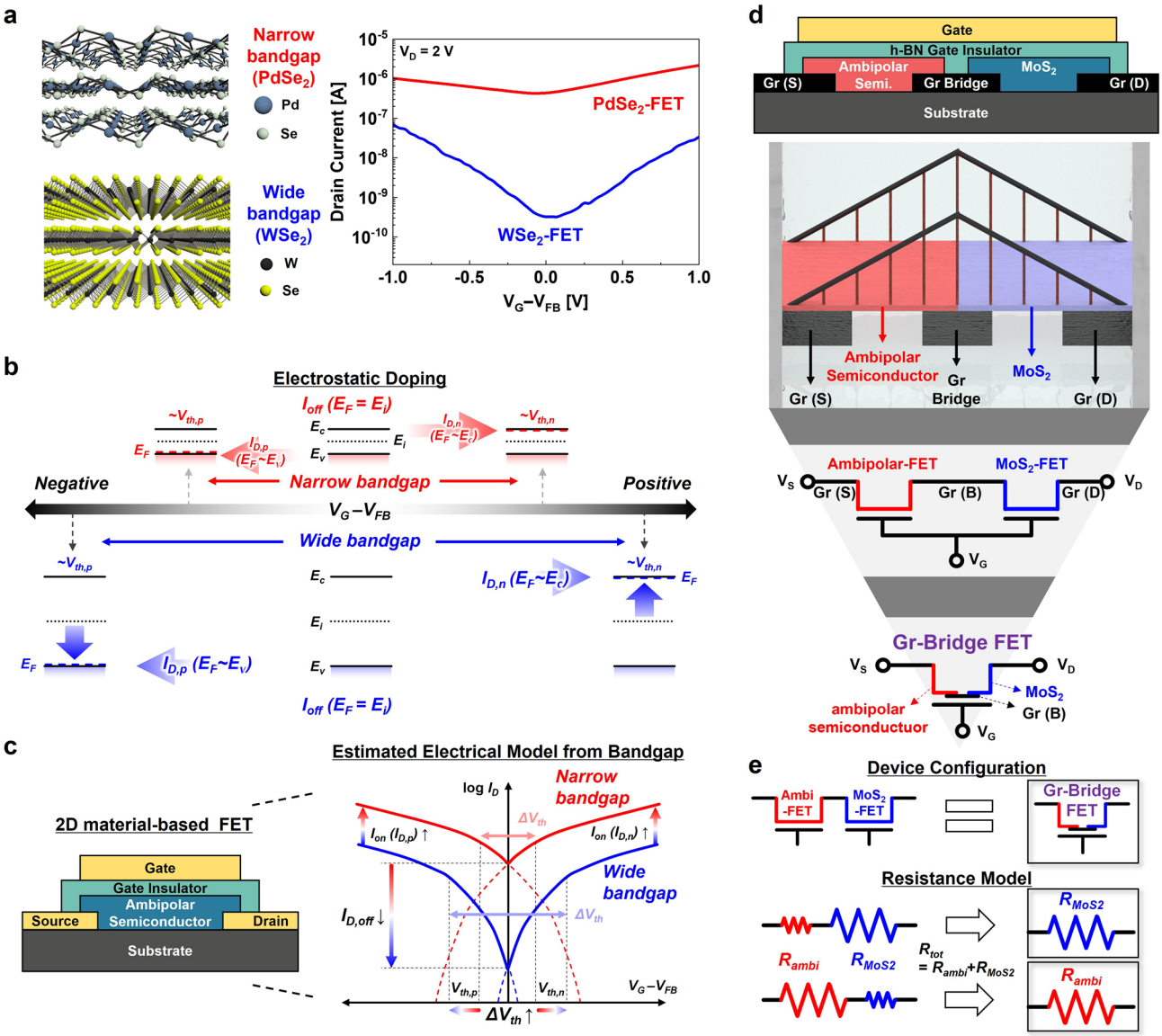

Fig. 1 **a** Atomic crystal structures and I_D–V_G transfer characteristic curves of the ambipolar $PdSe_2$- and WSe_2-FETs. **b** Schematic of the relationship between E_g, V_{th}, and I_D in ambipolar semiconductors. **c** Valley-like estimated electrical transfer model of 2D ambipolar semiconductor-based FETs according to the different energy bandgap properties (narrow and wide bandgap). **d** Conceptual device schematics and suggested electronic component symbol of the Gr-bridge heterostructure device (Gr-bridge FET). **e** Device configuration and resistance-in-series models of Gr-bridge FET

Such devices were formed as a platform of sequentially connected Gr-S, ambipolar semiconductors, Gr-bridge layers, MoS_2, and Gr-D, as shown in Fig. 1d. The Gr bridge layer allows for the inherent characteristics of each 2D vdW semiconductor because it can provide tunable contact properties to both 2D vdW active channels according to its gate-dependent Fermi level modulation [4, 11]. Essentially, the Gr-bridge FET can be regarded as a series connection of the ambipolar-FET and MoS_2-FET, with the same electrical characteristics. Figure 1e shows the simple resistance-in-series model of Gr-bridge FET. The total resistance (R_{tot}) depends on the sum of the resistance in each FET part owing to the series connection properties; therefore, R_{tot} will follow the higher resistance of the two active channels during the device operation. Based on these operating properties, the connected ambipolar and MoS_2 active channel devices in

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series will exhibit synthetic transfer characteristic curves as a breakthrough for high-end device applications.

3.2 $PdSe_2$-Gr-MoS_2 Heterostructure FET

The first Gr-bridge-based high-end device consists of ambipolar $PdSe_2$ (narrow bandgap) and *n*-type MoS_2 active channel materials for multi-value logic applications, as shown in Fig. 2a. Figure 2b, c shows the OM images before and after metal patterning for the extended S/D and common gate (G) electrodes. For sample preparation, the bottom h-BN, Gr S/D, MoS_2-Gr-$PdSe_2$ heterostructure, and h-BN gate insulator were sequentially exfoliated and transferred onto a 285 nm-thick silicon dioxide (SiO_2)/p^+-silicon (Si) substrate. Subsequently, Ti/Au (5 /50 nm) electrodes were patterned and deposited using a combination of e-beam lithography and e-beam evaporation systems. The detailed step-by-step fabrication flow and thickness information for each 2D vdW material are depicted in Fig. S2 and S3, respectively.

Figure 2d shows the I_D–V_G transfer curves of the MoS_2-FET (blue dashed line), $PdSe_2$-FET (red dashed line), and $PdSe_2$-Gr-MoS_2 heterostructure devices (solid black line) at a drain voltage (V_D) of 1 V. We named the Gr-bridge device ($PdSe_2$-Gr-MoS_2 FET) "PGM-FET." Because the h-BN sandwich structure was adopted to

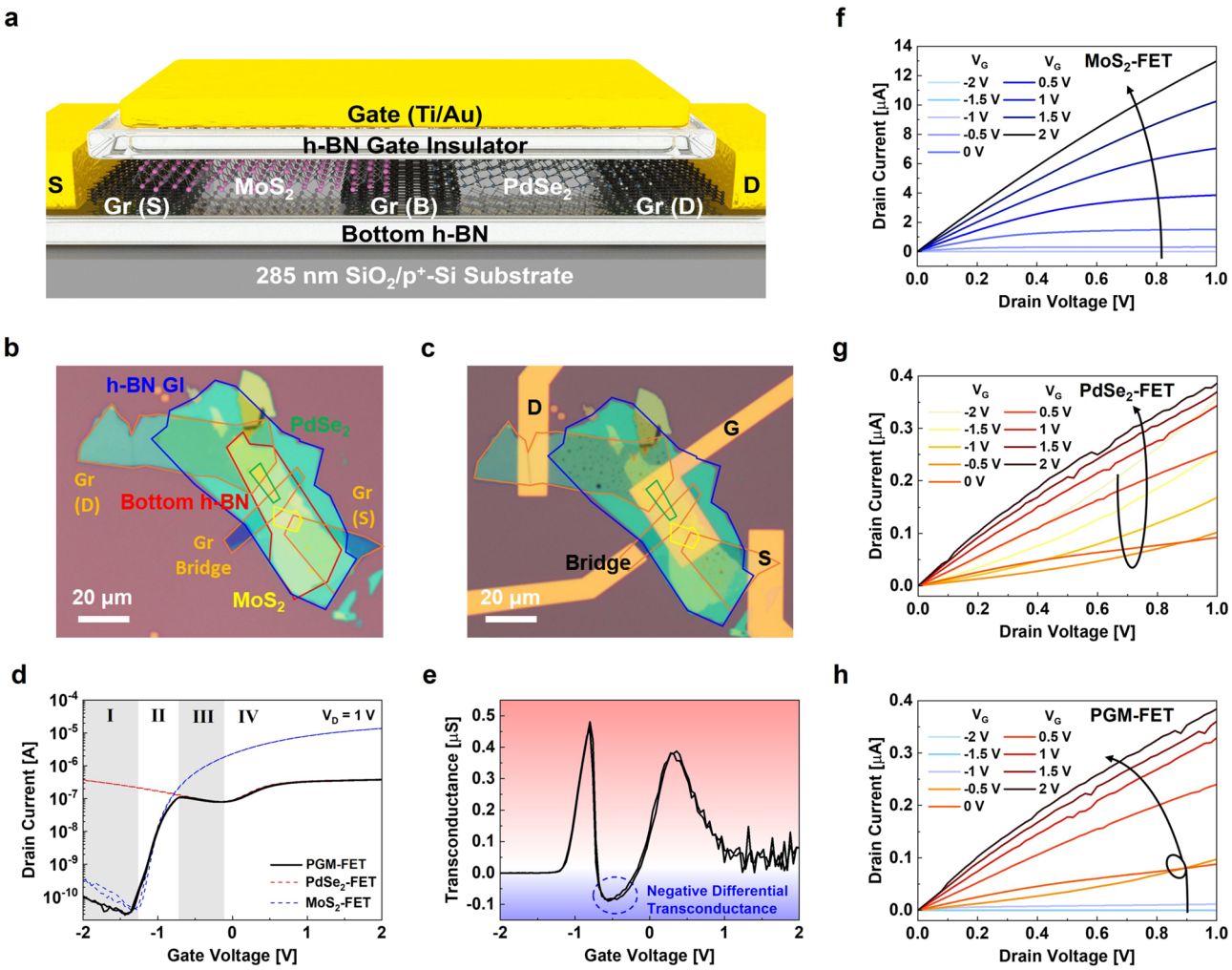

Fig. 2 **a** Cross-sectional 3D device schematic of the $PdSe_2$-Gr-MoS_2 heterostructure FET (PGM-FET) for multi-value logic applications. OM images of the PGM-FET **b** before and **c** after the extended metal electrode fabrication. **d** I_D–V_G transfer characteristic curves of the MoS_2-FET (blue dashed line), $PdSe_2$-FET (red dashed line), and PGM-FET (black solid line) at V_D of 1 V. **e** Estimated transconductance of the PGM-FET obtained from I_D–V_D output characteristic curves of **f** MoS_2-FET, **g** $PdSe_2$-FET, and **h** PGM-FET. (Color figure online)

provide high-quality interfaces, hysteresis-less ideal transfer properties exist in all FET operations [54–57]. The MoS_2-FET exhibits strong *n*-type transfer characteristics, and the $PdSe_2$-FET shows ambipolar transfer characteristics using the Gr bridge layer as a source. Because the graphene interlayer has a gate-tunable contact capacity, it can act as a "bridge," thereby reducing the Schottky junction properties between the ambipolar and *n*-type active channels. The detailed Raman spectrum analysis to confirm the clean and non-interactive interface properties of Gr-bridge and TMDC channels are shown in Fig. S4. Owing to the effect of the Gr bridge interconnection, the PGM-FET exhibits a tilde (~) symbol-like humped transfer characteristic curve: it traces the lower I_D of either the $PdSe_2$ or MoS_2 FETs according to the swept V_G (see the solid black line in Fig. 2d). The I_D of the PGM-FET follows the I_{OFF} (region I) and subthreshold I_D (region II) of the MoS_2-FET, while regions III and IV, respectively, denote the case in the transfer $I_{D,p}$ and $I_{D,n}$ of $PdSe_2$.

To analyze the detailed transport properties of the PGM-FET, the transconductance ($g_m = dI_D/dV_G$) was calculated, and a negative g_m was observed in region III (humped curve), as shown in Fig. 2e. Figure 2f–h shows the output characteristic (I_D–V_D) curves of the MoS_2-FET, $PdSe_2$-FET, and PGM-FET obtained from V_G ranging from − 2 to 2 V in steps of 0.5 V. The Gr bridge provides tunable ohmic contact properties; therefore, the output curves of the MoS_2 and $PdSe_2$ active channels exhibit typical *n*-type and ambipolar transport properties, respectively. Moreover, the PGM-FET exhibits the composite output characteristics of the MoS_2-FET (V_G range of − 2 to − 1 V) and $PdSe_2$-FET (V_G range of − 0.5 to 2 V).

3.3 PGM-FET-Based Multi-value Logic Circuit Applications

Based on the non-classical humped I_D–V_G transfer properties, we extended our PGM-FET study to multi-value logic circuit applications as a first-approach method. An external resistor of 10 MΩ was chosen for the resistive-load inverter circuit near the humped I_D curve, as shown in Fig. 3a. Figure 3b shows the voltage transfer characteristics (VTC) of the PGM-FET-based resistive-load inverter circuit under different supply voltage (V_{DD}) conditions. The inset shows three distinct levels of ternary inverted output voltage (V_{out}) responses. Input voltages (V_{in}) of − 2, 0, and 2 V generate V_{out} of V_{DD}, $V_{DD}/2$, and approximately 0 V, respectively. Figure 3c shows the absolute voltage gain ($|dV_{out}/dV_{in}|$) of the ternary inverter logic circuit under different V_{DD} conditions. The voltage gain is approximately 4 (first voltage drop) and approximately 1.6 (second voltage drop) at a V_{DD} of 2 V. The inset shows the dynamic V_{out} responses obtained from a sinusoidal waveform of V_{in}, which can identify the dynamic ternary levels of the demonstrated ternary logic circuit. The peak-to-peak voltage ($V_{p\text{-}p}$) and periodic time (T) were 4 V and 1 s, respectively.

We developed inverted ternary logic for the Gr-bridge structure, which simply employs a narrow-bandgap ambipolar semiconductor ($PdSe_2$) and an *n*-type semiconductor

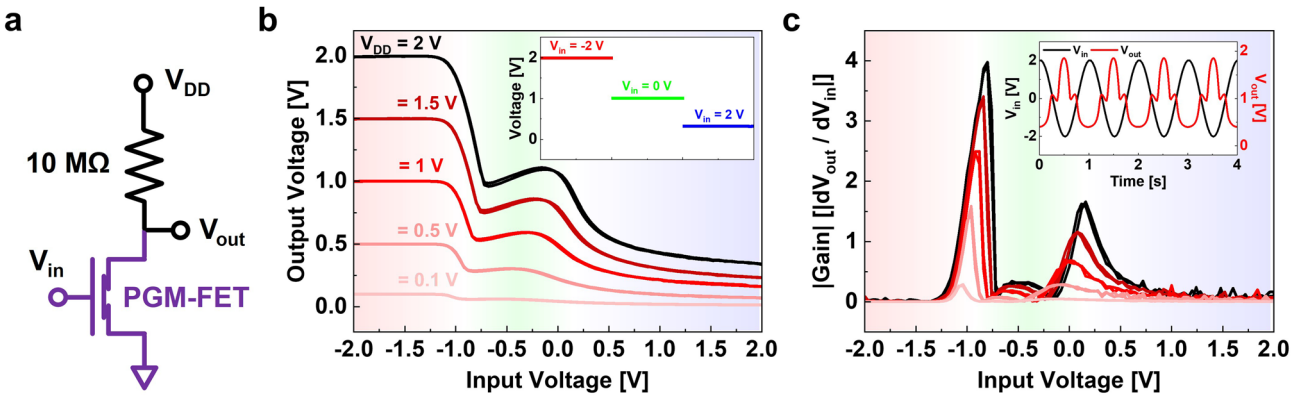

Fig. 3 **a** Circuit diagram of PGM-FET-based resistive-load inverter for multi-value logic circuit applications. **b** VTC characteristic curves of PGM-FET-based multi-value logic operations for V_{DD} ranging from 0.1 to 2 V. The inset shows three distinguished output states (ternary logic states). **c** Voltage gain of the demonstrated ternary inverter logic circuit for V_{DD} ranging from 0.1 to 2 V. The inset shows the dynamic V_{out} responses (red) from the sinusoidal waveform V_{in} (black). (Color figure online)

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(MoS_2). Based on the above understanding of the PGM-FET-based ternary logic circuit, we attempted to investigate a direct $PdSe_2$-MoS_2 junction FET (PMJ-FET) for a more advanced and practical device model, as shown in Fig. S5. Although the PMJ-FET also exhibits a non-classical humped I_D–V_G transfer curve and ternary logic circuit operation, the absence of the Gr-bridge interlayer results in rectifying properties at the $PdSe_2$/MoS_2 junction [58]. Consequently, the PMJ-FET exhibits asymmetric (having direction) device characteristics and a limitation in dynamic operation, whereas the PGM-FET exhibits symmetric (bidirectional) logic circuit operation properties. Furthermore, reliability problems remain in the PMJ-FET because controlling the optimized junction properties between the two different semiconductor active channels is difficult. As shown in Fig. S4d, the PMJ-FET does not trace the transfer curves of the MoS_2-FET and $PdSe_2$-FET because of the rectifying junction properties of MoS_2/$PdSe_2$ [42]. Therefore, adopting the Gr-bridge device structure will provide reliability and convenience for further study of high-end multi-value logic applications.

3.4 WSe_2-Gr-MoS_2 Heterostructure FET Device

As a second approach toward advanced electronic applications, WSe_2, a wide-bandgap ambipolar active channel, was chosen to realize the Gr-bridge heterostructure device instead of the $PdSe_2$-based ternary logic circuit. Figure 4a shows the 3D device schematic of WSe_2-Gr-MoS_2 FET, named "WGM-FET." Figure 4b, c shows the OM images before and after patterning of the extended S/D and G electrodes, respectively, through the same device fabrication processes of PGM-FET. The detailed process flow and thickness information for each layer are shown in Figs. S6 and S7, respectively. Figure 4d shows the I_D–V_G transfer curves of the MoS_2-FET (blue dashed line), WSe_2-FET (red dashed line), and WGM-FET (solid black line) at V_D of 2 V. In this case, the transfer curve of WGM-FET follows that of the MoS_2-FET in regions I and II and that of WSe_2-FET in regions III and IV. However, unlike the case of PGM-FET, the wider bandgap of the WSe_2 channel allows a low I_{OFF} level of WGM-FET (wider region III); therefore, the transfer characteristic curves resemble an uppercase letter

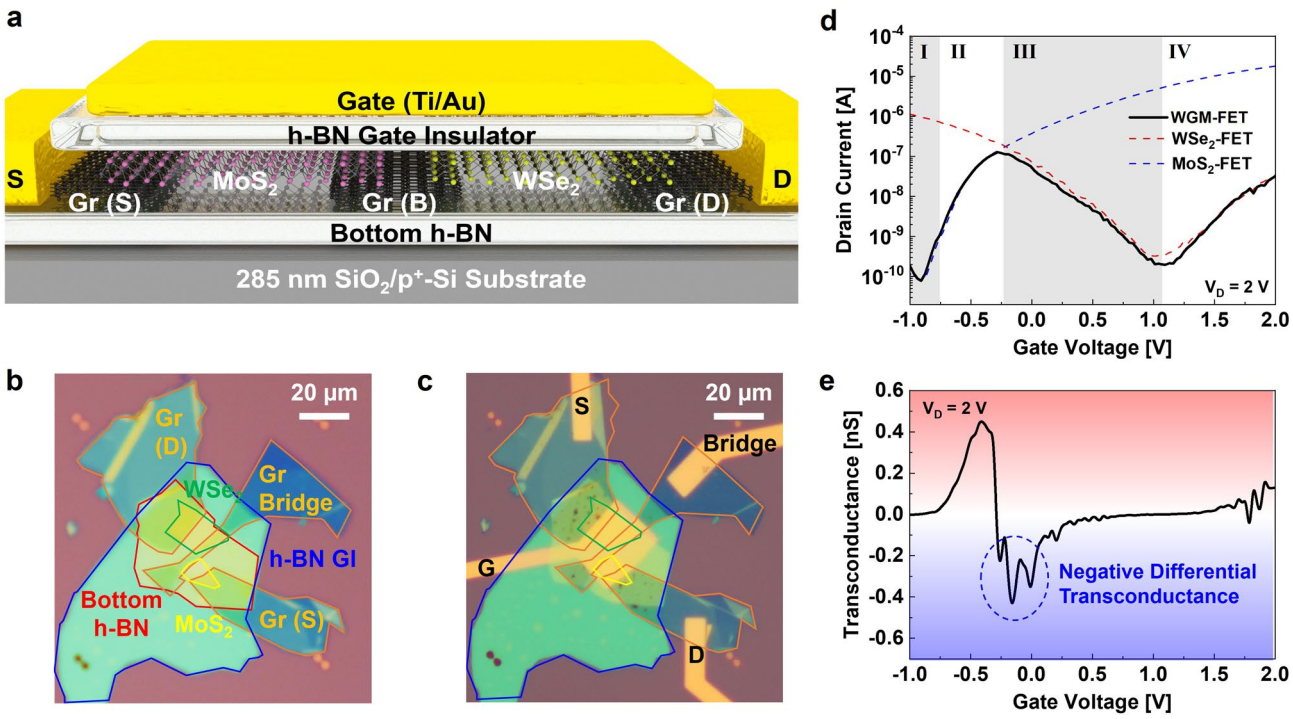

Fig. 4 **a** Cross-sectional 3D device schematic of the WSe_2-Gr-MoS_2 heterostructure FET (WGM-FET) for frequency tripler circuit applications. OM images of the WGM-FET **b** before and **c** after the extended metal electrode fabrication. **d** I_D–V_G transfer characteristic curves of the MoS_2-FET (blue dashed line), WSe_2-FET (red dashed line), and WGM-FET (black solid line). **e** Estimated transconductances of the WGM-FET obtained from **d**. (Color figure online)

"N". Figure 4e shows the g_m–V_G curve of the WGM-FET; a negative g_m was observed in operation region III owing to the *p*-type transition properties of the WSe_2 active channel.

3.5 WGM-FET-Based Frequency Tripler Circuit Applications

These non-classical transfer characteristics of the WGM-FET bring unique VTC characteristics of an upside-down letter "N"-like curve in inverter logic circuit applications, as shown in Fig. 5a. To achieve a resistive-load inverter circuit, an external resistor of 100 MΩ was connected to the WGM-FET. Figure 5b shows the VTC curve, and the four transition states were observed as sequentially "High", "Low", "High", and "Low" output states according to the voltage sweep of V_{in} at V_{DD} of 2 V. The inset shows the four distinguished logic states at V_{in} of − 1, − 0.5, 1, and 2 V. Figure 5c shows the voltage gain of our demonstrated inverter circuit, which has both negative and positive values.

The V_{in} sweep from "Low (− 1 V)" to "High (2 V)" should produce sequential output states of "High–Low–High–Low" and the backward V_{in} sweep from "High" to "Low" generated the reversed output states of

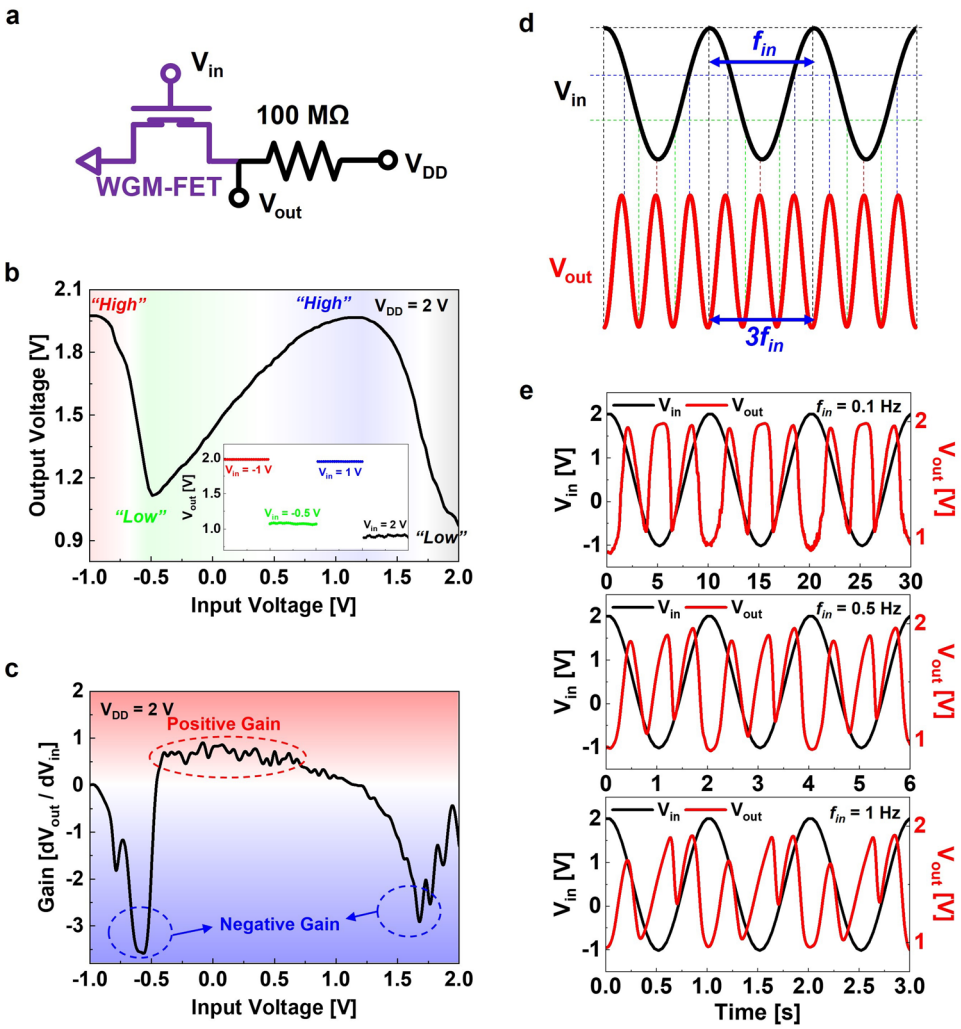

Fig. 5 **a** Circuit diagram of the WGM-FET-based resistive-load inverter circuit applications. **b** Upside-down letter "N"-like VTC curve of WGM-FET-based frequency tripler circuit operations at V_{DD} of 2 V. The inset shows four distinguished output states, that is, sequentially repeated "High" and "Low" states. **c** Voltage gain of the demonstrated WGM-FET-based frequency tripler circuit. **d** Expected frequency response of frequency tripler (three cycles of V_{out}) converted from a single cycle of V_{in}. **e** Real-time V_{out} responses (red) of the frequency tripler circuit for 0.1, 0.5, and 1 Hz input sinusoidal waveform V_{in} (black). (Color figure online)

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"Low–High–Low–High." That is, a double sweep of V_{in} of "Low–High–Low," similar to a single waveform, will produce the "High–Low–High–Low–High–Low–High" sequential output states. The repeatable "High" and "Low" output logic states enable an advanced frequency response application with respect to the sinusoidal waveform of V_{in}, as shown in Fig. 5d. As a result, a single cycle of sinusoidal waveform V_{in} should produce three cycles of the waveform V_{out}. This circuit application method can be regarded as a "frequency tripler," which can generate the output frequency (f_{out}) to triple the value from the input frequency (f_{in}). Finally, for the first time, we successfully demonstrated a frequency tripler application with a single Gr-bridge heterostructure FET consisting of a wide-bandgap ambipolar semiconductor. Figure 5e shows the real-time V_{out} responses for the 0.1, 0.5, and 1 Hz sinusoidal waveforms of V_{in} (see Fig. S8 for the real-time V_{out} response for the 1 Hz ramp waveform V_{in}). The V_{out} responses were analyzed using fast Fourier transform (FFT), as shown in Fig. S9. Our frequency response application should be economical to generate triple frequency toward low-power (frequency) and low-cost, more effective than the conventional frequency multiplier circuit for future advanced electronics.

4 Conclusions

In this study, Gr-bridge FETs consisting of laterally series-connected ambipolar semiconductor/Gr-bridge/*n*-type MoS_2 cascade channels were studied for high-end switching device applications based on their non-classical negative differential transconductance characteristics. The Gr-bridge layer could eliminate the Schottky junction properties between two semiconductor channels; therefore, the Gr-bridge FETs showed synthetic transfer characteristics, perfectly tracing the lower I_D of each channel material based on the simple resistance-in-series model, unlike the heterojunction devices without the Gr-bridge layer. Moreover, we successfully implemented two types of advanced electronic applications based on the bandgap properties of $PdSe_2$ (narrow-bandgap) and WSe_2 (wide-bandgap) ambipolar semiconductors for a multi-value logic inverter (PGM-FET) and frequency tripler (WGM-FET) circuits, respectively. Thus, we believe that the results of our Gr-bridge heterostructure devices and multi-functional circuit applications will provide reliability and convenience to open up a breakthrough toward future advanced electronics.

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