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Improved virtual synchronous control for grid-connected VSCs under grid voltage unbalanced conditions

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Abstract This paper presents an improved virtual synchronous control (VSynC) for the grid-connected voltage source converter (VSC) so as to continuously operate under the grid voltage with steady unbalance. The improved VSynC introduces the negative sequence power controls on basis of conventional VSynC. The improved VSynC is capable of regulating the negative sequence internal voltage to reduce the negative-sequence injected currents and oscillated powers of the VSC aroused by the negative-sequence grid voltage. Three alternative local control objectives for the VSC itself under steady state unbalanced grid conditions and their corresponding power references are deduced and computed. Simulated and experimental results are presented to validate the correctness and effectiveness of the proposed improved VSynC to enhance the continuous operation performance of VSynC-based VSCs during grid voltage steady-state unbalance.

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1 Introduction

In modern power system, more and more devices, e.g. high voltage direct current (HVDC) transmissions, energy storage systems and renewable energy generations, are integrated into power grid via voltage source converters (VSCs) [1, 2]. This poses great challenges to frequency dynamic and stability of power system due to the inertia loss. Virtual synchronous control (VSynC) is recently developed to feature the inertia characteristics in VSC to satisfy the requirement of inertial supports and frequency stability in power system [3–10].

Essentially, typical VSynC [3–10] usually employs second-order swing equations of synchronous generators to directly control the phase and magnitude motions of VSC's output voltage (i.e. internal voltage) and synchronize it with grid based on the active and reactive power deviations of VSCs. The inertia link ($\frac{1}{Js+D}$) in the swing equation features intrinsic inertia in the internal voltage of VSC for the natural inertial support to grid frequency. The typical control structures of various VSynC [5] can be classified with or without current control loops. Without rapid closed control loop of the current, the internal voltage is directly generated by the PWM (direct-VSynC). The direct VSynC can get more brief control structure and avoid some instability aroused by the current control. The control structure and dynamics of direct-VSynC [9, 10] are much different from the best-known vector current control (VC) [11, 12] and direct power control (DPC) [13, 14]. This paper mainly studies the direct VSynC.

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In fact, the steady-state imbalance of the grid voltage usually exists [15] due to steady-state imbalance of loads and transmission network. Under unbalanced grid voltage condition, the negative sequence grid voltage will produce the oscillated active and reactive powers at the twice grid frequency as well as the negative sequence currents. For the traditional VC and DPC, the enhanced control schemes have been widely studied to adapt the operation under steady-state grid voltage imbalance [16–26]. For VC, the positive- and negative-sequence current controllers [16–20] are used to control the positive- and negative-sequence internal voltages based on the VSC's positive- and negative-sequence current, respectively. In addition, the secondary level control based on the VC [21, 22] is designed for the VSC in micro grid to balance the grid voltage with the unbalanced load conditions. These methods regulate the reference voltage of the VSC's droop control to alter the negative sequence impedance according the negative sequence powers, which are grid level controls rather than a local control for VSCs. In the high voltage transmission network, the method in micro grid may not be completely effective. For DPC, due to its excellent dynamic performance, it has enough control bandwidth to completely synchronize the internal voltage with grid [23–26]. But, unfortunately, all the above-mentioned improved methods developed for VC and DPC are not appropriate for the VSynC due to their different control structures. The conventional VSynC directly regulates its internal voltage without any current controllers and under the effect of the inertia characteristic, the VSynC does not has enough control bandwidth to suppress the negative sequence currents and to handle the oscillated power components. Even under the steady-state slight imbalance, the negative current will become very large even damage the VSC, because it is only equal to the ratio between the negative sequence grid voltage and the impedance of filters.

As a newly developed control method for the VSC, the operation and control of the VSynC-based VSC itself are not widely discussed and studied under grid voltage steady-state imbalance, which limits the VSynC's developments and applications. [8] introduces a fault ride through method for the power synchronous controlled VSC, which employs current controllers to reduce the negative sequence currents during the fault in short term. But it is not suitable for the long-term operation of the VSC under the steady state unbalance. As a result, this paper aims to study an improved VSynC with the existing inertia characteristics and suitable for the long-term continuous operation under the steady-state unbalanced grid conditions, which will constitute the main contribution of this paper.

For the natural inertial support for grid frequency and enhancing the continuous operation capability of the VSynC-based VSC attached to voltage-unbalanced network, this paper introduces negative-sequence internal voltage and regulates its dynamics according to the negative sequence active and reactive power components. Then the set values of the positive- and negative-sequence powers are computed for the three local control objectives, i.e. eliminating the negative-sequence currents, removing active power or reactive power ripples through injecting required negative-sequence internal voltage.

The rest of this paper is organized as follows. In Section 2, the basic principle of conventional VSynC is introduced and the dynamic modeling is implemented under network voltage unbalanced conditions. Then the principle of developed negative-sequence synchronous control is introduced and the improved VSynC with different power references is presented to achieve the alternative control targets in Section 2. In Sections 4 and 5, the simulated and experimental results are presented to validate the performance of the improved VSynC, respectively. Finally, some conclusions are drawn in Section 6.

2 Modeling of VSCs based on virtual synchronous control

2.1 Virtual synchronous control (VSynC) under normal grid condition

The typical topology of grid-connected voltage source converter (VSC) is depicted in Fig. 1. Considering both terminal voltage (U_t) and internal voltage (U_c), i.e. output voltage of the VSC as ideal voltage sources, the internal voltage and terminal voltage vector can be written as:

$$\begin{cases} \boldsymbol{U}_c = U_c e^{j\theta_c} = U_c e^{j\omega_p t} \\ \boldsymbol{U}_t = U_t e^{j\theta_t} = U_t e^{j\omega_g t} \end{cases} \quad (1)$$

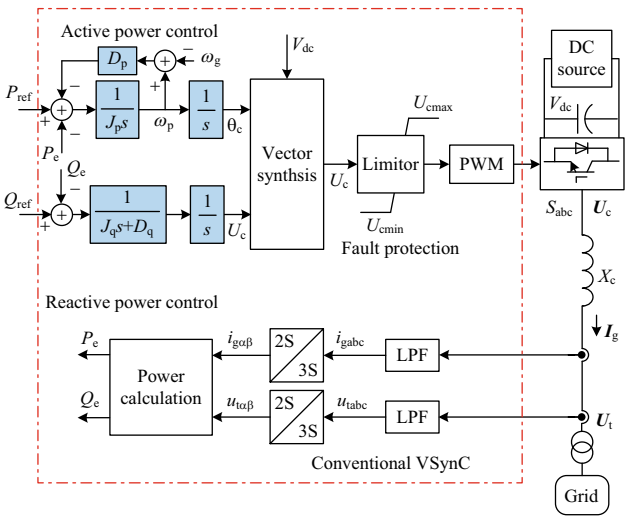


Fig. 1 Conventional VSynC for grid-connected VSCs

where U_c and U_t are the magnitudes of internal voltage and terminal voltage; θ_c and θ_t are the corresponding phase angles; ω_p and ω_g are the angular frequency of internal voltage and grid, ω_p is equal to ω_g under steady state.

The output currents and powers of VSC are given as:

$$\begin{cases} \boldsymbol{I}_g = \dfrac{\boldsymbol{U}_c - \boldsymbol{U}_t}{\mathrm{j}X_c} \\ P_e + \mathrm{j}Q_e = \boldsymbol{U}_t \hat{\boldsymbol{I}}_g \end{cases} \tag{2}$$

where X_c is the equivalent impedance of filter. In the high voltage transmission network, the resistor is usually ignored; P_e and Q_e are the instantaneous active and reactive powers of VSC.

The conventional VSynC [3–10] directly regulates the phase and magnitude of internal voltage for synchronizing with grid through the active and reactive power control as Fig. 1, and features the inertia in the internal voltage of VSC. The power controls are usually implemented by the second order controllers according to the errors of active and reactive powers, respectively, as (3):

$$\begin{cases} \theta_c = \dfrac{1}{s}\omega_p \\ \omega_p = \dfrac{1}{J_p s}(P_{ref} - P_e) - \dfrac{1}{J_p s} D_p(\omega_p - \omega_g) \\ U_c = \dfrac{1}{J_q s + D_q}\dfrac{1}{s}(Q_{ref} - Q_e) \end{cases} \tag{3}$$

where P_{ref} and Q_{ref} are the referred active and reactive powers. P_e and Q_e are the instantaneous powers. J_p, J_q, D_p and D_q are control parameters of the VSynC. A paralleled fault current limitator is usually employed to limit the fault current and cannot affect the normal operations, but it is out of the scope of this paper and not mainly concerned.

For providing the inertial supports to grid, the inertia characteristic should be featured in the power controllers. The Bode diagram of the active power controller is presented as Fig. 2. As shown in Fig. 2, the control bandwidth of VSynC with $J_p = 10$ and $D_p = 150$ is almost 4.41 Hz to provide the dynamic grid frequency support, which means that the oscillated power out of the frequency scope cannot be completely suppressed and handled. Larger inertia coefficient, more frequency supports. At the same time, the control bandwidth will decline as shown in Fig. 2.

2.2 VSynC-based VSC under unbalanced network voltage

When the network voltage is unbalanced, the voltage can be expressed as positive-sequence and negative-sequence components based on the symmetrical components theory [15].

$$\boldsymbol{U}_t = U_t^+ e^{\mathrm{j}\theta_t^+} + U_t^- e^{\mathrm{j}\theta_t^-} \tag{4}$$

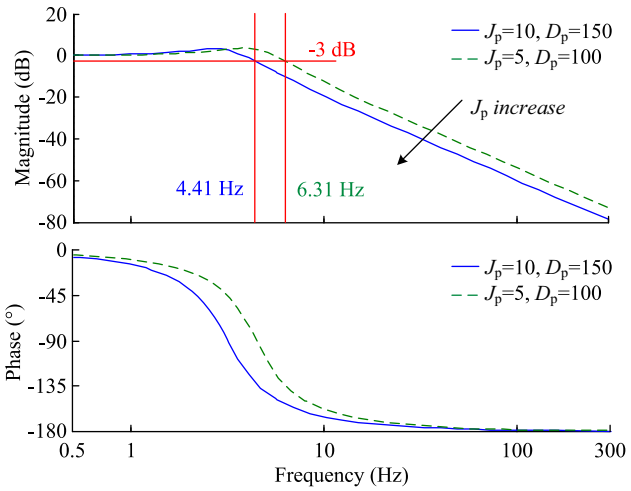


Fig. 2 Bode diagram of the VSynC's active power controller

where "+" and "−"denote the positive and negative sequence components (as shown in Fig. 3).

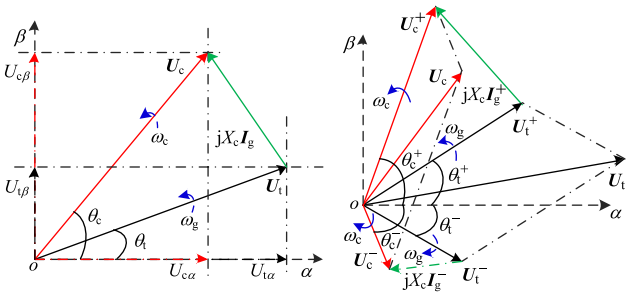
The internal voltage of VSC is also decomposed into positive- and negative-sequence components. Due to the limitation of the control bandwidth, the conventional VSynC cannot produce and control the negative sequence internal voltage component, viz. $\boldsymbol{U}_c^- \approx 0$.

$$\begin{cases} \boldsymbol{U}_c = \boldsymbol{U}_c^+ + \boldsymbol{U}_c^- \\ \boldsymbol{U}_c^+ = U_c^+ e^{\mathrm{j}\theta_c^+} \\ \boldsymbol{U}_c^- = U_c^- e^{\mathrm{j}\theta_c^-} \end{cases} \tag{5}$$

Then the positive-sequence and negative-sequence currents of VSC are expressed as:

$$\begin{cases} \boldsymbol{I}_g = \boldsymbol{I}_g^+ + \boldsymbol{I}_g^- \\ \boldsymbol{I}_g^+ = \dfrac{U_c^+ e^{\mathrm{j}\theta_c^+} - U_t^+ e^{\mathrm{j}\theta_t^+}}{\mathrm{j}X_c} \\ \boldsymbol{I}_g^- = \dfrac{U_c^- e^{\mathrm{j}\theta_c^-} - U_t^- e^{\mathrm{j}\theta_t^-}}{\mathrm{j}X_c} \end{cases} \tag{6}$$

Due to $\boldsymbol{U}_c^- \approx 0$, the negative sequence current magnitude is approximately equal to the U_t^-/X_c. Usually,



(a) Balanced grid voltage condition **(b)** Unbalanced grid voltage condition

Fig. 3 Phasor diagram of VSynC-based VSC under balanced and unbalanced network voltage conditions

the impedance of the filter is very small, about 0.1 p.u. Thus, the negative sequence grid voltage will produce very large current.

Substituting (4), (5) and (6) into (2), the active and reactive powers can be computed as:

$$\begin{cases} P_{\mathrm{e}} = P_{\mathrm{e0}}^{+} + P_{\mathrm{e0}}^{-} + P_{\mathrm{e1}} + P_{\mathrm{e2}} \\ Q_{\mathrm{e}} = Q_{\mathrm{e0}}^{+} + Q_{\mathrm{e0}}^{-} + Q_{\mathrm{e1}} + Q_{\mathrm{e2}} \end{cases} \tag{7}$$

$$\begin{cases} P_{\mathrm{e0}}^{+} = \dfrac{U_{\mathrm{c}}^{+} U_{\mathrm{t}}^{+} \sin\left(\theta_{\mathrm{c}}^{+} - \theta_{\mathrm{t}}^{+}\right)}{X_{\mathrm{c}}} \\ P_{\mathrm{e0}}^{-} = \dfrac{U_{\mathrm{c}}^{-} U_{\mathrm{t}}^{-} \sin\left(\theta_{\mathrm{c}}^{-} - \theta_{\mathrm{t}}^{-}\right)}{X_{\mathrm{c}}} \\ P_{\mathrm{e1}} = \dfrac{U_{\mathrm{c}}^{+} U_{\mathrm{t}}^{-} \sin\left(\theta_{\mathrm{c}}^{+} - \theta_{\mathrm{t}}^{-}\right) + U_{\mathrm{t}}^{+} U_{\mathrm{t}}^{-} \sin\left(\theta_{\mathrm{t}}^{-} - \theta_{\mathrm{t}}^{+}\right)}{X_{\mathrm{c}}} \\ P_{\mathrm{e2}} = \dfrac{U_{\mathrm{c}}^{-} U_{\mathrm{t}}^{+} \sin\left(\theta_{\mathrm{c}}^{-} - \theta_{\mathrm{t}}^{+}\right) + U_{\mathrm{t}}^{-} U_{\mathrm{t}}^{+} \sin\left(\theta_{\mathrm{t}}^{+} - \theta_{\mathrm{t}}^{-}\right)}{X_{\mathrm{c}}} \\ Q_{\mathrm{e0}}^{+} = \dfrac{U_{\mathrm{c}}^{+} U_{\mathrm{t}}^{+} \cos\left(\theta_{\mathrm{c}}^{+} - \theta_{\mathrm{t}}^{+}\right) - \left(U_{\mathrm{t}}^{+}\right)^{2}}{X_{\mathrm{c}}} \\ Q_{\mathrm{e0}}^{-} = \dfrac{U_{\mathrm{c}}^{-} U_{\mathrm{t}}^{-} \cos\left(\theta_{\mathrm{c}}^{-} - \theta_{\mathrm{t}}^{-}\right) - \left(U_{\mathrm{t}}^{-}\right)^{2}}{X_{\mathrm{c}}} \\ Q_{\mathrm{e1}} = \dfrac{U_{\mathrm{c}}^{+} U_{\mathrm{t}}^{-} \cos\left(\theta_{\mathrm{c}}^{+} - \theta_{\mathrm{t}}^{-}\right) - U_{\mathrm{t}}^{+} U_{\mathrm{t}}^{-} \cos\left(\theta_{\mathrm{t}}^{+} - \theta_{\mathrm{t}}^{-}\right)}{X_{\mathrm{c}}} \\ Q_{\mathrm{e2}} = \dfrac{U_{\mathrm{c}}^{-} U_{\mathrm{t}}^{+} \cos\left(\theta_{\mathrm{c}}^{-} - \theta_{\mathrm{t}}^{+}\right) - U_{\mathrm{t}}^{+} U_{\mathrm{t}}^{-} \cos\left(\theta_{\mathrm{t}}^{+} - \theta_{\mathrm{t}}^{-}\right)}{X_{\mathrm{c}}} \end{cases} \tag{8}$$

where P_{e0}^{+} and Q_{e0}^{+} are called positive-sequence active and reactive powers, which are generated by positive-sequence internal voltage and terminal voltage; P_{e0}^{-} and Q_{e0}^{-} are called negative-sequence active and reactive power generated by the negative-sequence internal voltage and terminal voltage; P_{e1} and Q_{e1} are the active and reactive power components oscillated at twice grid frequency by positive- sequence internal voltage and negative-sequence terminal voltage; P_{e2} and Q_{e2} are the oscillated active and reactive power components by negative-sequence internal voltage and positive-sequence terminal voltage; P_{e0}^{+}, Q_{e0}^{+}, P_{e0}^{-} and Q_{e0}^{-} are the constant components; P_{e1}, Q_{e1}, P_{e2} and Q_{e2} are the components oscillated at twice grid frequency. Due to the limited control bandwidth, the oscillated power components cannot be controlled and handled by the conventional VSynC, which will arouse severe power oscillations and is not acceptable by grid.

3 Improved virtual synchronous control

3.1 Negative-sequence power control

In order to handle the oscillated power components as shown in the (8), the negative-sequence internal voltage is injected to increase the control freedom degrees of VSynC-based VSC, and the corresponding negative sequence power controls are developed to synchronize the negative sequence internal voltage with the negative sequence grid voltage.

The negative sequence power control is designed as typical second-order controllers with the inputs of the negative-sequence active and reactive powers (P_{e0}^{-} and Q_{e0}^{-}) and their references (P_{ref}^{-} and Q_{ref}^{-}) as shown in Fig. 4. The negative sequence power controller are designed as:

$$\begin{cases} \theta_{\mathrm{c}}^{-} = -\dfrac{1}{s}\omega_{\mathrm{p}}^{-} \\ \omega_{\mathrm{p}}^{-} = \dfrac{1}{J_{\mathrm{p}}s}\left(P_{\mathrm{ref}}^{-} - P_{\mathrm{e}}^{-}\right) - \dfrac{1}{J_{\mathrm{p}}s} D_{\mathrm{p}}\left(\omega_{\mathrm{p}}^{-} - \omega_{\mathrm{g}}\right) \\ U_{\mathrm{c}}^{-} = \dfrac{1}{J_{\mathrm{q}}s + D_{\mathrm{q}}} \dfrac{1}{s}\left(Q_{\mathrm{ref}}^{-} - Q_{\mathrm{e}}^{-}\right) \end{cases} \tag{9}$$

The negative sequence power control is combined with the conventional power control as the improved VSynC as shown in Fig. 5. $u_{\mathrm{t}\alpha\beta}$ and $i_{\mathrm{g}\alpha\beta}$ are the $\alpha\beta$-axis components of grid voltage and current, respectively. $u_{\mathrm{t}\alpha\beta}^{+}$, $u_{\mathrm{t}\alpha\beta}^{-}$, $i_{\mathrm{g}\alpha\beta}^{+}$, $i_{\mathrm{g}\alpha\beta}^{-}$ are the positive-sequence and negative-sequence components of grid voltage and current, respectively.

3.2 Power reference calculation

Several alternative local control objectives for the VSC itself are analyzed and the corresponding power references are computed.

Target 1: Eliminating the negative-sequence currents to get balanced currents. This is to ensure safe and balanced heating of VSC.

Target 2: Removing the active power oscillations to output constant active power.

Target 3: Removing the reactive power oscillations to output constant reactive power.

These control targets are achieved through altering the positive and negative sequence references. For Target 1, the impact of negative-sequence voltage should be counteracted by the internal voltage of the VSC to eliminate the negative-sequence current. Thus the references of negative-sequence active and reactive powers are set as zero to guarantee the internal voltage of VSC coincided with negative-sequence network voltage.

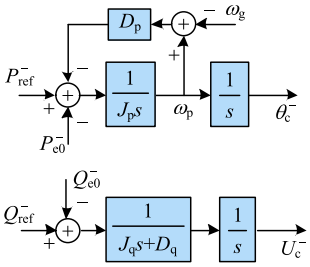


Fig. 4 Diagram of negative sequence power control block

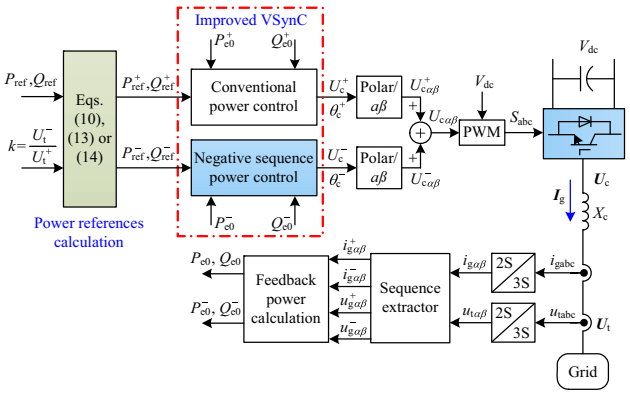


Fig. 5 Control diagram of the improved VSynC

$$\begin{cases} P_{\text{ref}}^{+} = P_{\text{ref}} \\ P_{\text{ref}}^{-} = 0 \\ Q_{\text{ref}}^{+} = Q_{\text{ref}} \\ Q_{\text{ref}}^{-} = 0 \end{cases} \tag{10}$$

The unbalance coefficient is defined as $k = U_t^-/U_t^+ . U_t^+$, then the oscillated active and reactive power components in (8) are simplified, and yields

$$\begin{cases} P_{\text{e1}} = k\left[P_{\text{e0}}^{+}\cos\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right) + Q_{\text{e0}}^{+}\sin\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right)\right] \\ P_{\text{e2}} = \dfrac{1}{k}\left[P_{\text{e0}}^{-}\cos\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right) - Q_{\text{e0}}^{-}\sin\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right)\right] \\ Q_{\text{e1}} = k\left[Q_{\text{e0}}^{+}\cos\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right) - P_{\text{e0}}^{+}\sin\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right)\right] \\ Q_{\text{e2}} = \dfrac{1}{k}\left[Q_{\text{e0}}^{-}\cos\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right) + P_{\text{e0}}^{-}\sin\left(\theta_{\text{t}}^{+} - \theta_{\text{t}}^{-}\right)\right] \end{cases} \tag{11}$$

For Target 2, the active power ripples of VSC should be removed viz. $P_{\text{e1}} + P_{\text{e2}} = 0$. According to (11), the power relations are expressed as:

$$\begin{cases} P_{\text{e0}}^{+} + \dfrac{1}{k^2}P_{\text{e0}}^{-} = 0 \\ Q_{\text{e0}}^{+} - \dfrac{1}{k^2}Q_{\text{e0}}^{-} = 0 \\ P_{\text{e0}}^{+} + P_{\text{e0}}^{-} = P_{\text{ref}} \\ Q_{\text{e0}}^{+} + Q_{\text{e0}}^{-} = Q_{\text{ref}} \end{cases} \tag{12}$$

Then, the positive and negative-sequence power references are computed.

$$\begin{cases} P_{\text{ref}}^{+} = -\dfrac{1}{k^2 - 1}P_{\text{ref}} \\ P_{\text{ref}}^{-} = \dfrac{k^2}{k^2 - 1}P_{\text{ref}} \\ Q_{\text{ref}}^{+} = \dfrac{1}{1 + k^2}Q_{\text{ref}} \\ Q_{\text{ref}}^{-} = \dfrac{k^2}{1 + k^2}Q_{\text{ref}} \end{cases} \tag{13}$$

Similarly, the power references can be obtained for Target 3 to guarantee $Q_{\text{e1}} + Q_{\text{e2}} = 0$.

$$\begin{cases} P_{\text{ref}}^{+} = \dfrac{1}{k^2 + 1}P_{\text{ref}} \\ P_{\text{ref}}^{-} = \dfrac{k^2}{k^2 + 1}P_{\text{ref}} \\ Q_{\text{ref}}^{+} = \dfrac{1}{1 - k^2}Q_{\text{ref}} \\ Q_{\text{ref}}^{-} = -\dfrac{k^2}{1 - k^2}Q_{\text{ref}} \end{cases} \tag{14}$$

Under balanced conditions, all the negative-sequence components are zero i.e. $k = 0$, thus both the negative – sequence active and reactive powers and their references are zero, and the negative-sequence internal voltage is also regulated to zero. As a result, the control performance of the VSynC-based VSC is dominated by the positive-sequence power control under balanced conditions.

3.3 Sequence extractor and feedback power calculation

In order to control the positive and negative sequence internal voltage, the positive and negative sequence active and reactive powers should be calculated as:

$$\begin{cases} P_{\text{e0}}^{+} = u_{\text{t}\alpha}^{+}i_{\text{g}\alpha}^{+} + u_{\text{t}\beta}^{+}i_{\text{g}\beta}^{+} \\ Q_{\text{e0}}^{+} = -u_{\text{t}\alpha}^{+}i_{\text{g}\beta}^{+} + u_{\text{t}\beta}^{+}i_{\text{g}\alpha}^{+} \\ P_{\text{e0}}^{-} = u_{\text{t}\alpha}^{-}i_{\text{g}\alpha}^{-} + u_{\text{t}\beta}^{-}i_{\text{g}\beta}^{-} \\ Q_{\text{e0}}^{-} = -u_{\text{t}\alpha}^{-}i_{\text{g}\beta}^{-} + u_{\text{t}\beta}^{-}i_{\text{g}\alpha}^{-} \end{cases} \tag{15}$$

where the positive and negative sequence components of grid voltage and current should be extracted to compute active and reactive powers.

This paper employs the amplitude-phase-locked loop (APLL) introduced in [27] to extract the positive and negative sequence components of grid voltage.

The construction of the basic APLL unit is shown in Fig. 6. The dynamic performance and mechanism of the APLL have been presented in [27], which is effective to extract the amplitude and phase of grid voltage. Where T_1, T_2 and D_1 are the control parameters of the APLL.

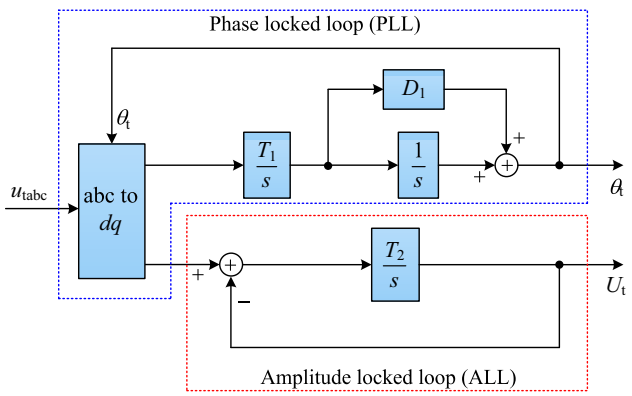


Fig. 6 Diagram of amplitude-phase-locked loop

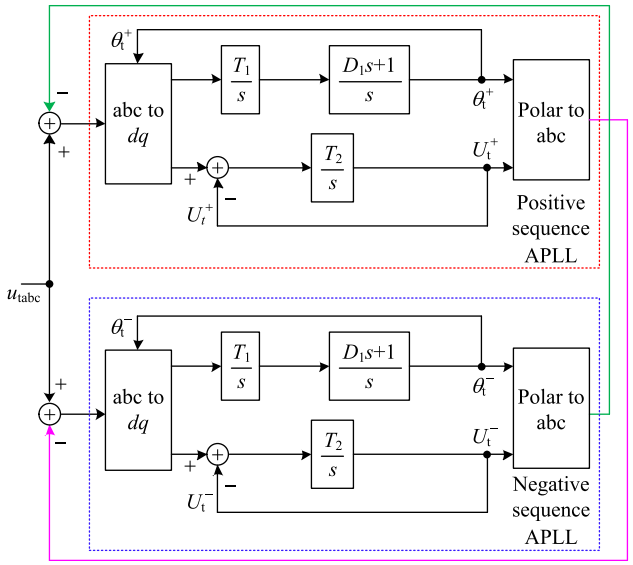


Fig. 7 Diagram of the positive and negative sequence APLL to decouple the positive- and negative-sequence components

But the only a basic APLL unit is just able to extract the positive sequence component of grid voltage, thus another APLL unit is combined as shown in Fig. 7 to decouple the positive and negative sequence grid voltage under the unbalanced grid conditions, respectively. Then the $\alpha\beta$-axis components can be calculated as:

$$\begin{cases} u_{t\alpha}^{+} = U_t^{+} \cos\ \theta_t^{+} \\ u_{t\beta}^{+} = U_t^{+} \sin\ \theta_t^{+} \\ u_{t\alpha}^{-} = U_t^{-} \cos\ \theta_t^{-} \\ u_{t\beta}^{-} = U_t^{-} \sin\ \theta_t^{-} \end{cases} \tag{16}$$

Moreover, the negative sequence current under the positive sequence reference frame oscillates at twice grid frequency, thus the notch filter [28] with a cut-off frequency at twice grid frequency is employed to extract the positive sequence current components under the positive sequence reference frame as shown in Fig. 8. Likewise the negative sequence current can be extracted.

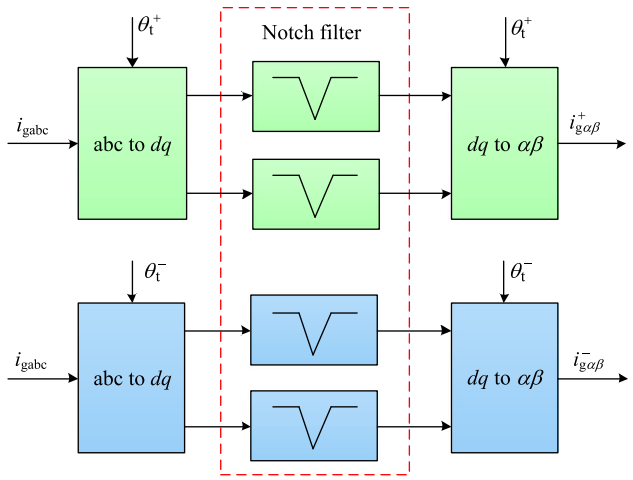
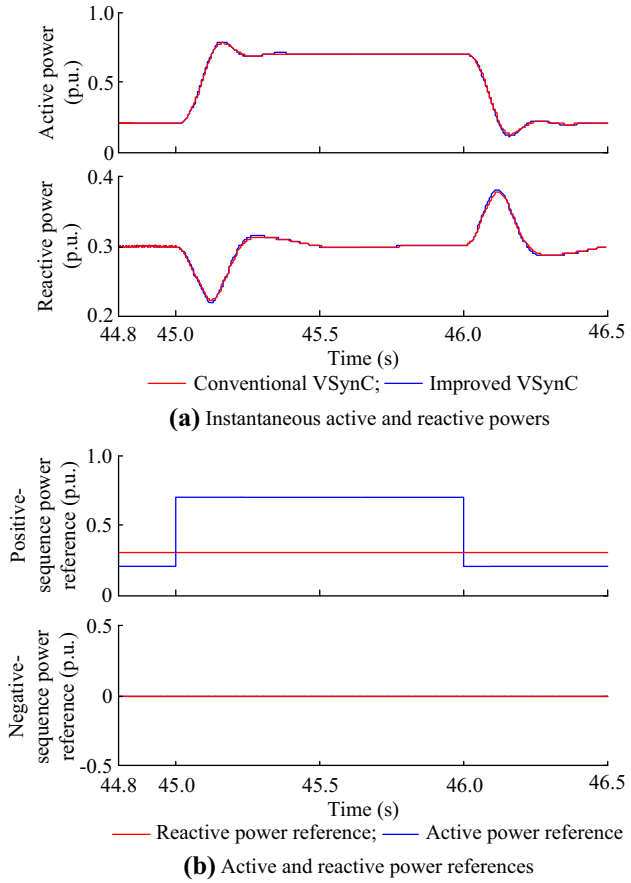


Fig. 8 Diagram of the sequence extraction for the current

Table 1 Parameters of simulated test system

Description	Value
Power and voltage base	2 MW, 0.69 kV
Filter impedance (X_c)	0.00796 + j0.0796 p.u.
DC-link voltage (V_{dc})	1.6 p.u.
Inertia coefficients (J_p, J_q)	2, 0.5
Damping coefficients (D_p, D_q)	150, 2



(a) Instantaneous active and reactive powers

(b) Active and reactive power references

Fig. 9 Performance of the grid-connected VSC based on the improved and conventional VSynC under balanced grid conditions

4 Simulated results

Simulations of the improved VSynC for a grid connected VSC were implemented by Matlab/Simulink. The simulated test system is established according to Fig. 1. A 2-MW VSC is integrated into grid through a transmission

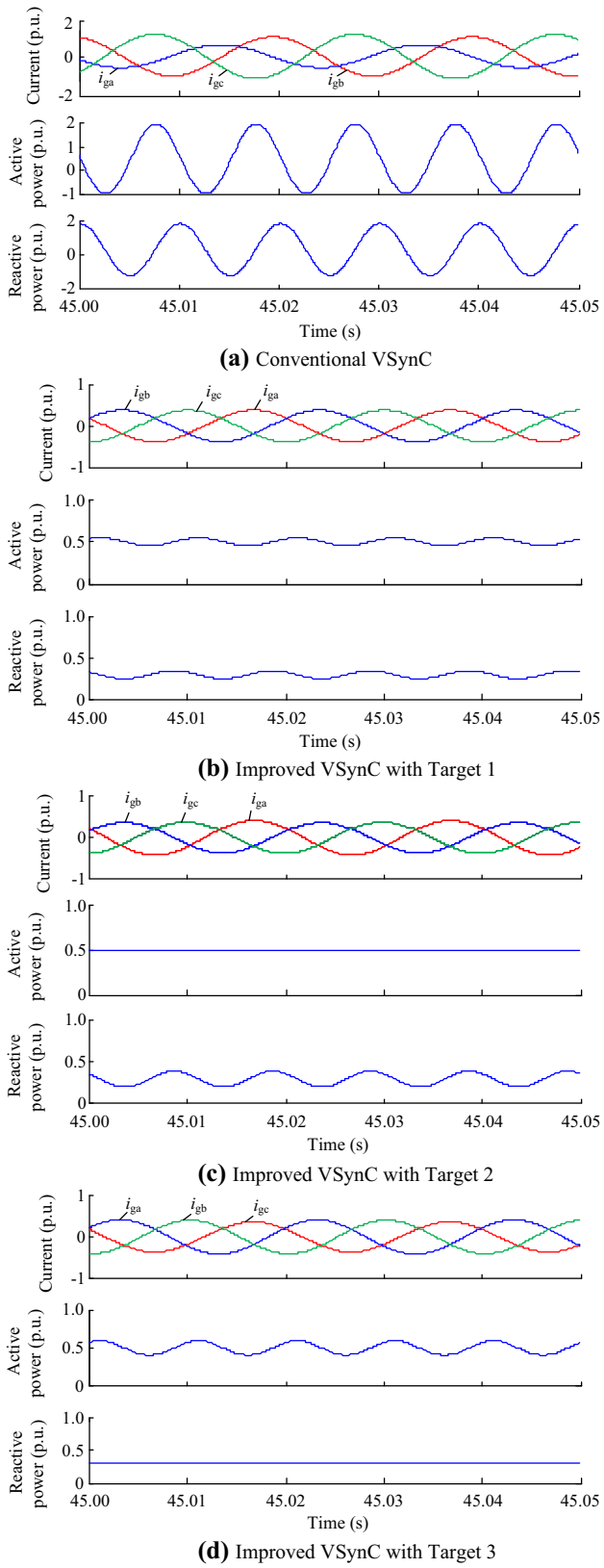


Fig. 10 Simulated results of the VSynC-based VSC under unbalanced grid conditions

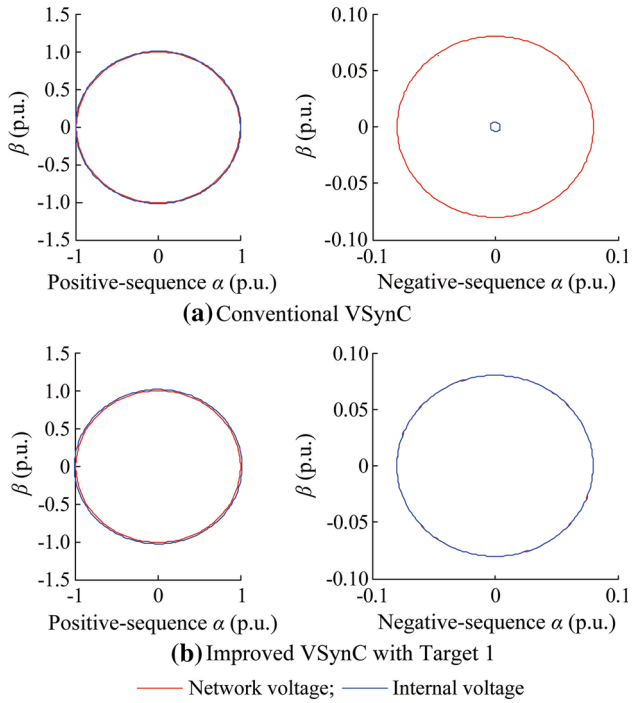


Fig. 11 Trajectory of positive- and negative-sequence grid and internal voltages of conventional and improved VSynC-based VSC

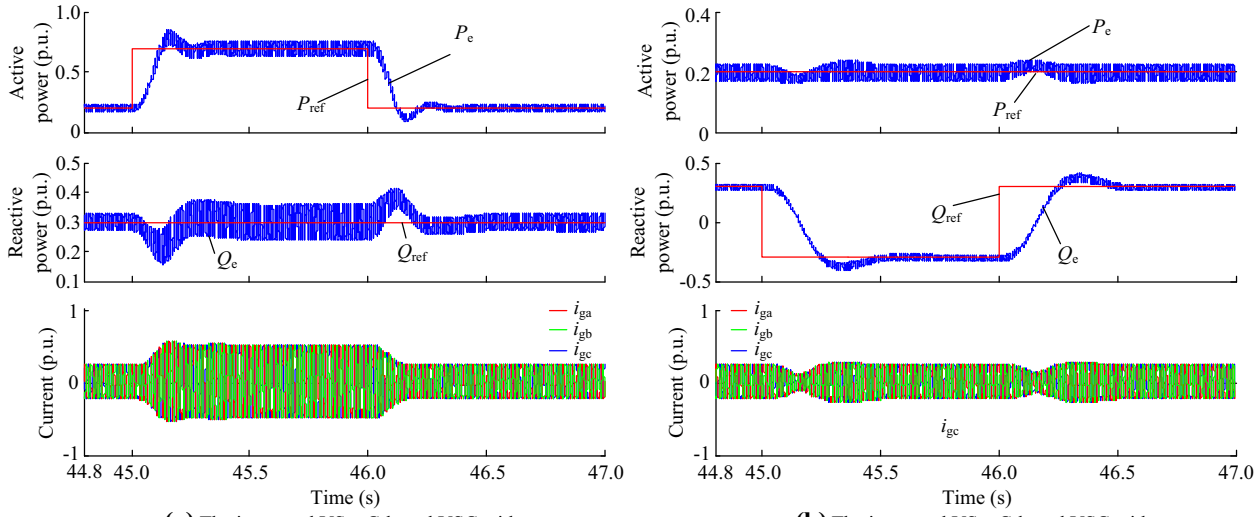
line. The voltage unbalance is created by injecting 8% of negative-sequence voltage into a three phase balanced voltage sources. In the simulation, the high-frequency current ripples are not mainly considered, thus the average model of VSC is adopted with no PWM dynamics. The detailed parameters of the simulated system are presented as Table 1.

4.1 Control performance of improved and conventional VSynC under normal grid conditions

Simulated results of the improved and conventional VSynC operating under balanced grid conditions are

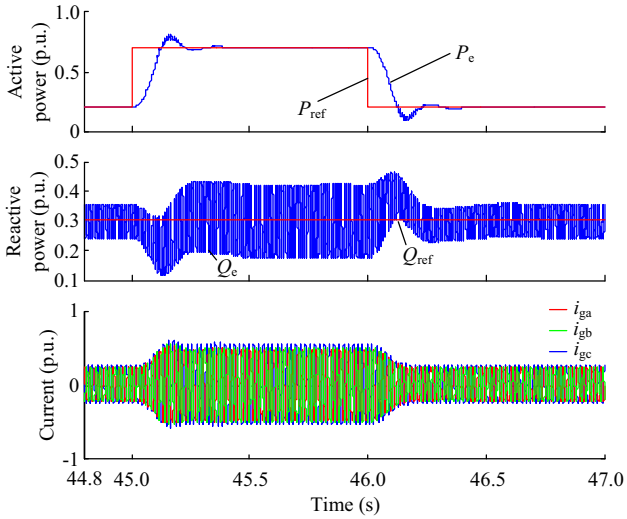
presented in Fig. 9a and b. Under balanced conditions, the power response of the conventional and improved VSynC are almost the same as shown in Fig. 9a. Because the negative-sequence grid voltage and current components are zero under balanced conditions, thus both the negative sequence powers and their references as shown in Fig. 9b are zero and the negative sequence power control also regulates the negative sequence internal voltage to zero.

As a conclusion, the supplement negative sequence power control in the improved VSynC scarcely influences the performance of VSynC under balanced conditions.

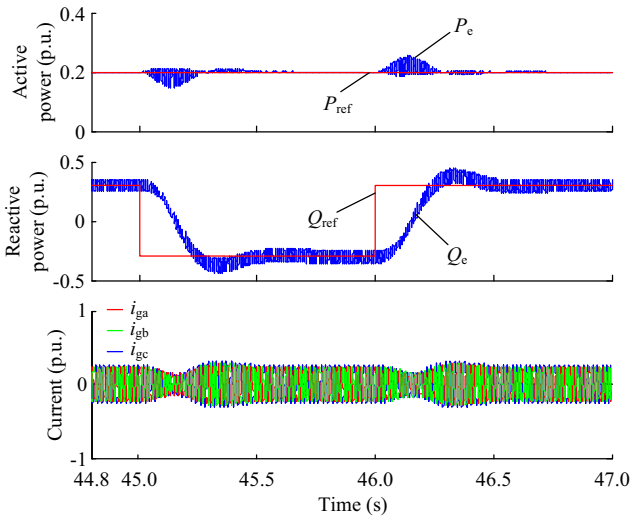


(a) The improved VSynC-based VSC with Target 1 during active power step

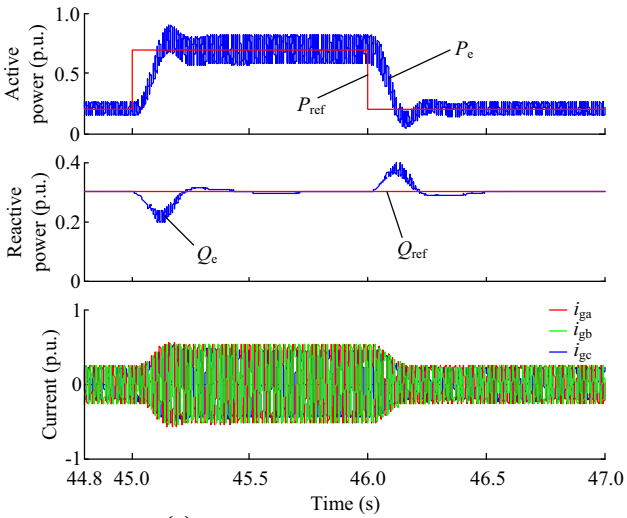
(b) The improved VSynC-based VSC with Target 1 during reactive power step



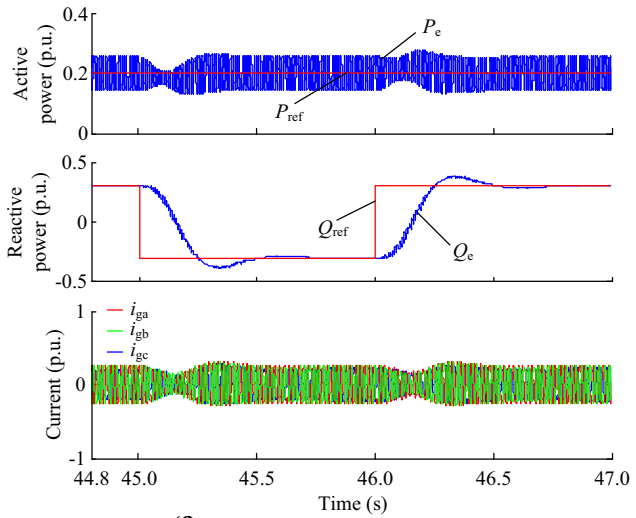
(c) The improved VSynC-based VSC with Target 2 during active power step



(d) The improved VSynC-based VSC with Target 2 during reactive power step



(e) The improved VSynC-based VSC with Target 3 during reactive power step



(f) The improved VSynC-based VSC with Target 3 during reactive power step

Fig. 12 Simulated results of the improved VSynC-based VSC under unbalanced grid conditions during active and reactive power step

4.2 Steady performance of the improved VSynC under unbalanced conditions

The steady performance is shown in Fig. 10, when the VSynC-based VSC is attached to the voltage-unbalanced network. With the conventional VSynC, the negative-sequence currents are very serious and the output power severely oscillates around the power reference at twice grid frequency.

Then when the improved VSynC with Target 1 is adopted, the negative-sequence current components of VSC are fully removed as Fig. 10b and the power ripples are obviously reduced. The effect of the negative sequence grid voltage is counteracted by the introduced negative sequence internal voltage, thus the negative sequence currents and powers are fully removed. While similarly, the active and reactive power ripples are eliminated with Target 2 and 3, respectively, as Fig. 10c and d. The unbalanced currents are reduced but not fully eliminated. The three alternative local control targets can be achieved.

The trajectory of the network voltages and the VSC's internal voltages is depicted in $\alpha\beta$-stationary reference frame as Fig. 11a and b, respectively. With the conventional VSynC, the positive-sequence internal voltage is completely synchronized with the positive-sequence network voltage, however there is very little negative-sequence internal voltage produced. The large negative-sequence voltage difference is going to produce large negative-sequence current, which will arouse trip-off and severe power oscillations of VSC. While both positive- and negative-sequence internal voltages are synchronized with grid voltage by using the improved VSynC. With Target 1, the negative-sequence internal voltage coincides with the negative-sequence grid voltage by the negative-sequence power control. Thus the influence of negative-sequence voltage is completely counteracted and then negative-sequence currents are fully removed.

4.3 Dynamic performance of the improved VSynC under unbalanced conditions

The dynamic-state performance of the improved VSynC –based VSC with different control targets under unbalanced conditions is illustrated as shown in Fig. 12a–f during the active and reactive power references change.

As shown in Fig. 12a, the active power reference is altered from 0.2 to 0.7 p.u. at 45 s and back to 0.2 p.u. at 46 s. Due to the influences of the negative-sequence voltage, the instantaneous active power of the improved VSynC–based VSC with Target 1 still oscillates at twice grid frequency but the average active power is follow the change of the actual active power reference as shown in Fig. 12a. And the average of the actual reactive power can also alter with the change of the reactive power reference of the improved VSynC-based VSC with Target 1.

Furthermore, the actual active and reactive powers of the improved VSynC-based VSC with Target 2 and 3 are shown as Fig. 12c, d and e, f, respectively. Both the averaged active and reactive powers can follow the change of the power references. As can be seen in Fig. 12, the dynamic state power responses of the improved VSynC-based VSC with different control targets are almost the same and is similar with the conventional VSynC.

5 Experimental validations

A 5 kW VSC prototype was set up to study and validate the performance of improved VSynC for VSC as Fig. 13. The conventional and improved VSynC were implemented in TI's TMS320F28335. The experimental results were recorded by YOKOGAWA's ScopeCorder DL850. The parameters of experimental prototype are given as Table 2. The switching and sampling frequency are 8 kHz and the nominal voltage is 250 V. A DC-source was employed to establish DC-link voltage of VSC. The unbalanced network voltage was created through a transformer with alternative taps. The unbalance coefficient (k) is around 0.15. The maximum current is set to even 40 A for the operation safe of the VSC and to observe VSC's performance during unbalance. The notch filter is used to decouple the positive

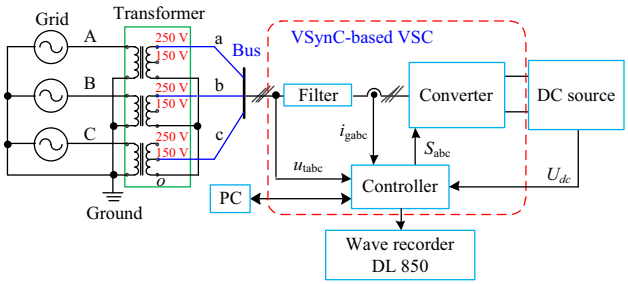


Fig. 13 Experimental test system

Table 2 Parameters of experimental system

Description	Value
Nominal power and voltage	5 kW, 250 V
Maximum current	40 A
Filter inductance (L_c)	10 mH
DC-link voltage (V_{dc})	650 V
Sample frequency (f_s)	8 kHz
Inertia coefficients (J_p, J_q)	10, 5
Damping coefficients (D_p, D_q)	200, 15

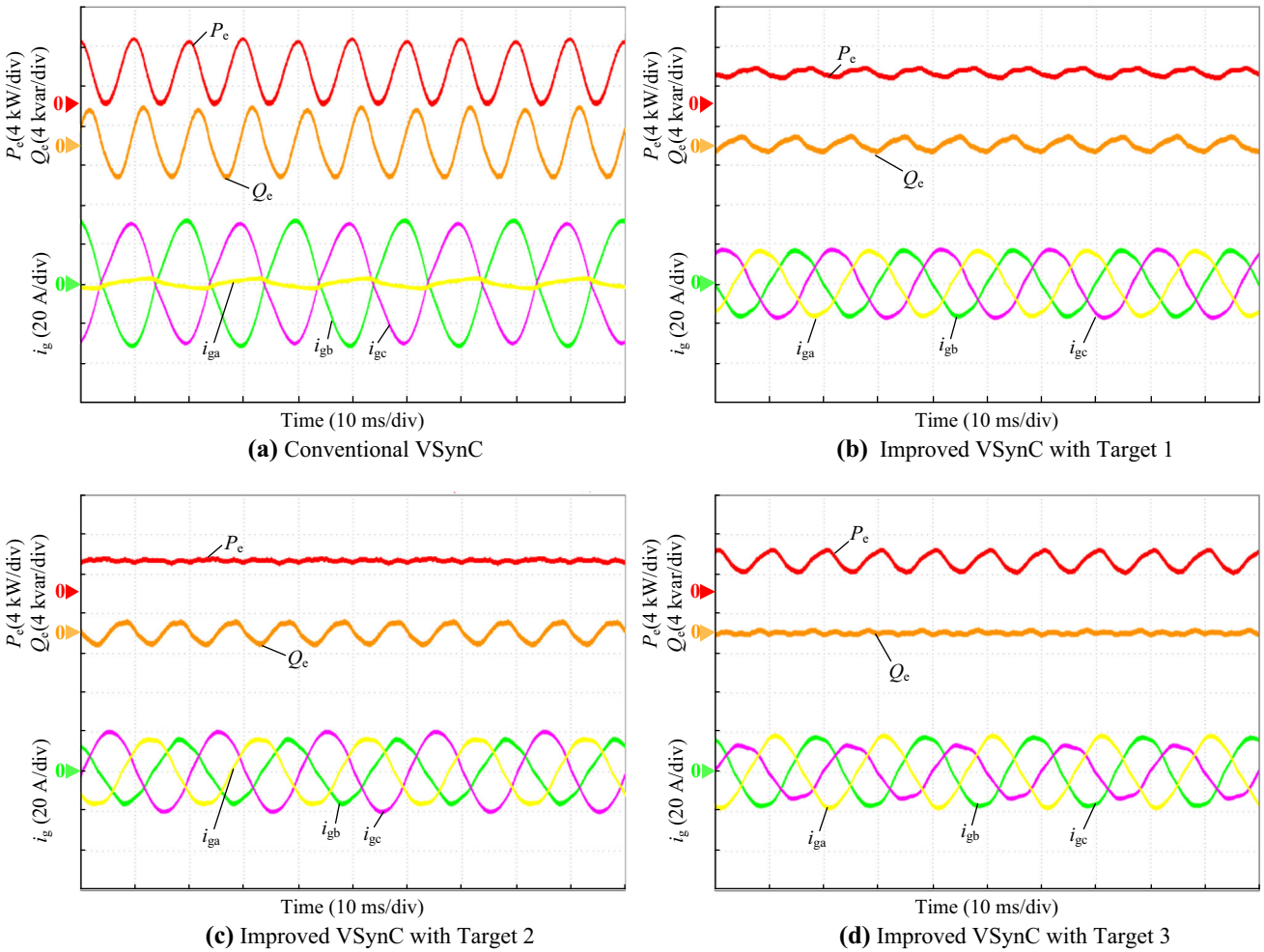


Fig. 14 Comparative experimental results of the VSC based on typical and improved VSynC with different control targets

and negative sequence components of grid voltage and current [28]. During the tests, the active and reactive power references (P_{ref} and Q_{ref}) are set to 3.2 kW and 0 kvar, respectively. Figure 14 depicts the experimental results. The active and reactive powers of the VSC based on conventional VSynC oscillates severely and the output currents are unbalanced with lots of negative-sequence currents as Fig. 14a. The largest phase current has nearly reached 23 A, which exceeds twice VSC's rated current and is going to trip off the VSC to avoid the damage in actual operation. But in the experiment, the maximum current capacity of VSC is enlarged to triple time for more clearly comparative results.

However, when the improved VSynC with Target 1 is employed, the negative-sequence currents are fully eliminated and the balanced output currents are obtained as Fig. 14b with the positive and negative-sequence power references as (9). The active and reactive power oscillations are obviously reduced but still existing. It is effective to avoid the trip-off and damage of VSC aroused by too large output currents. Moreover with Target 2 and 3 as Fig. 14c and d, the active and reactive power ripples are eliminated, respectively. And the unbalance of output currents is reduced in spite that the negative -sequence currents are still existing.

Furthermore, the current unbalance percentage (I_g^-/I_g^+) of conventional VSynC is around 92.6%. The active and reactive power ripples reach 58.4% and 66.7%. While using the improved VSynC with Target 1, the current unbalance percentage is reduced to 5.2%. With Target 2 and 3, the active and reactive power ripples are reduced to 0.8% and 1.2%, respectively.

Thus, the improved VSynC is able to achieve the identified alternative local control targets and enhances the performance of VSCs under unbalanced network.

6 Conclusion

This paper presents an improved VSynC for the continuous operations of grid-connected VSCS integrated into high voltage transmission network under unbalanced voltage conditions. In the improved VSynC, the negative sequence internal voltage is introduced and controlled so as to reduce the serious negative sequence currents and the oscillated powers. The positive and negative sequence power references are calculated to achieve the three basic alternative local control targets for the VSC itself, which are the basis of the further study on modifying the VSC's influence on grid voltage and frequency dynamic under grid unbalanced conditions. The experimental and simulated results validate the performance of the improved VSynC.

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