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High step-up quasi-Z-source DC–DC converters with single switched capacitor branch

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Abstract Aiming to integrate the respective merits of the switched-capacitor converter and the quasi-Z-source converter. An novel high step-up quasi-Z-source DC–DC converter with a single switched-capacitor branch is proposed. Compared to other high boost DC–DC converters, the proposed converter can provide higher output voltage gain, lower current stress across the switches, and lower voltage stress across the output diodes by using the same or similar passive and active components. Therefore, the efficiency and reliability of the converter can be improved. The topological derivation, operating principle, parameter selection, and comparison with other DC–DC converters are presented. Finally, both simulations and experimental results are given to verify the characteristics of the proposed converter.

Keywords DC–DC converter, High voltage gain, Quasi-Z-source network, Switched-capacitor

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1 Introduction

With the advance of modern industrial applications and the massive exploitation of conventional fossil energy, environmental pollution and energy shortages are becoming more and more serious. Therefore, it is necessary to develop new energy resources such as solar energy, and wind energy, which are renewable and environmental protection, to replace the traditional fossil energy [1, 2]. However, the output voltage of renewable energy sources tends to be low, and far from the desired dc-link voltage level of grid-connected inverters. Thus, there is more and more demand for high step-up DC–DC converters, and lots of research has been carried out on this topic. Many other industrial applications, such as TV-CRTs, X-ray systems, auxiliary power supplies for electrical vehicles, high-intensity discharge (HID) lamps for automobiles, also require dc/dc converters with high step-up voltage conversion ratio [3, 4].

Among the non-isolated DC–DC converter topologies, the traditional boost converter is one of the most commonly used topologies for voltage step-up. Theoretically speaking, its output voltage will be much higher than the input voltage when the duty ratio approaches 1. However, the duty ratio is limited when considering the parasitic parameters of each component. Therefore, in practical applications, the output voltage gain of the conventional boost converter is limited, which often cannot meet the requirements [5–7].

To obtain a higher voltage gain, conventional boost converters can be connected in series [8]. However, the whole system will become complicated due to many components and additional control units, which will increase its cost and size, degrade its efficiency and reliability. In addition to cascading, the voltage gain of the non-

isolated DC–DC converters can be increased effectively by using coupled inductors with an appropriate turn ratio instead of traditional inductors [9, 10].However, the energy stored in the leakage inductance is another problem, which needs to be solved by additional snubber circuits, leading to high volume, high weight and low efficiency.

A converter adopting interleaved configuration has been presented in [11], which can be used to reduce the voltage and current stress and obtain a high voltage gain. In [12] and [13], some high step-up DC–DC converters with voltage multiplier cells have been presented. Moreover, using switched-inductors to replace traditional inductors, some non-isolated high step-up converters have been proposed in [14–16]. Similarly, as presented in [17–22], switched capacitor techniques can also be utilized in DC–DCconverter topologies to achieve high voltage gain.

However, the above DC–DC converters are all very complex, and the output voltage gain is still not high enough for many practical applications. Therefore, in 2003, the simple, novel and efficient idea of a Z-source network was firstly proposed by [23]. The Z-source impedance network consists of two inductors and two capacitors, connected in an X-shape. The Z-source network was firstly applied in DC–AC inverters, i.e., the traditional Z-source inverter (ZSI) [23], which gives the inverter both buck and boost conversion ability in a single-stage topology. Since then, the Z-source network has greatly advanced due to its distinct advantages, e.g., it utilizes the shoot-through zero state to realize high voltage gain, no dead time is needed, and it avoid misgating-on caused by the electromagnetic interference (EMI). Therefore, the Z-source inverter is suitable for renewable power generation systems, such as, fuel cells and photovoltaic (PV) applications. Based on the Z-source network, many publications have been reported to develop the performance of ZSI, e.g., the improved ZSI in [24] and the quasi-Z-source inverter (qZSI) in [25–29].

Especially, the quasi-Z-source inverter, not only retains the main characteristics of the ZSI, but also has its own new features, such as continuous input current, low capacitor voltage stress and a common ground for the input and output. The Z-source network and the quasi-Z-source network can also be applied to boost the output voltage gain of DC–DC converters. In [30], a PWM Z-source DC–DC converter is proposed, and its output voltage gain is higher than the traditional boost converter. In [31], a novel Z-source DC–DC converter is presented, which uses the Z-source network to replace the traditional inductor in a conventional boost converter. In [32], based on the quasi-Z-source network, a modified Z-source DC–DC converter is proposed, which provides a higher voltage gain than the converter in [30]. However, the output voltage-gains of these Z-source DC–DC converters are still not large enough for many industrial applications, so it remains a challenge to design higher step-up DC–DC converters.

In this paper, a novel high step-up quasi-Z-source DC–DC converter with a single switched-capacitor branch is proposed and thus named a switched-capacitor quasi-Z -source converter (SC-qZSC). When the switch is turned off, the energy transferred from the inductors is used to charge the capacitors in parallel. When switch is on, the switched capacitors are connected in series to supply the load. Therefore, the converter can provide higher output voltage gain.

The rest of the paper is organized as follows. Section 2 describes the derivation and configuration of the proposed converter. The operating principle and parameter selection are presented in Section 3 and Section 4, respectively. Section 4 also presents the boundary condition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and the load ranges of the proposed converter under the CCM condition. It is followed by the comparison with other DC–DC converters in Section 5. In Section 6 and Section 7, the simulation and experimental results are presented respectively to verify the theoretical analysis. Finally, a conclusion is drawn in Section 8.

2 Configuration of the proposed converter

Based on the switched-capacitor converter in Fig. 1 [17], and the quasi-Z-source converter in Fig. 2 [32], the proposed converter is depicted in Fig. 3. The basic idea of the proposed converter is using an additional single switched capacitor branch (C_2, D_2) combined with another single switched-capacitor branch (C_1, D_1) which is hidden in the quasi-Z-source network to form a switched-capacitor cell(C_1, C_2, D_1, D_2).As shown in Fig. 3, the quasi-Z-source network consists of inductors L_1, L_2, capacitors C_1, C_3, and diode D_1.By combining the switched-capacitor cell with the quasi-Z-source network, the proposed converter can reach a higher output voltage gain. According to the position of the additional switched-capacitor branch (C_2, D_2), two kinds of SC-qZSC can be constructed, as shown in Fig. 3(a) and Fig. 3b.

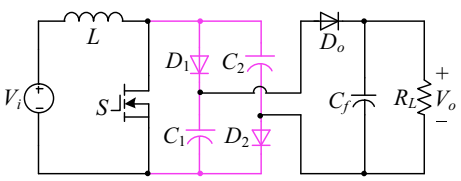


Fig. 1 Boost converter with a switched-capacitor cell

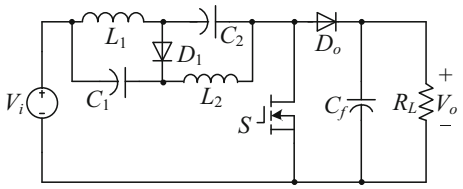
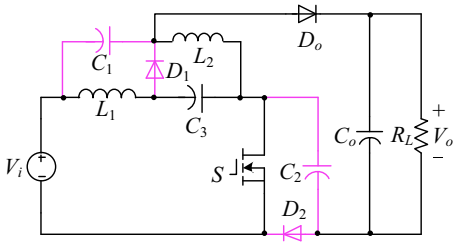
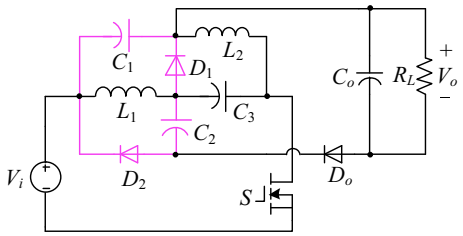


Fig. 2 Modified Z-source DC-DC converter



(a) SC-qZSC Type-1



(b) SC-qZSC Type-2

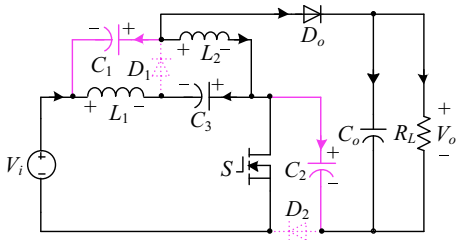
Fig. 3 Configuration of the proposed converter

3 Operating principle of proposed converter

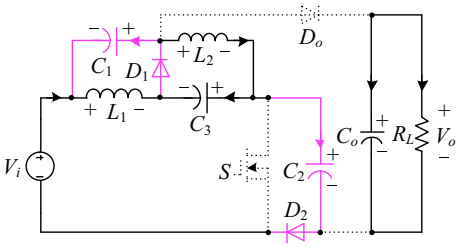
For simplicity, the steady state analysis of the proposed converter is based on the following assumptions.

1) The power switch S (MOSFET), diodes, load resistors, inductors and capacitors are all ideal, and the parasitic effect is ignored.
2) L_1=L_2=L and C_1=C_3=C in the quasi-Z-source network, and C_1=C_2=C in the switched-capacitor cell, thus C_1=C_2=C_3=C.

Referring to Fig. 3a, when the converter is operating in CCM, there will exist two operation modes, and the corresponding equivalent circuits are shown in Fig. 4. When switch S is on, as shown in Fig. 4a, diodes D_1 and D_2 are off due to the reverse parallel connection with capacitors. The input voltage V_i and C_3 charge L_1, and V_i and C_1 charge L_2. Meanwhile, C_1 and C_2 are in series with V_i to supply the load through S. By applying Kirchoff voltage law, the following steady-state equations can be derived: v_{L1}=V_i+V_{C3}, v_{L2}=V_i+V_{C1}, and v_o=V_i+V_{C1}+V_{C2}. When S is turned off, as shown in Fig. 4b, D_1 and D_2 are on, D_o is reverse blocking, inductor L_1 charges C_1, L_2 charges C_3, V_i and L_1 are in series with L_2 to charge C_2, and the load R_L is powered by capacitor C_o. Thus, similar relationships can be



(a) Mode 1: S, $D_o$on, D_1, D_2 off



(b) Mode 2: D_1, D_2 on, S, D_o off

Fig. 4 Equivalent circuits of the proposed SC-qZSC Type-1

obtained: v_{L1}+V_{C1}=0, v_{L2}+V_{C3}=0, and V_i=v_{L1}−V_{C3}+V_{C2}. By the volt-second balance principle of the inductor, the average voltage across an inductor is zero in the steady state. Defining the duty cycle of S as D=T_{on}/T_s, where T_{on} is the conduction time of switch S, T_s is the corresponding switching period. Thus, we have:

$$V_{C1} = V_{C3} = \frac{D}{1-2D} V_i \tag{1}$$

$$V_{C2} = V_i + V_{C1} + V_{C3} = \frac{1}{1-2D} V_i \tag{2}$$

From (1) and (2), the output voltage V_o can be derived as:

$$V_o = V_i + V_{C1} + V_{C2} = \frac{2-D}{1-2D} V_i \tag{3}$$

Thus, the output voltage gain G of the proposed SC-qZSC Type-1 converter can be obtained as:

$$G = \frac{V_o}{V_i} = \frac{2-D}{1-2D} \tag{4}$$

Similarly, for the converter in Fig. 3b, when S is turned on, diodes D_1 and D_2 are off, V_i and C_3 charge L_1, and V_i and C_1 charge L_2. Meanwhile, C_1 and C_2 are in series with V_i and C_3 to supply the load through S. By applying Kirchoff voltage law, one can obtain the following equations: v_{L1}=V_i+V_{C3}, v_{L2}=V_i+V_{C1}, and v_o=V_i+V_{C1}+V_{C2}+V_{C3}. When S is turned off, D_1 and D_2 are on, diode D_o is reverse blocking, the inductor L_1charges C_1 and C_2 in parallel, L_2 charges C_3, and the load is powered by capacitor C_o. Thus, v_{L1}+V_{C1}=0, v_{L1}+V_{C2}=0, and v_{L2}+V_{C3}=0. By the volt-second balance principle of inductors L_1 and L_2, one can obtain:

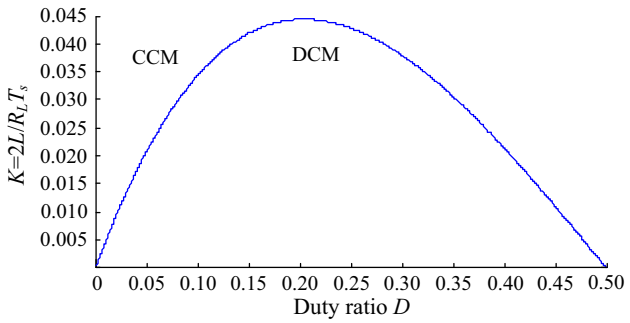


Fig. 5 Boundary condition K as a function of duty ratio D

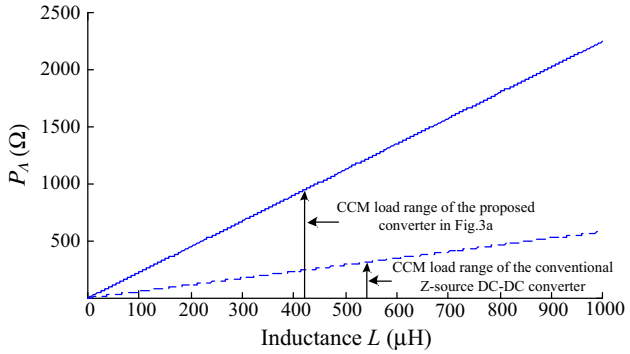


Fig. 6 Comparison of CCM load ranges between the proposed converter and the conventional Z-source DC-DC converter

$$V_{C1} = V_{C2} = V_{C3} = \frac{D}{1-2D} V_i \tag{5}$$

$$V_o = V_i + V_{C1} + V_{C2} + V_{C3} = \frac{1+D}{1-2D} V_i \tag{6}$$

Therefore, the output voltage gain G' of SC-qZSC Type-2 can be derived as:

$$G' = \frac{V_o}{V_i} = \frac{1+D}{1-2D} \tag{7}$$

Comparing the output voltage gain (4) with (7), it can be found that the output voltage gain of SC-qZSC Type-1 is higher than that of SC-qZSC Type-2. That is, G=G'+1. Therefore, we will take the SC-qZSC Type-1 as the example to present a detailed analysis in the rest of the paper.

4 Parameter selection

Based on the operating principle analysis in Section 3, parameter selection for SC-qZSC Type-1 will be discussed in this section. Normally, parameterselectionof passive and active components in a converter mainly depends on their rated voltages and rated currents. Hence, the voltage and current stresses of each component will be deduced first.

4.1 Voltage stress of each component

According to the operating principle analysis in Section 3, when switch S is on, diodes D_1 and $D_2$are off. From Fig. 4a, the voltage stresses of D_1 and D_2 can be obtained as:

$$V_{D_1} = V_{D_2} = \frac{1}{1-2D} V_i \tag{8}$$

When S is off, diodes D_1 and D_2 are on, and D_o is off. From Fig. 4b, the voltage stresses of S and D_o can be obtained as:

$$V_s = V_{D_o} = \frac{1}{1-2D} V_i \tag{9}$$

The output voltage V_o and capacitor voltage stresses have been derived in Section 3.

4.2 Current stress of each component

Based on the ampere-second balance property of capacitor C, the average current through a capacitor in steady state is zero, and applying Kirchoff current law to capacitors C_1, C_2, C_3 and C_o in Fig. 4a and b, we have:

$$\begin{cases} \int_0^{DT_s} (i_{L1\_on} - i_{in\_on})\mathrm{d}t + \int_{DT_s}^{T_s} (i_{L1\_off} - i_{in\_off})\mathrm{d}t = 0 \\ \int_0^{DT_s} (i_{L1\_on} + i_{L2\_on} - i_{in\_on})\mathrm{d}t + \int_{DT_s}^{T_s} i_{in\_off}\mathrm{d}t = 0 \\ \int_0^{DT_s} (-i_{L1\_on})\mathrm{d}t + \int_{DT_s}^{T_s} (i_{L2\_off} - i_{in\_off})\mathrm{d}t = 0 \\ \int_0^{DT_s} (i_{in\_on} - i_{L1\_on} - i_{L2\_on} - I_o)\mathrm{d}t + \int_{DT_s}^{T_s} (-I_o)\mathrm{d}t = 0 \end{cases} \tag{10}$$

where i_{L_on}, i_{L_off} and i_{in_on}, i_{in_off} are the inductor currents and the input currents when S is on and off, respectively. Assuming that the inductors are large enough, and the inductor currents in each operating mode change linearly, the average inductor current can be expressed as:

$$I_L = \frac{1}{DT_s} \int_0^{DT_s} i_{L\_on}\mathrm{d}t = \frac{1}{(1-D)T_s} \int_{DT_s}^{T_s} i_{L\_off}\mathrm{d}t \tag{11}$$

Combining (11) with (10), we can obtain:

Table 1 Voltage and current stresses of the proposed converter Proposed SC-qZSC Type-1

Parameter	Voltage stress	Parameter	Current stress
C_1,C_3	$\frac{D}{1-2D} V_i$	L_1	$\frac{2-D}{1-2D} I_o$
C_2	$\frac{1}{1-2D} V_i$	L_2	$\frac{1+D}{1-2D} I_o$
D_1,D_2	$\frac{1}{1-2D} V_i$	D_1	$\frac{2-D}{1-2D} I_o$
D_o	$\frac{1}{1-2D} V_i$	D_2,D_o	I_o
S	$\frac{1}{1-2D} V_i$	S	$\frac{1+D}{1-2D} I_o$

$$\begin{cases} I_{L1} = \dfrac{2-D}{1-2D} I_o \\ I_{L2} = \dfrac{1+D}{1-2D} I_o \end{cases} \tag{12}$$

When switch S is turned on, the currents through S and the output diode D_o are:

$$\begin{cases} I_S = \dfrac{1+D}{D(1-2D)} I_o \\ I_{Do} = \dfrac{I_o}{D} \end{cases} \tag{13}$$

When S is turned off, the currents through diodes D_1, D_2 are:

$$\begin{cases} I_{D1} = \dfrac{2-D}{(1-D)(1-2D)} I_o \\ I_{D2} = \dfrac{1}{1-D} I_o \end{cases} \tag{14}$$

Therefore, the average current flow through switch S and the diodes over a switching period can be derived as:

$$\begin{cases} I_{D_1} = \dfrac{2-D}{1-2D} I_o \\ I_{D_2} = I_{D_o} = I_o \\ I_s = \dfrac{1+D}{1-2D} I_o \end{cases} \tag{15}$$

4.3 Parameter selection of inductors

1) Inductors L_1 and L_2: When switch S is off, the inductance of L_1 and L_2, can be derived based on following differential equation:

$$L = \frac{v_L \mathrm{d}t}{\mathrm{d}i_L} \tag{16}$$

where $\mathrm{d}i_L$ is the inductor current rippleduring the OFF state, and $\mathrm{d}t$=(1-D)T_s is the duration of the OFF state. Generally, a larger inductor current ripple will cause a larger current stress in the switch and diodes. Thus, the inductor current ripple should be limited to a permitted range. For a given permitted fluctuation range x_L% of the inductor current, $\mathrm{d}i_L$ can be expressed as:

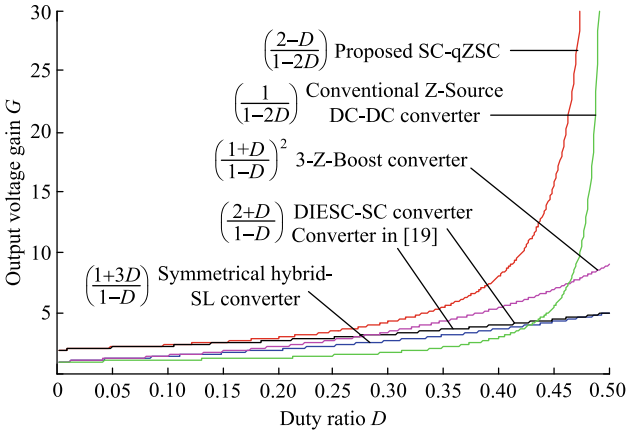


Fig. 7 Comparison of output voltage gains

$$\mathrm{d}i_L = \frac{v_L \mathrm{d}t}{L} = x_L\% I_L \tag{17}$$

Then, from Fig. 4b, (16) and (17), we have:

$$L_1 = \frac{(1-D)T_s V_{C1}}{x_L\% I_{L1}} \quad L_2 = \frac{(1-D)T_s V_{C3}}{x_L\% I_{L2}} \tag{18}$$

Substituting (1) and (12) into (18), the inductance L_1 and L_2 should satisfy the following equations:

$$\begin{cases} L_{1\min} \geq \dfrac{D(1-D)(1-2D)R_L}{(2-D)^2 x_L\% f_s} \\ L_{2\min} \geq \dfrac{D(1-D)(1-2D)R_L}{(1+D)(2-D)x_L\% f_s} \end{cases} \tag{19}$$

It can be observed that for a given load resistance $\mathrm{R_L}$and the duty ratio D, the inductance of L_1 and L_2will be determined by (19) directly.

2) Boundary condition between CCM and DCM: In order to ensure the proposed converter operates in continuous conduction mode, the inductor currents (i_{L1}, i_{L2}) should be maintained continuously during a whole switching cycle, thus:

$$\begin{cases} I_{L1} - \dfrac{1}{2}\Delta i_{L1} \geq 0 \\ I_{L2} - \dfrac{1}{2}\Delta i_{L2} \geq 0 \end{cases} \tag{20}$$

Substituting (12) and (17) into (20), then we have:

Table 2 Comparison of the number of components

Topologies	Inductors	Capacitors	Diodes	Switches
Symmetrical hybrid-SL converter	4	1	7	2
Converter in [19]	1-coupled inductor	4	4	1
3-Z-network boost converter	4	2	9	1
3-Z-network boost converter	2	5	4	1
Proposed SC-qZSC Type-1	2	4	3	1

$$\begin{cases} \dfrac{2L_1}{R_L T_s} \geq \dfrac{D(1-D)(1-2D)}{(2-D)^2} \\ \dfrac{2L_2}{R_L T_s} \geq \dfrac{D(1-D)(1-2D)}{(1+D)(2-D)} \end{cases} \tag{21}$$

Because the Z-source network is symmetric, L_1=L_2=L. Therefore, from (21), the boundary condition between CCM and DCM can be expressed as:

$$\frac{2L}{R_L T_s} \geq \frac{D(1-D)(1-2D)}{(1+D)(2-D)} \tag{22}$$

Denote K=$2L/R_L T_s$, and then, Fig. 5 shows a plot of the critical ratio K as a function of duty ratio D at the CCM and DCM boundary.

From (22), we can obtain:

$$R_L \leq \frac{2Lf_s(2+D-D^2)}{2D^3-3D^2+D} \tag{23}$$

which is the limited load condition for the converter operating in CCM. The load R_L is proportional to the inductance L in (23). Thus, by increasing the inductance L, the load capacity of the converter can be further enhanced. Based on (23), when the duty ratio D is equal to 0.204, the maximum load resistance $R_{L\max}$ can be derived as (24) for CCM operation.

$$R_{L\max} = \frac{2Lf_s}{0.0445} \tag{24}$$

Therefore, the proposed converter will operate in continuous conduction mode regardless of the duty ratio D as long as the load R_L satisfies $R_L \leq R_{L\max}$.

Moreover, a comparison of the CCM load range has been made between the proposed converter and the conventional Z-source DC–DC converter in [30], as shown in Fig. 6, for which the switching frequency f_s is set to 50kHz . It can be seen that the load range of the proposed SC-qZSC Type-1 converter is much wider than that of the conventional Z-source DC–DCconverter with the same inductance.

4.4 Parameter selection of capacitors

1) Capacitors C_1, C_2 and C_3: From the above analysis, when switch S is on, the capacitor voltages V_{C1} and V_{C2} are in series with the input voltage V_i to power the load R_L. However, because the sum of V_{C1}, V_{C2} and V_i is a little higher than the output voltage V_o, there will exist a small voltage ripple ΔV_C on the capacitors at the switching frequency. In order to limit ΔV_C to a small range, a permitted fluctuation range x_C% of capacitor voltage V_C is introduced here.

During the ON state of switch S, capacitors can be designed based on the following differential equation:

$$C = \frac{I_{C\_on}\mathrm{d}t}{\mathrm{d}v_C} \tag{25}$$

where I_{C_on} is the capacitor current when S is on; $\mathrm{d}t$=DT_s is the ON time of S, and $\mathrm{d}v_C$=x_C%V_C. Now $I_{C1\_on} = I_{in\_on} - I_{L1}$, $I_{C2\_on} = I_{L1} + I_{L2} - I_{in\_on}$, and $I_{C3\_on} = -I_{L1}$, so substituting these three equations into (25) leads to:

$$\begin{cases} C_1 = \dfrac{(D^2-D+1)I_o}{Dx_C\%V_i f_s} \\ C_2 = \dfrac{(1-2D)I_o}{x_C\%V_i f_s} \\ C_3 = \dfrac{(2-D)I_o}{x_C\%V_i f_s} \end{cases} \tag{26}$$

Therefore, the capacitance of C_1, C_2 and C_3 can be designed by (26) directly.

2) Output filter capacitor C_o: Similarly, when S is off, the output diode (D_o) will be reverse blocking. Therefore, the current flow through capacitor C_o will be equal to the output current I_o. Thus:

$$C_o = \frac{I_o \mathrm{d}t}{\Delta v_{Co}} = \frac{I_o \mathrm{d}t}{x_C\%V_o} \tag{27}$$

where $\mathrm{d}t$=$(1-D)T_s$. Substituting (3) into (27), the capacitance of capacitor C_o can be obtained as:

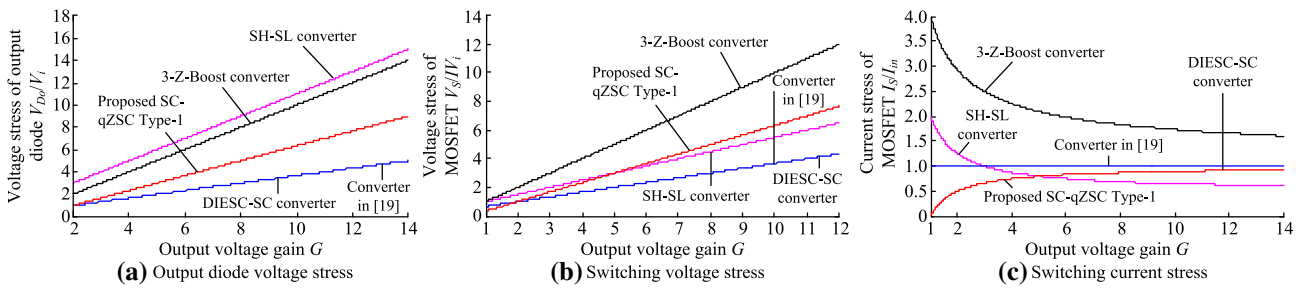


Fig. 8 Comparison results of the proposed SC-qZSC converter

$$C_o = \frac{(1-D)(1-2D)I_o}{(2-D)x_C\%V_i f_s} \tag{28}$$

4.5 Parameter selection of switching devices

Generally, the parameters of diodes and MOFETs can be selected according to their voltage and current stresses, which have been summarized in Table 1.

5 Comparison with other DC–DC converters

5.1 Comparison of output voltage gains

The output voltage gain of the proposed SC-qZSC Type-1 is plotted in Fig.7as a function of the duty ratio D, and compared with the3-Z-network boost converter in [6], the symmetrical hybrid switched-inductor converter (SH-SLC) in [16], the converter in [19] (the turns ratio of the coupled inductor is set to 1), the high step-up converter with double inductor energy storage cell based switched-capacitors (DIESC-SC converter) in [20], and the conventional ZSC in [30] (Table 2).

The ideal expressions for the output voltage gains are given in Table 3. And all these five converters are non-isolated DC–DC topologies. From Fig. 7, it can be observed that the output voltage gain of the proposed SC-qZSC Type-1 converter is higher than that of the other four converters for all duty ratios in the range (0, 0.5).

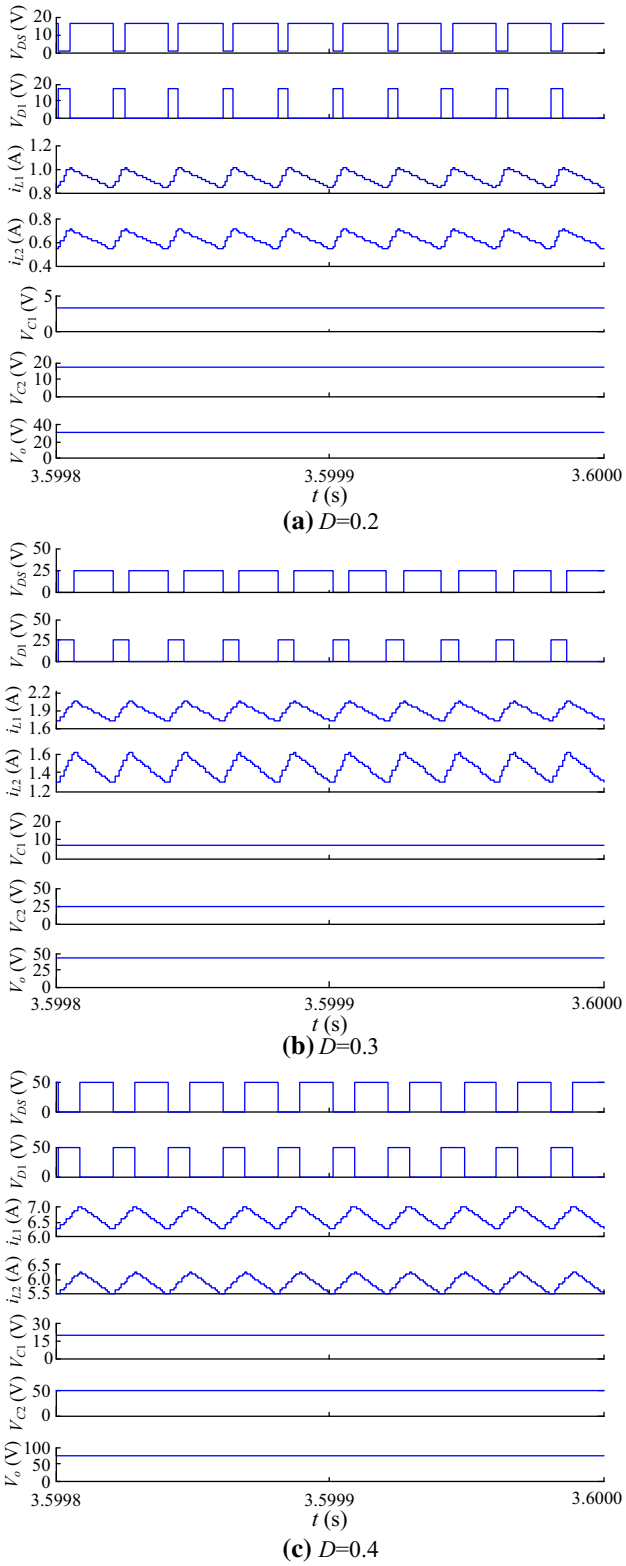
5.2 Comparison of the number of components

Table 2 shows the comparison of the number of passive and active components used in these five converters. From this table, it can be seen that the total number of components used in the proposed converter is no more than in the other four DC–DC converters. Therefore, compared with these four topologies, the proposed converter can provide higher output voltage gain by using the same or similar active and passive components.

5.3 Comparison of stresses

In this section, the voltage and current stresses of these five converters are compared under the same DC input voltage V_i, input current I_{in}, and output voltage gain G. The stresses on components of these five DC–DC topologies have been summarized and tabulated in Table 3.

The comparison of the output diode voltage stress for these five converters is depicted in Fig. 8a.It can be seen, for producing the same output voltage gain G, the proposed converter has lower output diode voltage stress than the SH-SLC converter and the 3-Z boost converter. Although it is a little higher than the DIESC-SC converter and converter in [19], it requires one less inductor and one less capacitor than DIESC-SC converter and one less diode



(a) D=0.2

(b) D=0.3

(c) D=0.4

Fig. 9 Simulation results

than the converter in [19]. Figure 8b shows the comparison of the switching voltage stress for these five topologies. It can be seen that the proposed converter has lower switching voltage stress than the 3-Z boost converter. However, when the output voltage gain G is larger than 5, it will be a little higher than the SH-SLC converter and the DIESC-SC converter. This is due to the proposed converter has higher boost ability. Fig. 8c shows the comparison of the switching current stress. It can be observed that the proposed converter only has a slightly higher switching current stress than DIESC-SC converter when G is larger than 5, but lower than the other three DC–DC converters.

6 Simulation results

The simulation parameters are selected according to the design conditions developed in Section 4: $V_i = 10$ V, $C_1 = C_2 = C_3 = 330$ μF, $L_1 = L_2 = 220$ μH, output filter capacitor $C_o = 330$ μF, switching frequency $f_s = 30$ kHz, rated output power $P_{out} = 64$ W and $R_L = 100$ Ω.

The simulation results are shown in Fig. 9. The three graphs each show, from top to bottom, the simulated waveforms for the drain-source voltage of switch S, the voltage of diode D_1 (or D_2), the currents in L_1 and L_2, the voltages of C_1 (or C_3) and C_2, and the output voltage V_o.

As shown in Fig. 9, the converter operates in CCM and includes two operating states. When the duty ratio is equal to 0.2, the capacitor voltages V_{C1} (or V_{C3}) is about 3.3 V and V_{C2} is about 16.67 V, and the output voltage V_o is about 30 V. When the duty ratio is 0.3, the capacitor voltageV_{C1} (or V_{C3}) is 7.5 V, V_{C2} is 25 V, and the output voltages is 42.5 V. When the duty ratio is 0.4, the capacitor voltage V_{C1} (or V_{C3}) is 20 V, V_{C2} are 50 V, and the output voltage is 80 V. Theseare all in accordance with the theoretical values calculated from (1), (2), and (3).

7 Experimental results

A prototype of the proposed SC-qZSC Type-1 converter was built to verify the steady state analysis in Section 3. The experimental parameters were chosen to match the simulation parameters given in Section 6.

The semiconductor switch S (Type:IRFP250N) is driven by the 2BB0108T basic board with driver 2SC0108T, and three MBRF30H150CTdiodes are used for D_1, D_2 and D_o. The ON resistance r_{DS} of switch S is 0.075 Ω.

The experimental waveforms of the proposed converter with a regulated DC input voltage source V_i=10 V, are shown in Fig. 10. From the top to the bottom, in each graph, the waveforms are the driven voltage of switch S, v_{GS}; the current of inductor L_1, i_{L1}; the current of inductor

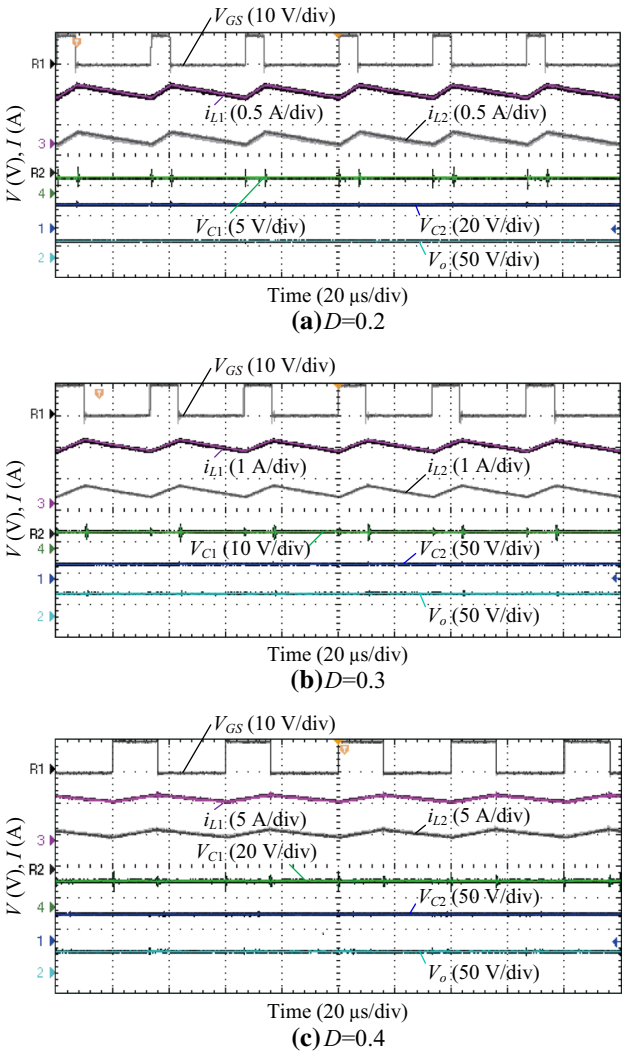


Fig. 10 Experimental waveforms with a regulated dc input voltage

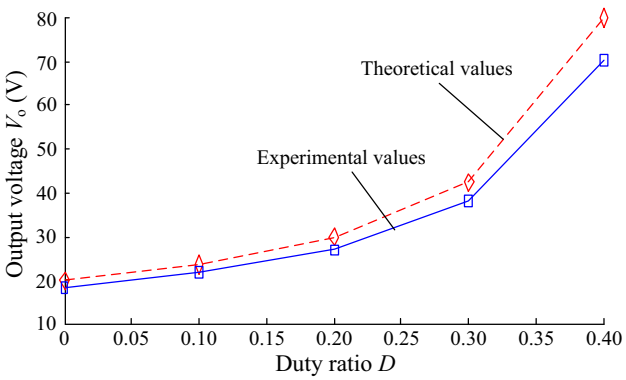


Fig. 11 Comparison between the experimental and theoretical values

L_2, i_{L2}; the capacitor voltages V_{C1} (or V_{C3}) and V_{C2}; and the output voltage V_o.

As shown in Fig. 10a, when the duty ratio $D = 0.2$, the measured values of capacitor voltages and output voltage are $V_{C1} = V_{C3} = 2.3$ V, $V_{C2} = 15.5$ V, and V_o=27.2 V,

while the theoretical values are $V_{C1} = V_{C3} = 3.3$ V, $V_{C2} = 16.67$ V, and V_o= 30 V. As shown in Fig. 10(b), when the duty ratio $D = 0.3$, the measured values of capacitor voltages and the output voltage are V_{C1}= $V_{C3} = 5.2$ V, $V_{C2} = 22.8$ V, and $V_o = 38.1$ V, while the expected values are $V_{C1} = V_{C3} = 7.5$ V, $V_{C2} = 25$ V, and $V_o = 42.5$ V. Fig. 10c shows the experimental waveforms when D=0.4, the measured values of capacitor voltages and the output voltage are $V_{C1} = V_{C3} = 16.8$ V, $V_{C2} = 45.1$ V, and V_o= 70.3 V, while the theoretical values are $V_{C1} = V_{C3} = 20$ V, $V_{C2} = 50$ V, and V_o= 80 V. The comparison between theoretical values and measured values is given in Fig. 11. It shows there are some differences between the measured values and theoretical values, which are mainly caused by the equivalent series resistance (ESR) of each component and the forward voltage drop of diodes.

In order to take the parasitic parameters of passive and active components into consideration, we assume that the forward voltage drops on diodes are V_D, the parasitic resistances of the inductors are r_L, the equivalent series resistances (ESRs) of capacitors are r_C, and the equivalent drain-to-source on-resistance of switch S is r_{DS}. Therefore, the relationship between the efficiency and the duty ratio of the proposed converter can be derived as:

$$\eta = \frac{2D(1-2D)(2-D) - (1+D)(t_r + t_f)f_s - 2D(1-2D)(4-5D)V_F/V_i}{2(2-D)\left[D(1-2D) + \frac{(1-D)(1+D)^2 r_{DS} + D(1-D)(5-2D+2D^2)r_L + Qr_C}{(1-D)(1-2D)R_L}\right]} \tag{29}$$

where $Q = (1 - D + D^2)^2 + (2D - D^2)^2 + (2 - 2D + D^2)(1 - 2D)^2$, t_r is the turn-on delay time, and t_f is the turn-off delay time. The detailed derivation of (29) is given in the Appendix.

The efficiency of the proposed converter under the condition of V_i=10 V, duty ratio D=0.2 ~ 0.4, R_L=100 Ω was measured, and a comparison between the measured and the theoretical predicted efficiencies is presented in Fig. 12. It can be seen that by increasing the value of the duty cycle the measured efficiency of the proposed converter is reduced, and the difference between the calculated and experimental results is increased. The reason is that by increasing the duty cycle the conduction power losses on devices will be increased, too. This fact applies to all kinds of converters based on impedance source network.

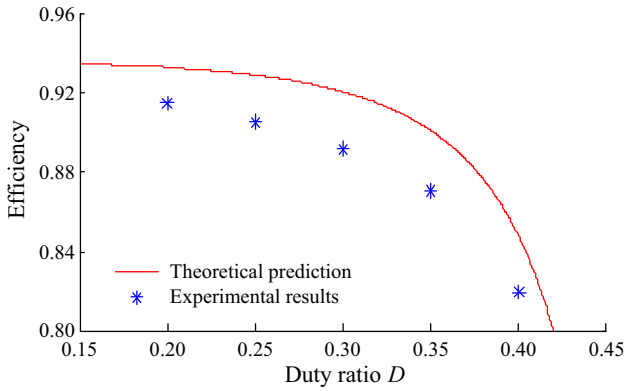


Fig. 12 Comparison between the experimental and the expected efficiencies

8 Conclusion

Based on the respective merits of the switched -capacitor converter and the quasi-Z-source converter, anew high step-up quasi-Z-source DC–DC converter with a single switched-capacitor branch was proposed in this paper. The operating principle analysis, parameter selection, the boundary condition between continuous and discontinuous conduction mode (CCM and DCM), and the comparison with other existed high step-up DC–DC converters have been presented in detail. Finally, both the simulations and experimental results are given to validate the effectiveness of the proposed converter. In comparison with other existed high step-up DC–DC converters, the proposed converter provides higher output voltage gain, lower voltage stress across the output diodes, and lower current stress across the switches. Thus, the efficiency and reliability of the proposed converter can be improved, which implies that it would be suitable for high step-up voltage conversion applications, such as TV-CRTs, X-ray systems, high intensity discharge lamps for automobile headlamps, as well as grid connection of renewable energy sources.

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Appendix A

This Appendix shows the detailed derivation of the relationship between the efficiency and the duty ratio of the proposed converter given in equation (29).To simplify the calculation, we assume that inductors L_1, L_2 have the same parasitic resistance r_L, capacitors C_1, C_2, C_3 and C_o have the same ESR r_C, and diodes D_1, D_2 and D_o have the same

Table 3 Stress comparison in the same V_i, I_{in}, and G

Topologies	Symmetrical hybrid-SL converter	DIESC-SC converter	Converter in [19]	3-Z-Boost	Proposed SC-qZSC (Type 1)
Voltage gain	$\frac{1+3D}{1-D}$	$\frac{2+D}{1-D}$	$\frac{2+D}{1-D}$	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{2-D}{1-2D}$
Voltage stress of switches	$(1+G)V_i/2$	$(G+1)V_i/3$	$(G+1)V_i/3$	GV_i	$(2G-1)V_i/3$
Current stress of switches	$\frac{G+3}{2G}I_{in}$	$\frac{G-1}{G}I_{in}$	I_{in}	$\frac{G+2\sqrt{G}+1}{G}I_{in}$	$\frac{G-1}{G}I_{in}$
Voltage of output diodes	$(1+G)V_i$	$(G+1)V_i/3$	$(G+1)V_i/3$	GV_i	$(2G-1)V_i/3$
Voltage of other diodes	$(G-1)V_i/4$	$(G+1)V_i/3$	$(G+1)V_i/3$	$(\sqrt{G}-1)V_i/2$	$(2G-1)V_i/3$
				$(G-\sqrt{G})V_i/2$	
	V_i			$\sqrt{G}V_i$ V_i	
				$(G-\sqrt{G})V_i$	
Inductor current	$\frac{G+3}{4G}I_{in}$	I_{in}	I_{in}	$(G+\sqrt{G})I_{in}/2$	$(G-1)I_{in}/G$
		I_{in}/G		$(1+\sqrt{G})I_{in}/2$	

forward voltage drop V_D. The converter losses, and the voltage and current waveforms are assumed to be piece-wise linear segment. Then, the derivation of (29) proceeds as follows.

1) Active switch conduction loss

$$P_{r_{DS}} = I^2_{S_{(RMS)}} r_{DS} = \frac{(1+D)^2}{D(1-2D)^2}\frac{P_o}{R_L} r_{DS} \tag{A1}$$

2) Active switch switching loss

$$\begin{aligned} P_{sw} &= \frac{1}{2} V_{off\_state} I_{on\_state} \left(t_r + t_f\right) f_s \\ &= \frac{(1+D)\left(t_r + t_f\right) f_s V_{in}}{2D(1-2D)^2}\frac{P_o}{V_o} \end{aligned} \tag{A2}$$

3) Diode conduction losses

$$P_{V_F} = V_F I_D = \frac{4-5D}{1-2D}\frac{P_o}{V_o} V_F \tag{A3}$$

4) Inductor conduction losses

$$P_{r_L} = I^2_{L_{(RMS)}} r_L = \frac{(2-D)^2+(1+D)^2}{(1-2D)^2}\frac{P_o}{R_L} r_L \tag{A4}$$

5) Capacitor conduction losses

$$\begin{aligned} P_{r_C} &= I^2_{C_{(RMS)}} r_C \\ &= \frac{(1-D+D^2)^2+(2D-D^2)^2+(2-2D+D^2)(1-2D)^2}{D(1-D)(1-2D)^2}\frac{P_o}{R_L} r_C \end{aligned} \tag{A5}$$

Based on (A1)-(A5), the total power losses can be obtained as:

$$P_{losses} = P_{r_{DS}} + P_{sw} + P_{V_D} + P_{r_L} + P_{r_C} \tag{A6}$$

Therefore, the efficiency of the proposed converter can be derived as:

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_o + P_{losses}} = \frac{1}{1 + P_{losses}/P_o} \tag{A7}$$

Substituting (A1), (A2), (A3), (A4) and (A5) into (A7), one can obtain

$$\eta = \frac{2D(1-2D)(2-D) - (1+D)\left(t_r + t_f\right) f_s - 2D(1-2D)(4-5D)V_F/V_i}{2(2-D)\left[D(1-2D) + \frac{(1-D)(1+D)^2 r_{DS} + D(1-D)(5-2D+2D^2) r_L + Q r_C}{(1-D)(1-2D) R_L}\right]} \tag{A8}$$

where $Q = (1-D+D^2)^2 + (2D-D^2)^2 + (2-2D+D^2)(1-2D)^2$; t_r is the turn-on delay time; t_f is the turn-off delay time. Therefore, (A8) is the same as (29).

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