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Fault ride-through of renewable energy conversion systems during voltage recovery

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Abstract Asymmetrical voltage swells during recovery of a short-circuit fault lead to fluctuations in the dc-link voltage of a renewable energy conversion system (RECS), and may induce reversed power flow and even trip the RECS. This paper studies characteristics of both typical causes resulting in the practical asymmetrical voltage swell and the voltage at the point of common coupling (PCC) during the fault recovery. As analyzed, the fault recovery process can be divided into two continuous periods in which different control strategies have to be applied. Also protective measures are necessary in the transient period of the process. Additionally, the asymmetrical high-voltage ride-through capability and the controllability criteria of the RECS are analyzed based on eliminating the fluctuations. Furthermore, an asymmetrical control scheme is proposed to maintain the controllability of the RECS and ride through the entire recovery process. As verified by the simulation, the scheme can promise the RECS to deal with the practical fault recovery period and mitigate the dc-link voltage fluctuations, which improves the reliability of the RECS and the power system.

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1 Introduction

In recent years, renewable energy conversion systems (RECSs), an important part of power system, develop rapidly all over the world. Unfortunately, RECSs present quite different characteristics from conventional synchronous generators (SGs). By employing grid connected power inverters, RECSs can provide much faster power response than SGs. Besides, the inverter-coupled RECS has limited fault tolerant capability during grid disturbance, such as voltage sags or swells [1].

To avoid the power system stability issue being influenced by the integrated large-scale RECS, independent system operators (ISOs) require the RECS to operate abiding by strict grid codes. One of important requirements in the grid codes is the low-voltage ride-through (LVRT) capability which demands the RECS to stay on-grid and supply the expected reactive current to support the utility during grid faults. Generally, the LVRT code defines steady and dynamic performances of the RECS in three continuous periods after the grid fault occurred, including fault transient, fault continuous, and fault recovery periods [2]. The LVRT capability and strategies of the RECS during the first two periods have been thoroughly studied in many previous literature [3, 4]. In the fault recovery period, the RECS is required to recover active power output in a defined rate. This is possible, for the simple reason that the power response of the inverter-coupled RECS can be fast enough to satisfy the requirements. Unfortunately, voltage swells always occur during the voltage recovery period, which may cause shutdown of the RECS and result in

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failure of the fault ride through [5, 6]. Thus, the swells bring challenges to the RECS in terms of control capability and schemes. Taking wind power plant as an example, a large number of wind turbines tripped for dozens of times during the fault recovery period due to the voltage swells in Northwest wind farms of China in 2011 [7].

In order to avoid the tripping of the RECS during voltage swells, some ISOs, such as Scotland, Australia, Spain, and Western Electricity Coordinating Council (WECC), also released high-voltage ride-through (HVRT) requirements in which the RECS should keep connected with the grid when voltage swells occur, as shown in Fig. 1 [8, 9]. Taking Australia code as an example, the guideline requires wind turbines to stay connected for 60 ms when the PCC voltage soars to 1.3 pu.

It is noticed that the HVRT codes are defined for the voltage swells in steady state and they only address the symmetrical situations. Voltage swells can occur due to the removal of large loads, shunt capacitor energization and so on [10–12]. Unfortunately, the loads are unbalanced in general [13], and switching operations of circuit breakers in the transmission lines and the shunt capacitors are not synchronous either [14]. Thus, voltage swells during the practical fault recovery change with transients and unbalances. Such phenomena largely increase the ride-through difficulties in the RECS.

In normal situations, the grid connected inverter of the RECS modulates its output voltage so that active and reactive currents between the inverter and the grid can be regulated. By doing this, dc-link voltage of the inverter is remained and reactive power can be distributed arbitrarily [15]. Voltage swells will induce current surge to the inverter, resulting in dc-link overvoltage and even tripping the inverter [16]. Moreover, since the output voltage of the inverter is limited by the dc-link voltage, the output current will run out of control when the voltage swell is high [17]. With consideration of transients and unbalance, the situation could be worse. Apart from the overvoltage issue,

fluctuations in the dc-link voltage and influence of the controller delay lead to power quality issue and even tripping of the inverters.

Different strategies can deal with voltage swells during the fault recovery period for the RECS. Generally, they can be classified into two categories. One is hardware based scheme which needs additional facilities. The other is software based scheme which focuses on advanced control techniques. Doubly fed induction generator (DFIG)-based RECSs are not discussed in this paper.

Crowbar circuit is popular and has been equipped in the commercial RECS [18–20]. It can dissipate excessive power during voltage swells to avoid dc-link overvoltage of the inverters. Improved topology of the crowbar circuit can provide more effective control performance [16]. In order to avoid power losses, superconducting magnetic energy storage unit (SMES) can be integrated with the crowbar circuit [21]. Other facilities, such as static synchronous compensators (STATCOM) and dynamic voltage restorers (DVR), are also applicable. Such facilities can actively mitigate the voltage swell at the point of common coupling (PCC) of the RECS by injecting reactive current or series voltage [22–24]. The hardware based scheme leads to extra costs.

Software based scheme tries to improve the fault ride-through capability of the RECS by redesign control schemes of the inverters. In [25], the over-modulation technique is applied to expand the output voltage range of the inverter to avoid the dc-link overvoltage. However, the effectiveness of such scheme is limited. The variable-band hysteresis can provide quick transient response to enhance the fault ride-through capability of the inverter [26, 27]. The performance of this controller is affected by low-order current harmonic distortions and variable switching frequency. The reactive current control can reduce the PCC overvoltage [28–30]. However, this strategy cannot deal with severe voltage swells because of the current rating. Furthermore, flexible advanced algorithms are proposed to deal with dc-link voltage fluctuation caused by severe symmetrical voltage swells [17, 31].

The above previous studies ignore typical voltage dynamics at the PCC during the fault recovery period. Besides, asymmetrical HVRT capability and control strategy of the RECS during the recovery period have not been studied.

This paper analyzed the asymmetrical HVRT capability and proposed a scheme for the RECS during fault recovery period. As presented in this paper, typical voltage swells during the recovery period have limited voltage unbalance, phase angle jump and discrete transients. Based on characteristics of the voltage at PCC, the fault recovery process can be divided into two periods: transient period and continuous period. In the continuous period, sequence
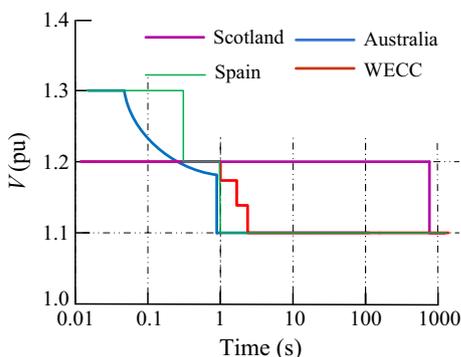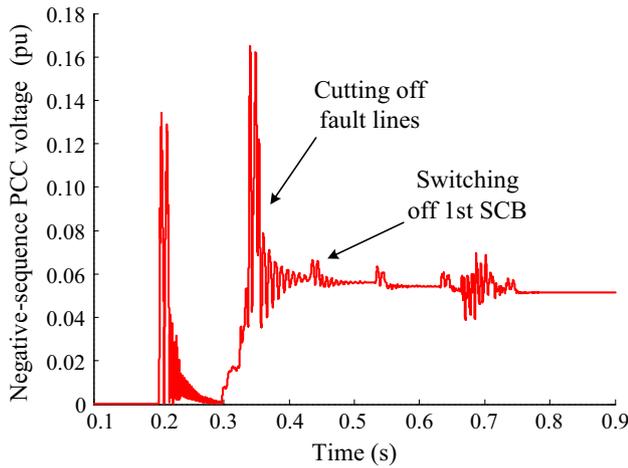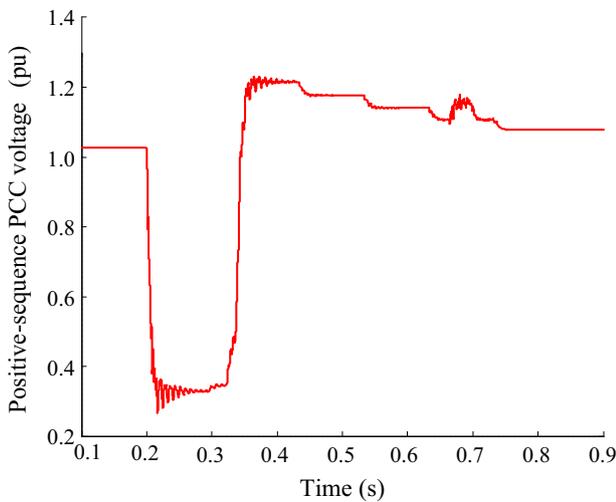

Fig. 1 HVRT grid codes for wind farms integrated into the utility grid

voltages at PCC keep comparatively stable and their maximum amplitude is less than 1.3 pu. A controllability criteria of the RECS is analyzed from the perspective of the asymmetrical PCC overvoltage, and its control capability is also evaluated during the fault recovery. Further, different control schemes are designed for different voltage periods. In the transient period, sharp dc-link overvoltage due to voltage transients is dealt with. In the continuous period, the output current and the dc-link voltage are controlled according to the height of the asymmetrical overvoltage, in order to keep the RECS under control and satisfy the grid codes.

2 Characteristics of PCC voltage during fault recovery

This section aims to study characteristics of typical causes resulting in practical asymmetrical voltage swells at PCC and characteristics of the voltage at PCC during fault recovery. Meanwhile, a typical power system integrated with a RECS is modeled to study the maximum amplitude and sequence components of PCC voltage. The diagram of the power system is shown in Fig. 2.

2.1 Typical causes resulting in asymmetrical voltage swells at PCC during fault recovery

Overvoltage at PCC during the fault recovery is related to typical operations of the RECS to clean the short-circuit fault, which are presented as follows.

2.1.1 Cutting off large loads

According to the grid codes, RECSs should not only support long-term operations under the grid voltage of 1.1 pu but also withstand grid voltage's unbalance no more than 5% for minutes to adapt change of loads [8, 32]. Since this paper is not focused on load modeling, the effect of load shedding can be equivalent to uprush of the grid voltage, and the worst situation can be regarded as the upper bound in the codes.

2.1.2 Switching shunt capacitor banks (SCBs)

According to technical regulations of the ISO in China, capacity of the SCBs can be set as 25% to 50% of the total capacity of the RECS [33, 34]. And the SCBs always contain 2 to 4 banks. Circuit breakers (CB) of the SCBs are controlled to open and close at the optimum angle of current or voltage [14]. Moreover, switching-off of a bank has to be followed with an interval before the next switching-off to prevent switching the SCBs frequently. To shorten simulation time, the interval is set to 100 ms in this paper.

2.1.3 Reclosing transmission lines

Reclosing fault transmission lines is singly operated in each phase, since the RECS is generally integrated into a voltage network (110 kV or above) [14].

2.1.4 Changing taps of main transformers

The main transformer of the RECS is an on-load tap changing transformer, which takes a long time to adjust the transformation ratio slightly [34]. Therefore, this operation is not taken into account.

2.1.5 Severest voltage swells at PCC

The severest voltage swells at PCC may result from three-phase short-circuit faults where the typical operations overlap. Representative order and duration of the operations after the faults occur are presented by a Gantt chart, as shown in Fig. 3. If the grid voltage soars to 1.05 pu positive-sequence voltage and 0.05 pu negative-sequence voltage due to the removal of unbalanced loads, the sequence voltages at PCC are illustrated in Fig. 4.

As denoted in Fig. 4, the positive-sequence PCC voltage is less than 1.3 pu, and the negative-sequence PCC voltage is less than 0.18 pu. Practical characteristics of the PCC voltage are studied in the subsection.

Fig. 2 Typical diagram of the power system integrated with a RECS

Fig. 3 Representative order and duration of the operations after fault

(a) Negative-sequence voltage

(b) Positive-sequence voltage

Fig. 4 Negative- and positive-sequence voltages at PCC after short-circuit fault

2.2 Characteristic analysis of PCC voltage during fault recovery

To formulate the maximum amplitude and sequence components of PCC overvoltage during the fault recovery, the system shown in Fig. 2 can be simplified as the voltage divider model in Fig. 5. If the RECS cannot provide the current to support the grid recovery, the analyzed PCC overvoltage would be the severest. Therefore, the RECS is neglected in the model.

In the model, $\dot{U}_{grid,x}$ is the grid voltage, and $\dot{U}_{g,x}$ is the voltage at PCC. Z_L is the impedance of the transmission lines. $Z_{RE,x}$ is the impedance between the PCC and the ground. In these phases that are still during the short-circuit fault, $Z_{RE,x}$ is the short-circuit impedance defined as $Z_{f,x}$. In these phases where the fault line is cut off, $Z_{RE,x}$ is the impedance of the SCBs defined as $Z_{c,x} \cdot x = a, b, c$.
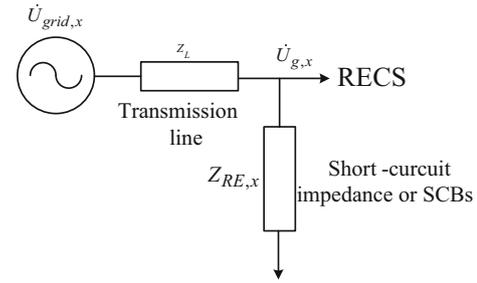
Fig. 5 Voltage divider model of the power system integrated with a RECS

$Z_{f,x}$ can be expressed as [2]:

$$Z_{f,x} = \lambda e^{i\alpha} Z_L \tag{1}$$

where λ indicates the relative fault distance depending on the fault location; α is a impedance angle containing: $0°$ for transmission systems, $-20°$ for distribution systems, and $-60°$ for offshore wind farms.

2.2.1 Characteristics of PCC overvoltage caused by cutting off fault lines

Based on this model, the voltage at PCC can be defined as follows:

$$\dot{U}_{g,x} = \frac{Z_{RE,x}}{Z_L + Z_{RE,x}} \cdot \dot{U}_{grid,x} \tag{2}$$

Supposed that the CB in phase B opens first. Then the sequence PCC voltages can be expressed as:

$$\begin{bmatrix} \dot{U}_{g+} \\ \dot{U}_{g-} \\ \dot{U}_{g0} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \dot{U}_{g,a} \\ \dot{U}_{g,b} \\ \dot{U}_{g,c} \end{bmatrix} \tag{3}$$

where $a = e^{i120°}$; $\dot{U}_{g+}$, $\dot{U}_{g-}$, and $\dot{U}_{g0}$ are the positive-, negative- and zero-sequence voltages at PCC. The zero-sequence voltage is neglected, since it is isolated by the Y/Δ configured transformers. The positive- and negative-sequence voltages can be calculated from (3):

$$\dot{U}_{g+} = \left(\frac{3 - 2\omega^2 L_L C_x}{1 - \omega^2 L_L C_x} - \frac{2}{1 + \lambda e^{i\alpha}} \right) \frac{\dot{U}_{grid}}{3} \tag{4}$$

$$\dot{U}_{g-} = \left(\frac{\omega^2 L_L C_x}{1 - \omega^2 L_L C_x} + \frac{1}{1 + \lambda e^{i\alpha}} \right) \frac{\dot{U}_{grid}}{3} \cdot e^{i120°} \tag{5}$$

where C_x is the capacitance of all the SCBs; L_L is the inductance of Z_L.

Suppose that the CB in phase C trips then. The sequence PCC voltages can be shown in Fig. 6 under $\alpha = -20°$.

As denoted in Fig. 6, the positive-sequence voltage increases fast during cutting off fault lines; the magnitude of the negative-sequence voltage is large; and the phase-
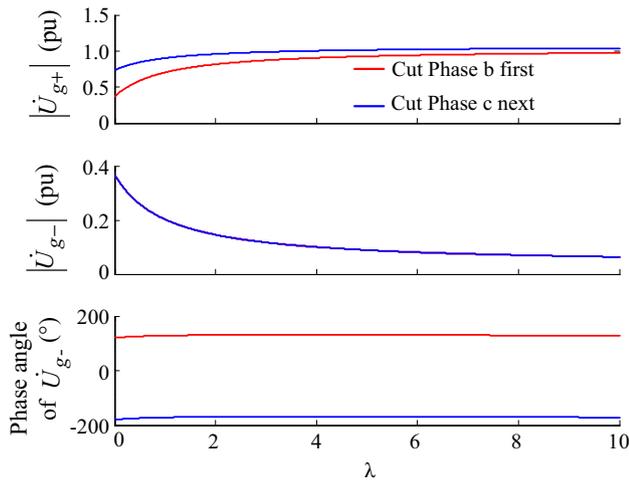
Fig. 6 Positive- and negative-sequence PCC voltages during cutting off fault lines

angle jumps with breakers tripping three times in a cycle of the grid voltage. It should be noticed that single-phase transient overvoltage may appear at PCC, since the SCBs are charged by the residual transmission line current if the CBs of the transmission lines do not operate at the current zero-crossing.

2.2.2 Characteristics of PCC overvoltage caused by SCBs

Characteristics of the PCC overvoltage caused by the SCBs can be discussed by means of the proposed analysis method and the model shown in Fig. 5. After the PCC voltage recovers, switching SCBs out of synchrony gives rise to asymmetrical overvoltage. Besides, the overvoltage at PCC is severest when just a single-phase capacitor of the first SCB is cut off.

Supposed that the capacitor in phase B is turned off first. Based on (2) and (3), the sequence voltages at PCC can be obtained:
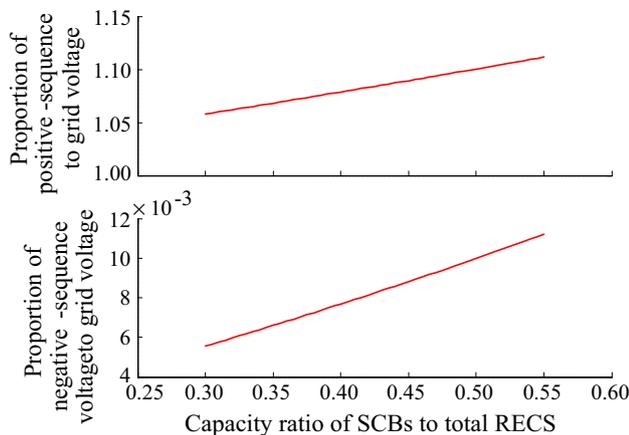
Fig. 7 Proportion of sequence PCC voltages to the grid voltage under different capacity ratios of SCBs to the total RECS
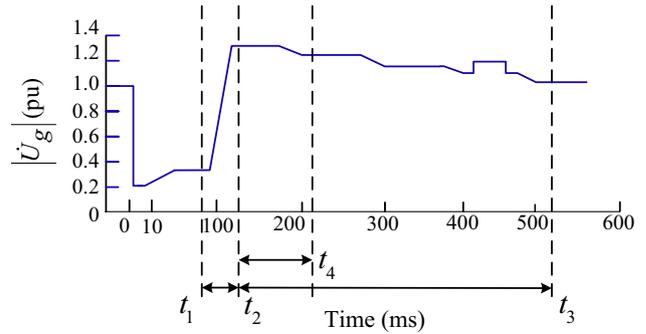
Fig. 8 Division of fault recovery process at PCC

$$\dot{U}_{g+} = \frac{12 - 10\omega^2 L_L C_x}{(1 - \omega^2 L C_x)(4 - 3\omega^2 L_L C_x)} \frac{\dot{U}_{grid}}{3}$$

$$\dot{U}_{g-} = \frac{\omega^2 L_L C_x}{(1 - \omega^2 L_L C_x)(4 - 3\omega^2 L_L C_x)} \frac{\dot{U}_{grid}}{3} e^{-i60°} \quad (6)$$

The proportion of sequence PCC voltages to the grid voltage can be illustrated in Fig. 7 under different capacity ratios of the SCBs to the RECS. The horizontal axis is the capacity ratio of the SCBs to the total RECS; the vertical axis is the proportion of the sequence PCC voltages to the grid voltage.

The sequence PCC voltages can be calculated similarly, when the CBs of the first SCB act then in other phases. And it can be found that there is no phase angle jump, and the sequence voltage magnitudes keep comparatively stable.

According to Fig. 7, the positive- and negative-sequence PCC voltages come up to 1.221 pu and 0.01 pu respectively, when the capacity ratio of the SCBs to the entire RECS is 50% and the grid voltage jumps to 1.1 pu due to the removal of loads. Moreover, the grid codes require that RECSs can withstand the grid voltage's unbalance no more than 5%. Therefore, the maximum amplitude of the negative-sequence voltage at PCC approaches 0.06 pu in this period.
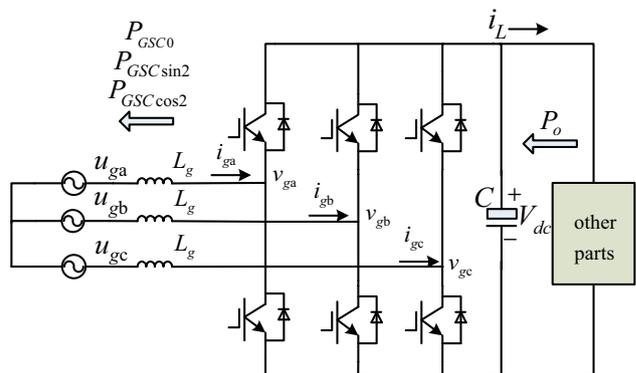

Fig. 9 Typical model of RECSs

2.3 Division of fault recovery period at PCC

The fault recovery process can be divided into two periods based on the analyzed characteristics of the PCC voltage, as shown in Fig. 8.

2.3.1 Transient period (t_1–t_2)

In this period, protective measures are necessary to help the RECS regain the controllability. The positive- and negative-sequence PCC voltages change rapidly. The dc-link overvoltage may result from the limited detection speed of the PLL and the single-phase transient overvoltage. However, the requirement of this period has not been stipulated.

2.3.2 Continuous period (t_2–t_3)

The relatively stable asymmetrical overvoltage appears at PCC. The positive- and negative-sequence voltages are less than 1.3 pu and 0.07 pu respectively. Thus, the maximum operated PCC voltage of 1.3 pu is reasonable required by the codes. According to the grid codes, the RECS must be under control and provide expected reactive current. The asymmetrical HVRT capacity of the RECS has to be analyzed in this period.

3 Analysis of RECS's control objective in continuous period of fault recovery

The control objective of the RECS in the continuous period is discussed in the following when the PCC voltage soars asymmetrically. The RECS has been aggregated as a single unit shown in Fig. 9, since the voltage swell just continues a short period. Other parts of the RECS except the inverter are replaced by an equivalent power source.

In this model, L_g is the grid-connected inductance, and $i_{g,x}$ is the input current of the inverter. $v_{g,x}$ is the output voltage of the inverter, V_{dc} is the dc-link voltage. P_o is the input power. P_{GSC0} is the fundamental output active power. $P_{GSC\sin 2}$ and $P_{GSC\cos 2}$ are the double- frequency output active power. The load current is defined as i_L. The voltage relationship of the inverter can be expressed as:

$$\begin{cases} \dot{U}^+_{gdq+} = j\omega L_g \dot{I}^+_{gdq+} + \dot{V}^+_{gdq+} + \dfrac{L_g d\dot{I}^+_{gdq+}}{dt} \\ \dot{U}^-_{gdq-} = -j\omega L_g \dot{I}^-_{gdq-} + \dot{V}^-_{gdq-} + \dfrac{L_g d\dot{I}^-_{gdq-}}{dt} \end{cases} \tag{7}$$

where the superscripts "+" and "−" indicate the positive- and negative-sequence components; the subscript "$dq+$"

and "$dq-$" indicate the reference frames rotating at ω and $-\omega$; $\dot{U}_g$ and $\dot{I}_g$ denote the space vector of the PCC voltage and the input current respectively; $\dot{V}_g$ is the needed output voltage of the RECS.

Fluctuations on the dc-link voltage are existed due to double-frequency ripples of the active power on the gird-tied inductor and the power outputted by the inverter, which is discussed by [35] in detail. The fluctuations may cause harmonics in the output current, the over- or under-voltage protection, and even tripping of the RECS. Nevertheless, the negative-sequence PCC voltage is small in the continuous period. Therefore, the control objective can be set to eliminate the fluctuations.

To achieve the elimination, the negative-sequence output current can be presented with the following space vectors:

$$i^-_{d-} + j i^-_{q-} = \dot{L}_0 + \dot{L}_1 \tag{8}$$

$$\dot{L}_0 = -j\left[2\omega L_g(i^{+2}_{d+} + i^{+2}_{q+}) - u^+_{gd+} i^+_{q+} \right] \frac{\dot{U}^-_{gdq-}}{k} \tag{9}$$

$$\dot{L}_1 = -u^+_{gd+} i^+_{d+} \frac{\dot{U}^-_{gdq-}}{k} \tag{10}$$

where $k = (u^+_{gd+} + 2\omega L_g i^+_{q+})^2 + 4\omega^2 L_g^2 i^{+2}_{d+}$; $\dot{L}_1$ is parallel to $\dot{U}^-_{gdq-}$, and $\dot{L}_0$ is perpendicular to $\dot{U}^-_{gdq-}$. Further, the voltage space vector relationship of the inverter shown in Fig. 10 can be deduced from (7)–(10):

$$\dot{U}^+_{gdq+} + \dot{U}^-_{gdq-}e^{j\theta} = \dot{V}_{gdq} + j\omega L_g \dot{I}^+_{gdq+} - j\omega L_g(\dot{L}_0 + \dot{L}_1)e^{j\theta} \tag{11}$$

where θ is the angle between $\dot{U}^+_{gdq+}$ and $\dot{U}^-_{gdq-}$.

Derived from Fig. 10, $|\dot{V}_{gdq}|$ reaches the maximum defined as $|\dot{V}_{gdq}|_{\max}$, when θ is around 0°. According to the inverter's characteristics, $|\dot{V}_{gdq}|_{\max}$ has to be less than V_{dc}/m, if the RECS maintains its controllability and the control objective can be achieved. m is the modulation index, for SVPWM, $m = \sqrt{3}$.

4 Control capability of RECS in continuous period of fault recovery

This section aims to study control capability of the RECS under the asymmetrical PCC overvoltage in the continuous period. The analysis can be employed as the guideline of new grid codes and control strategy design.

The inverter of the RECS is limited by output voltage and current ratings. Besides, the RECS has to support the positive-sequence inductive current, which is less than zero
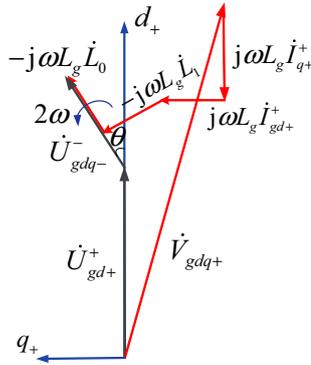
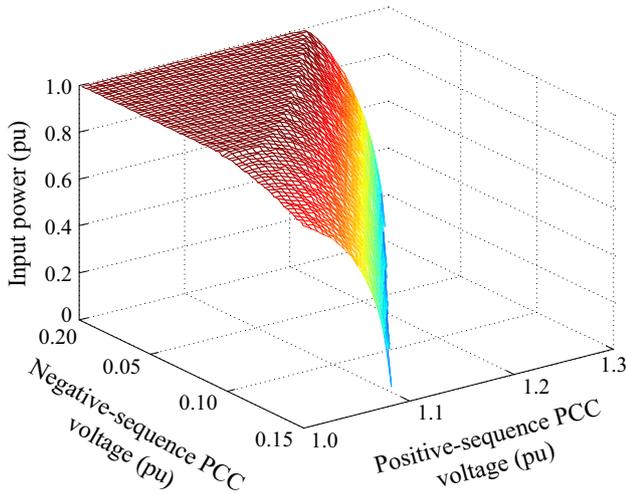Fig. 10 Voltage space vector diagram of the inverter

Fig. 12 Maximum HVRT capability of RECS when input power is zero

Fig. 11 Asymmetrical HVRT capability of RECS when $V_{dc} = 1.1$ pu
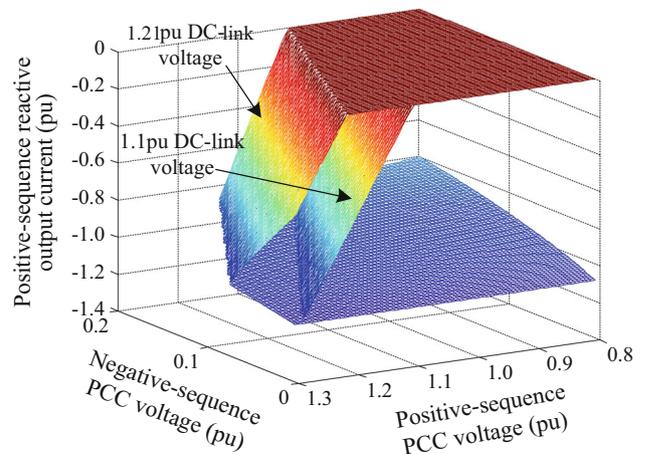
Fig. 13 Positive-sequence inductive current range supplied by RECS

Table 1 Parameter of a single unit in the RECS

Parameter	Value
Nominal power	1.5 MW
Nominal line voltage	575 V
DC-link rated voltage	900 V
Grid-connected inductance	0.1 mH

in the model shown in Fig. 9. The ratings can be expressed as:

$$\left| \dot{I}_{gdq+}^{+} \right| + \left| \dot{I}_{gdq-}^{-} \right| \leq I_{g\max} \tag{12}$$

$$\left| \dot{V}_{gdq} \right|_{\max} \leq V_{dc}/m \tag{13}$$

$$i_{gq+}^{+} \leq 0 \tag{14}$$

where $I_{g\max}$ is the maximum output current. It is generally 1.1 times of the rated inverter current.

In practice, only i_{q+}^{+} can be regulated to assist the RECS to ride through the asymmetrical overvoltage. i_{d+}^{+} is determined by the dc-link voltage through a PI controller. i_{d-}^{-} and i_{q-}^{-} have to satisfy (8)–(10) in order to eliminate the dc-link voltage fluctuations.

In terms of symmetrical voltage swells, the needed output voltage of the RECS decreases clearly, when the voltage on the inductor increases which is generated by more inductive output current [9]. However, under the asymmetrical conditions, the relationship between $\dot{V}_{gdq}|_{\max}$ and i_{q+}^{+} becomes vague, since the inductor voltage is influenced by not only i_{q+}^{+} but also the negative-sequence output current. The subsection aims to study the relationship and find a critical factor determining the RECS's controllability.
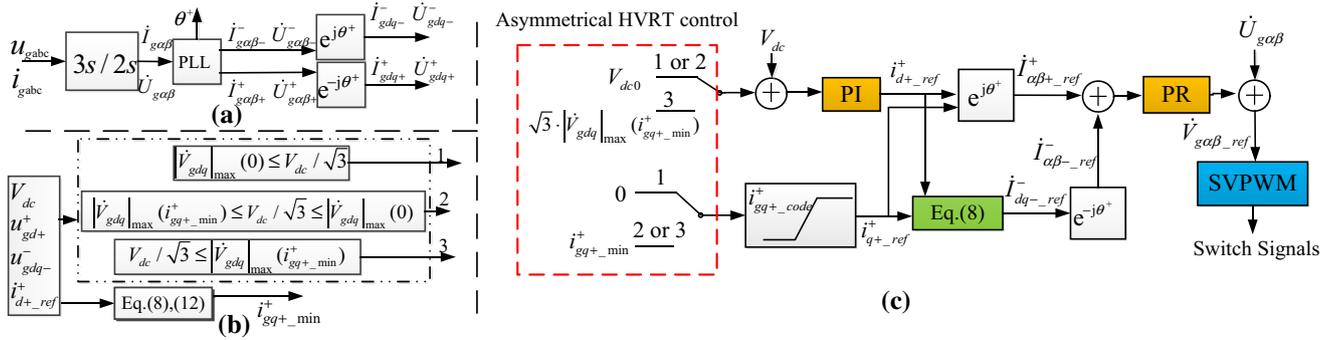
Fig. 14 Control diagram of the RECS with asymmetrical voltage swell

4.1 Relationship between maximum needed output voltage and positive-sequence output reactive current

In the practical RECS, P_0 can be regarded as a constant value during the fault recovery. Then, $\left|\dot{V}_{gdq}\right|_{\max}$ is just related to i_{q+}^+, when the sequence PCC voltages are given. Therefore, $\left|\dot{V}_{gdq}\right|_{\max}$ can be further expressed as $\left|\dot{V}_{gdq}\right|_{\max}(i_{q+}^+)$.

Under the asymmetrical PCC overvoltage, P_0 should satisfy the following expression [8]:

$$P_{GSC0} = -\frac{3}{2}\left(u_{gd+}^+ i_{gd+}^+ + u_{gd-}^- i_{gd-}^- + u_{gq-}^- i_{gq-}^-\right) \quad (15)$$

Therefore, i_{d+}^+ is coupled to i_{q+}^+ in this situation, and the coupling effect can be expressed as:

$$\frac{\mathrm{d}i_{gd+}^+}{\mathrm{d}i_{gq+}^+} = \frac{-4\omega L_g i_{gd+}^+ \left|\dot{U}_{gdq-}^-\right|^2}{\left(u_{gd+}^+ + 2\omega L_g i_{q+}^+\right)^2 - \left|\dot{U}_{gdq-}^-\right|^2}$$
$$\cdot \frac{1}{\left(u_{gd+}^+ + 2\omega L_g i_{q+}^+\right)} > 0 \quad (16)$$

According to Fig. 10, $\left|\dot{V}_{gdq}\right|_{\max}(i_{q+}^+)$ is mainly determined by its component on d-axle which can be defined as v_{gd}. Further, the partial derivatives of v_{gd} with i_{d+}^+ and i_{q+}^+ are greater than zero calculated from Fig. 10. The correlation between $\left|\dot{V}_{gdq}\right|_{\max}(i_{q+}^+)$ and i_{q+}^+ can be deduced:

$$\frac{\mathrm{d}\left|\dot{V}_{gdq}\right|_{\max}(i_{q+}^+)}{\mathrm{d}i_{gq+}^+} \approx \frac{\mathrm{d}v_{gd}}{\mathrm{d}i_{gq+}^+} = \frac{\partial v_{gd}}{\partial i_{gd+}^+}\frac{\mathrm{d}i_{gd+}^+}{\mathrm{d}i_{gq+}^+} + \frac{\partial v_{gd}}{\partial i_{gq+}^+} > 0 \quad (17)$$

Derived from (17), i_{q+}^+ is positively correlated to $\left|\dot{V}_{gdq}\right|_{\max}(i_{q+}^+)$ under the constant input power and PCC voltage. That means: $\left|\dot{V}_{gdq}\right|_{\max}$ decreases, when more positive-sequence inductive current is outputted under asymmetrical overvoltage. This is similar to the

conclusion under the symmetrical voltage swells. Therefore, the controllability of the RECS would be determined by the inductor voltage, which is generated by the maximum positive-sequence inductive current within the current ratings.

4.2 Asymmetrical HVRT capability of RECS

According to the above analysis, the controllability criteria of the RECS in the continuous period can be expressed as:

$$\left|\dot{V}_{gdq}\right|_{\max}(i_{q+\_\min}^+) \le V_{dc}/m \quad (18)$$

where $i_{q+\_\min}^+$ corresponds to the maximum positive-sequence inductive output current. Substituting (10)–(12) into (14), $i_{q+\_\min}^+$ can be simply solved with an iterative solution by a computer.

Further, the asymmetrical HVRT capability of the RECS can be analyzed under the different input power and sequence PCC voltages based on the criteria. As a result, the capability can be described as a nonlinear optimization problem. The equality and inequality constraints include (8)–(11), (12), and (18). The objective function can be expressed as:

$$P_{0\_\max} = \max\{P_0\} \quad (19)$$

Taking the sequence PCC voltages as variables, the maximum input power are illustrated in Fig. 11. The parameters in this study are given in Table 1.

The capability reaches the maximum scope, when the input power is zero. It is illustrated in Fig. 10 under the constant dc-link voltage of 1.1 pu. Besides, Fig. 11 shows the positive-sequence reactive current range supplied by the RECS with no input power.

As denoted in Fig. 13, the current range varies widely under different sequence PCC voltages. The minimum positive-sequence inductive output current to maintain the RECS's controllability corresponds to the maximum i_{q+}^+

(a) Normal control strategy
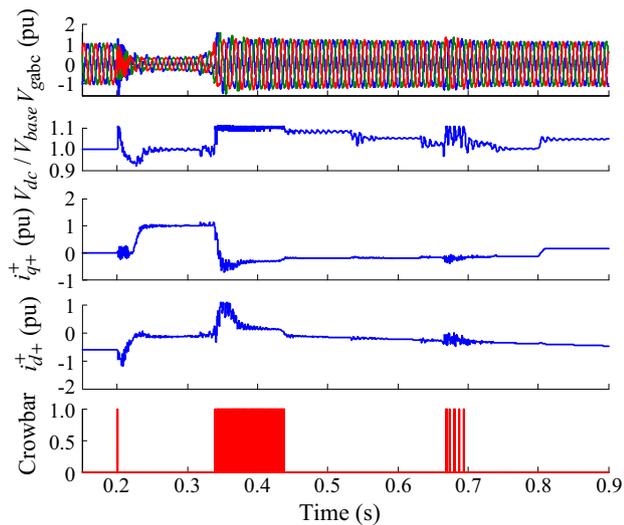
(a) Normal control strategy
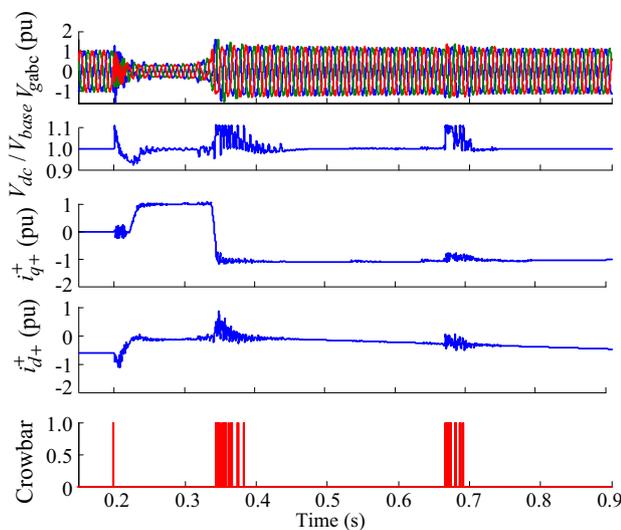
(b) Proposed asymmetrical control strategy

Fig. 15 Simulation results of the RECS in Scenario 1

(b) Proposed asymmetrical control strategy

Fig. 16 Simulation results of the RECS in Scenario 2

defined as $i^+_{q+\_max}$, and can also be solved based on the relationship between $\left|\dot{V}_{gdq}\right|_{max}$ and i^+_{q+} as follows.
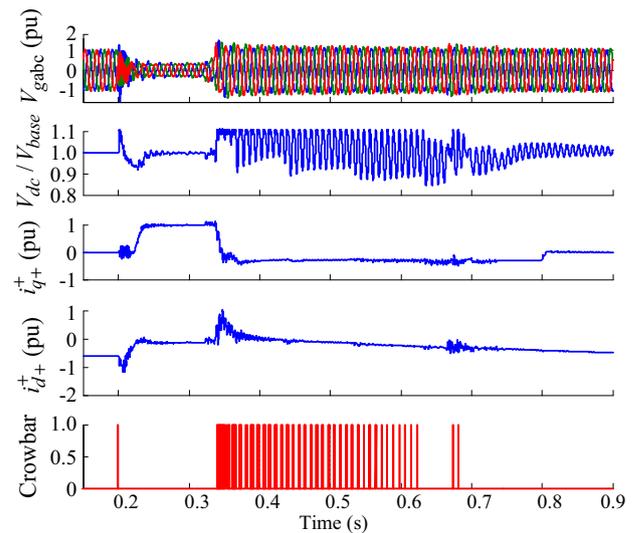
If $\left|\dot{V}_{gdq}\right|_{max}(i^+_{gq+}=0) \leq V_{dc}/\sqrt{3}$, $i^+_{q+\_max}$ can be obtained:

$$i^+_{gq+\_max} = 0 \qquad (20)$$

If $\left|\dot{V}_{gdq}\right|_{max}(i^+_{gq+}=0) > V_{dc}/\sqrt{3}$, $i^+_{q+\_max}$ can be deduced from the following expression:

$$\left|\dot{V}_{gdq}\right|_{max}(i^+_{gq+\_max}) = V_{dc}/\sqrt{3} \qquad (21)$$

Derived from Fig. 11, the power inputted to the RECS's inverter would influence the controllability of the RECS during the fault recovery. However, the input power is

practically required to increase fast by the codes. Thus, recovery speed of the power should not be set to a too high value. Additionally denoted in Fig. 12, the RECS can just ride through the negative- and positive-sequence PCC voltage of 0.7 pu and 1.2 pu at the same time, even when the input power remains zero. According to the maximum sequence PCC voltages of the practical fault recovery analyzed in Section 2, the RECS cannot always both counteract the overvoltage and eliminate the dc-link voltage fluctuations during the continuous period. Therefore, rising in the dc-link voltage is necessary to enhance the asymmetrical HVRT capability of the RECS based on Fig. 13.

5 Asymmetrical control strategy of RECSs during fault recovery

According to the analysis in Section 2, different control schemes have to be employed in the two periods of the fault recovery. Thus, the proposed control strategy contains two parts. In the transient period, a dc-link chopper circuit is applied to avoid tripping the RECS in this strategy. This paper will not discuss it in detail, for the fact that the control scheme of the circuit has been studied widely. In the continuous period, an asymmetrical HVRT scheme is proposed to accomplish the HVRT objective.

The control diagram of the RECS is illustrated in Fig. 14. When the RECS can remain controllable with adjusting the inductive output current, the calculated $i_{gq+\_min}^+$ is used as the reactive current reference in order to keep the dc-link voltage stable. If there is no solution, the dc-link voltage reference would increase to the minimum value which can guarantee the RECS controllability. Moreover, the reactive output current required by the codes ($i_{q+\_code}^+$) should be taken into account.

It should be noticed that the positive-sequence active current reference ($i_{gd+\_ref}^+$) keeps comparatively stable, since it is given by the outer voltage regulating loop of the controller which is slower than the inner current loop. Therefore, this strategy is performed based on $i_{gd+\_ref}^+$ instead of P_0 in order to decrease the control complexity.

6 Simulation verification

The simulations are designed to verify the analysis and effectiveness of the proposed control strategy during the fault recovery. The typical diagram of the RECS integration and the fault recovery process presented in Fig. 2 and Fig. 3 are implemented in the simulation. A RECS rated at 8×1.5 MW is simulated and the parameters are given in Table 1. V_{base} is the DC-link rated voltage.

During the fault recovery, the RECS recovers the active power output in a defined rate. Additionally, the RECS with the normal control strategy is regulated to output constant positive-sequence inductive current of 0.3 pu satisfying E.ON code, when the PCC voltage is greater than 1.1 pu. The conclusions can be drawn from the performance of the RECS shown in Fig. 15 and Fig. 16:

1) In the transient period, the dc-link chopper circuit is triggered, and two control strategies have no effects. These demonstrate the necessity of these protective measures during the fault recovery.

2) With the normal control, the RECS cannot maintain the stability of the dc-link voltage for the over-modulation. Besides, oscillations appear on the dc-link voltage due to the negative-sequence PCC voltage in the continuous period.

3) The proposed control strategy sharply deduces the frequency of triggering the chopper. And the dc-link voltage oscillations can be mitigated because the control effects of the negative-sequence current are identical.

4) When the positive-sequence PCC voltage decreases to the normal range, the RECS cannot regain controllability under the condition that the positive-sequence reactive current reference is zero. That means the RECS cannot be regulated directly based on the grid code requirement.

6.1 Scenario 1

The grid voltage soars to 1.1 pu symmetrically due to the removal of loads. See Fig. 15.

6.2 Scenario 2

The grid voltage soars to positive- and negative-sequence components of 1.05 pu and 0.05 pu due to the removal of unbalanced loads. See Fig. 16.

7 Conclusions

Asymmetrical voltage swells with transients can occur during the fault recovery period. The swells result in fluctuations in the dc-link voltage of RECSs, and may cause reversed power flow and even trip of the RECS.

By studying the characteristics of the typical causes resulting in asymmetrical voltage swells, the PCC voltage during the fault recovery have limited voltage unbalance, phase angle jump and discrete transients. Furthermore, the fault recovery process can be divided into two periods, and different control strategies should be applied in the periods. The asymmetrical HVRT capability of the RECS is analyzed quantitatively by considering the elimination of the dc-link voltage fluctuations. As analyzed in the paper, the RECS cannot always ride through the continuous period during the practical fault recovery without increasing the dc-link voltage, even when the input active power is zero. Additionally, the RECS should not restore the active power output in a too large rate. The results can be used as the guideline of new HVRT grid codes. Based on the analysis, an asymmetrical HVRT control strategy with a chopper circuit is proposed for the RECS to ride through the entire fault recovery process and mitigate the fluctuations. Simulation verified the effectiveness of the strategy.

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