

Islanding detection based on asymmetric tripping of feeder circuit breaker in ungrounded power distribution system

Yuwei SHANG¹, Shenxing SHI¹, Xinzhou DONG¹



Abstract An islanding detection method in ungrounded power distribution system based on single-phase operating mechanisms of the circuit breaker (CB) is proposed in this paper. When CB opens three phase circuits to form an island, one phase circuit is opened firstly and the other two phase circuits are opened secondly after certain duration. During the period when only one phase circuit is opened, negative sequence voltage with certain duration is obtained at DG side because of the asymmetric operation of the system. After all three phase circuits are opened, the voltage variation direction of the two phases that are secondly disconnected from the grid follows the voltage variation direction of the firstly disconnected phase. Based on the above voltage characteristics, an islanding detection scheme is proposed to identify genuine islanding from system disturbances. The performance of the proposed scheme is tested in PSCAD/EMTDC using a 10 kV distribution network with synchronous DG interconnection. Simulation results demonstrate the proposed method is effective and reliable to detect islanding formation.

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State Key Laboratory of Power Systems, Department of Electrical Engineering, Tsinghua University, Beijing 100084, China **Keywords** Distributed generation, Islanding detection, Circuit breaker, Single-phase operating mechanisms

1 Introduction

According to the development strategy of renewable energy industry in China, distributed generation (DG) projects are about to develop more quickly in the following years [1]. As DG plays an increasingly important role in power distribution network, islanding detection capability becomes an essential requirement for distributed generator. Islanding refers to the condition when a portion of power system is energized solely by one or more DGs, while that portion of the grid is electrically separated from the rest of the power system due to faults, utility control measures, as well as system maintenance and repair operations [2, 3]. For fault-induced islanding, protection relays equipped by DG, such as overcurrent relay, are responsible to isolate the DG from the fault [4, 5]. And anti-islanding protection is equipped to disconnect DG immediately after islanding formation, especially for islanding that is not induced by the fault, which is also used to evaluate the performance of the anti-islanding protection relay [6, 7].

In order to tackle this problem, islanding detection techniques have been extensively studied in recent years, which can be classified as local methods and remote methods [6]. Local methods consist of active methods and passive methods. Active methods inject small disturbances into the grid at DG site, and then determine islanding formation based on locally measured responses [8–10]. Active methods are widely used for inverter-based DGs, but few of them have been fully developed for synchronous DGs. Passive strategies detect islanding based on locally measured parameters [11–





13]. These methods are usually of low-cost. However, they are incapable of differentiating islanding formation from disturbances. As a result, islanding detection performance can be severely deteriorated under system disturbance scenarios. This defect has been proved in field application [5].

Remote methods use communication means to transmit specific signals from the substation to DG, and a receiver located at DG site to determine whether an island forms or not in accordance with the received signal. One remote technique is transfer trip scheme, which uses telecommunication means to trip the islanded DG [13]. This scheme monitors the status of all openable devices between the DG and the utility using a central algorithm, if a switching operation causes disconnection to the substation, and the central algorithm will determine the islanded areas and then send tripping signal to the islanded DG. Although it is simple in concept, this scheme can be expensive. Besides, when telecommunication coverage is weak, the specific signal will not be reliably received, and the islanding detection performance will be jeopardized [11].

Another promising remote technique is power line signaling based scheme [14, 15]. This scheme continuously transmits specific signal from upstream substation to downstream DG by a dedicated signal generator. Power line is used as the communication link. Once the upstream circuit breaker (CB) opens to form an island, the DG is unable to receive the signal. As a result, a trip command is sent to disconnect the DG. This scheme outperforms other methods because the injected signal can distinguish genuine islanding and disturbance. However, it is not an economical solution, especially when the amount of interconnected DG is small. Besides, when system fault disturbance occurs, the transmitted signal over the power line may be distorted and interrupted, which will lead to mal-operation.

Following the idea of signal injection, this paper proposes an islanding detection strategy based on single-phase operating mechanisms of CB. With the development of micro-processor based control technology and the increased requirement of customers on power supply reliability, it is feasible for medium-voltage CB to employ single-phase operating mechanisms and to open three phase circuits asymmetrically [11, 16]. Following islanding formation induced by the asymmetric tripping of CB, specific signal is obtained at DG side to identify genuine islanding from system disturbances.

The rest of the paper is developed as follows. Section 2 explains the basic principle of the proposed method, and Section 3 presents the islanding detection algorithm. Then, the islanding detection scheme is presented in Section 4, and A 10 kV ungrounded power distribution network with synchronous DG interconnection is employed to test the proposed method in Section 5. Tested scenarios include islanding formation, load variation and fault disturbance cases. Finally, conclusion is made in Section 6.

2 Basic principle

Before islanding, both the main grid and DG feed the load together. When islanding forms, the proposed asymmetric tripping mode of CB at the grid side operates as follows. One phase circuit such as phase A is opened in advance, then, the other two phase circuits are opened after a fixed delay, for example 60 ms (3 cycles under 50 Hz system). Finally, islanding is formed when all three phase circuits are opened.

Accordingly, three phase voltages at DG side will experience the following changes in response to islanding formation. Before islanding, when distribution system normally operates, the three phase voltages are balanced and within the permissible operation zone of voltage, hence the negative sequence voltage V_2 is negligible. During islanding, when only phase A circuit is opened while phase B and phase C circuits are still connected to the grid, phase A voltage at DG side will change either with an increasing or decreasing direction compared to the rated phase voltage, for reactive power distribution in power system will change, even if active power is balanced between DG and the load. And V_2 will be induced and last at least until the time, at which phase B and phase C circuits are opened, due to the asymmetrical operation.

After all three phase circuits are opened and islanding is finally formed, phase B and phase C voltages will follow the same varying direction of phase A voltage because three phase voltages at DG side become balanced again. Besides, negative sequence voltage V_2 will disappear after three phase voltages at DG side are balanced.

To conclude, based on CB's asymmetric tripping, the islanding formation will result in two evident voltage characteristics at DG side. One is that negative sequence voltage V_2 will appear at first with certain duration. The other one is that three phase voltages will have the same variation direction but with a fixed time gap.

Besides islanding formation, the above voltage characteristics of DG side are further evaluated under other operation scenarios, such as normal load variation and fault disturbance [11, 17]. Although normal load variation scenarios include balanced and unbalanced load variation, on the one hand balanced load variation will not generate negative sequence voltage V_2 , on the other hand unbalanced load variation will have different phase voltages variation characteristics compared with islanding formation. As for fault disturbance, it can be divided into two stages, with the first stage representing fault existence and the second representing fault isolation. During fault existence, depending on the specific fault type, the faulted phase voltage will decrease from the rated voltage, while the sound phase voltages may maintain or even increase





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from the rated voltage in neutral ungrounded system. After fault isolation, three phase voltages will recover to the same magnitude. Accordingly, three phase voltage variation directions are always not the same.

Therefore, the basic principle of the proposed islanding detection method employs unique voltage characteristics at DG side during islanding formation.

3 Islanding detection algorithm

The foregoing two voltage characteristics of islanding formation are implemented by defining the first and second criterion respectively. In the first criterion, voltage unbalance (V_U) is calculated in (1) to implement the characteristic of negative sequence voltage:

$$V_U = \frac{V_2}{V_1} \tag{1}$$

where V_2 and V_1 are root mean square (RMS) values of negative and positive sequence voltage at DG side, respectively.

Assume SET1 is the threshold for V_U , the first criterion is established as:

$$\begin{cases}
V_{U,t} > \text{SET1} \\
t > T_1
\end{cases}$$
(2)

where subscript t indicates the duration of V_U in response to the asymmetric tripping process of CB, and T_1 denotes the duration threshold. In the paper, the asymmetric tripping duration of CB is 60 ms, and T_1 is set as 50 ms by considering the transient process of voltage variation.

The second criterion on three phase voltages variation characteristics is implemented by defining phase voltage variation direction (PVVD). Let $[V_{\min}, V_{\max}]$ denotes the normal phase voltage operation zone, where V_{\min} and V_{\max} represent the lowest and highest RMS values of phase voltage respectively. When phase voltage is within the voltage operation zone, the corresponding PVVD result is "0"; Otherwise, the PVVD would be "-1" if phase voltage below V_{\min} and "1" if above V_{\max} . For illustration purposes, A_{PVVD} , B_{PVVD} and C_{PVVD} are used to denote PVVD results of phase A, B and C voltages respectively. S_{PVVD} represents the integrated results of A_{PVVD} , B_{PVVD} and C_{PVVD} , for instance S_{PVVD} (-1, 1, 0) denotes that A_{PVVD} , B_{PVVD} , and C_{PVVD} are -1, 1 and 0 respectively. Based on this definition, the second criterion is established in (3) and (4), indicating two possible variation directions of phase A voltage after phase A's CB is opened, respectively. Specifically, (3) indicates the increment of phase A voltage, while (4) indicates the decrement of phase A voltage from the rated voltage.

$$\begin{cases}
A_{\text{PVVD},dt} = 1 \\
S_{\text{PVVD},dt+T} = (1,1,1)
\end{cases} (3)$$

$$\begin{cases}
A_{\text{PVVD},dt} = -1; & B_{\text{PVVD},dt} \neq -1; & C_{\text{PVVD},dt} \neq -1 \\
S_{\text{PVVD},dt+T} = (-1,-1,-1)
\end{cases} (4)$$

In (3), subscript dt represents the set time delay to calculate the first S_{PVVD} after V_U exceeds SET1 to avoid the effect of transient process; T denotes the preset asymmetric tripping delay between the operation of phase A and phase B, C circuit breakers, thus, subscript dt+T represents the time to calculate the second S_{PVVD} after V_U exceeds SET1. Accordingly, (3) means that during islanding formation, phase A voltage at time dt increases above the voltage setting zone, and three phase voltages at time dt+T increase above the setting zone after phase-A's CB is opened. In the paper, T is set as 60 ms and dt 30 ms for 50 Hz power system. In (4), notations dt and T are the same as that in (3). But to discriminate islanding formation from fault disturbance in power distribution system with neutral ungrounded, at time dt both phase B and phase C voltages are introduced and investigated. For islanding formation, at time dt both phase B and C circuits are remained connected to the main grid, so $B_{PVVD,dt}$ and $C_{\text{PVVD.d}t}$ will maintain the system voltage, unequal to "-1". However, given three-phase fault occurs, $B_{PVVD,dt}$ and $C_{\text{PVVD},dt}$ will be "-1".

The above thresholds can be set according to the National Standard of Power Quality [18, 19], which stipulates the admissible phase voltage unbalance and deviation in medium-voltage distribution system. For 10 kV system, the admissible three-phase voltage unbalance should be below 2% under normal load variation. So, SET1 is set as 2% in the paper. For the permissible operation zone of phase voltage $[V_{\min}, V_{\max}]$, it is worth noting that the permissible phase voltage is between 88% and 110% of rated RMS value according to IEEE std 1547-2003 [2], whereas in China both positive and negative power supply voltage deviation should be less than 7% of the rated value [19]. And in the paper, V_{\min} and V_{\max} are set as 93% and 107% of rated RMS value of phase voltage respectively according to [19].

4 Islanding detection scheme

By combining the two criteria in a logical order, the islanding detection scheme is proposed in Fig. 1. Firstly, V_U is derived in real time from sampled three phase voltages and continuously compared with the threshold SET1. If V_U is less than SET1, it is determined that the system is





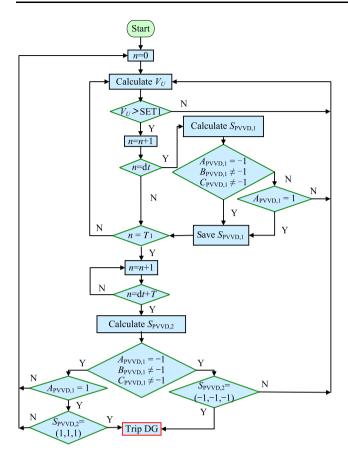


Fig. 1 Flow chart of the proposed islanding detection scheme

under normal condition and the scheme moves to analyze the next sampling point. Once V_U exceeds SET1, a timer starts counting up to set values by using a loop variable n. And in the scheme, three critical time should be calculated. The first critical time is dt. During the time dt, V_U should exceed SET1 continuously. If V_U cannot keep exceeding SET1 before n reaches to dt, it is determined as system disturbance and the scheme will be reset immediately. If V_U meets the requirement, at time dt, $S_{\rm PVVD}$ will be calculated as $S_{\rm PVVD,1}$, which consists of $A_{\rm PVVD,1}$, $B_{\rm PVVD,1}$ and $C_{\rm PVVD,1}$ equals to "-1" while both $B_{\rm PVVD,1}$ and $C_{\rm PVVD,1}$ do not, or, if $A_{\rm PVVD,1}$ equals to "1", $S_{\rm PVVD,1}$ will be saved for further evaluation. All other obtained PVVD results will be concluded as disturbance and the scheme reset immediately.

After $S_{\mathrm{PVVD},1}$ is saved, the second critical time T_1 is judged, which is the duration threshold for V_U exceeding SET1. During the process n increasing to T_1 , if any V_U decreases below SET1, the scheme resets immediately. Otherwise, the first criterion will be qualified when V_U keeps exceeding SET1 until T_1 is reached.

After the qualification of the first criterion, the scheme goes on to evaluate the second criterion at the third critical time point dt plus T. At this time point, the second

 $S_{\rm PVVD}$ is calculated as $S_{\rm PVVD,2}$. Next, both $S_{\rm PVVD,1}$ and $S_{\rm PVVD,2}$ are used to evaluate the second criterion. If $A_{\rm PVVD,1}$ equals to "-1" and $S_{\rm PVVD,2}$ equals to (-1, -1, -1), while $B_{\rm PVVD,1}$ and $C_{\rm PVVD,1}$ are unequal to "-1"; or, if $A_{\rm PVVD,1}$ equals to "1" and $S_{\rm PVVD,2}$ equals to (1, 1, 1), the second criterion will be finally qualified.

If all the foregoing requirements are met, the scheme determines that islanding is formed and a trip signal is issued immediately to disconnect DG.

5 Simulation tests

This section assesses the detection performance of the proposed scheme. The investigated system is a modified network from [5]. Fig. 2 shows the single line diagram of the network. A 110 kV, 50 Hz sub-transmission system feeds the 10 kV distribution system through 110/10 kV, Yg/Δ transformer. A 1 MVA synchronous DG is connected at node 327. An induction motor is connected at node 337. The CB between node 302 and 327 is equipped with asymmetric tripping mode.

The simulation tests are conducted using PSCAD/EMTDC. Specific simulation models and typical parameters are as follows. Distribution feeders are simulated using Bergeron model. Transformers are modeled using *T* circuit. Load is simulated using constant impedance load model. The synchronous DG is equipped with an exciter controlled by voltage. Inertia constant of DG is set as 2 s. The induction motor is simulated using a wound rotor machine, and is rated 0.2 MVA. For the CB between node 302 and 327, the asymmetric tripping duration *T* is 60 ms. In the

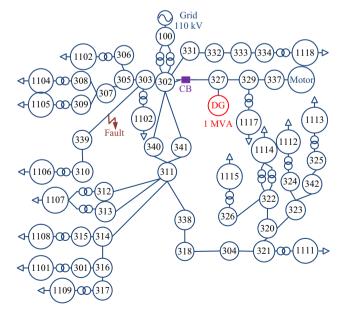


Fig. 2 Single line diagram of the tested system



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islanding detection scheme, T_1 and dt are set as 50 and 30 ms, respectively.

The tested scenarios include islanding formation scenario, load variation scenario and fault disturbance scenario. Load variation scenarios include both balanced and unbalanced load variation, as well as motor start. And fault disturbance scenarios include both symmetric and asymmetric fault disturbance cases.

5.1 Islanding formation scenario

In the simulation, the CB between node 302 and 327 is opened asymmetrically at 5 s. Fig. 3 presents a typical simulation result of the proposed method. Islanding starts to form at 5 s and phase voltages at DG side vary in response to the opening of CB. V_U begins to vary and exceed SET1 at 5.008 s. After 30 ms, $S_{\rm PVVD}$ (-1, 0, 0) is obtained at 5.038 s, which is saved as $S_{\rm PVVD,1}$ for further evaluation. Then, the scheme checks the duration of the first criteria. As seen, from 5.008 s to 5.058 s, V_U keeps exceeding SET1, so the first criterion is met. Further, $S_{\rm PVVD}$ (-1, -1, -1) is obtained and maintained since 5.092 s, so the second criterion is met at 5.098 s, which is 90 ms delay from the instant V_U exceeds SET1. As a result, a trip signal is issued to disconnect DG.

5.2 Normal load variation scenario

Two scenarios of normal load variation scenarios are conducted. One scenario is simulated by adding three-phase or single-phase load to node 1117, which represents balanced and unbalanced load variation respectively. For unbalanced variation, the single-phase load is connected to phase-A circuit. The other scenario is conducted by starting the motor connected at node 337.

In the first scenario, both the local load before load variation and the added load are varied to examine the proposed method. A typical case is simulated by setting the local load as 220% of DG nominal power, and the added three-phase or single-phase load as 90% of DG nominal power. For balanced load variation, in regardless of phase voltage, V_{II} is very insensitive to such scenarios; for unbalanced load variation, V_U increases to 0.26%, which is below SET1, so the proposed scheme does not mal-operate in these two cases. Additionally, it is also found in other simulations that as the local load and added load get heavier, the voltage variation becomes greater. But maloperation of the scheme is prevented in all simulated cases since V_U does not exceed the threshold. This is reasonable due to the existence of the main grid. In comparison with the large balanced network, normal local load variation presents very limited impact on the overall voltage unbalance value.

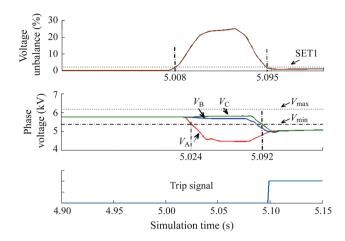


Fig. 3 Islanding detection performance under islanding formation condition

In the second scenario, the induction motor is started from zero speed with the simulation results presented in Fig. 4. The motor is started at 5 s, and all three phase voltages at DG side vary in response to the motor startup. From 5 s to 5.05 s, V_U increases but is below SET1. Afterwards, three phase voltages become balanced again and V_U becomes 0. As a result, the proposed method does not mal-operate during motor startup.

5.3 Fault disturbance scenario

The fault disturbance scenario is conducted by simulating fault occurring on the location shown in Fig. 2. Simulated fault types include single-phase-to-ground fault, two-phase-short-circuit fault, two-phase-to-ground fault, and three-phase fault. To test the proposed method comprehensively, the duration of fault disturbance is varied from 60 ms to 300 ms, considering the typical fault clearing time in medium-voltage distribution system [5].

Figure 5 shows simulation results of the proposed strategy when single-phase-to-ground fault disturbance occurs, the faulted phase is phase A. As seen, fault occurs from 5 s and exists about 200 ms. During fault, $V_{\rm A}$ quickly decreases to 65% of rated value, while $V_{\rm B}$ and $V_{\rm C}$ increases to 123% and 119%, respectively. After 5.22 s, three phase voltages recover to normal value because the fault is cleared. During and after fault, $V_{\rm U}$ does not exceed SET1, so the proposed method is not activated. As a result, the method prevents nuisance trip under this fault disturbance case.

Figure 6 shows simulation result under two-phase-to-ground fault disturbance with faulted phases of phase A and phase B. The fault is assumed to exist for about 60 ms, which equals to the asymmetric tripping operation duration of CB under islanding formation scenario. After fault





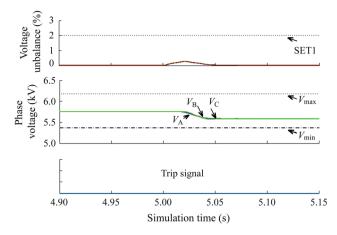


Fig. 4 Islanding detection performance under motor start condition

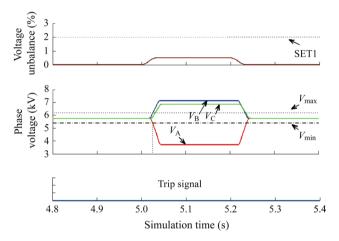


Fig. 5 Islanding detection performance under single-phase-to-ground fault disturbance

occurrence, V_A , V_B , and V_C quickly changes to 80%, 84% and 145% of rated value, respectively. Due to the unbalance of three phase voltages, V_U exceeds SET1 at 5.011 s. After 11 ms, V_A decreases below V_{\min} . Then at 5.031 s, V_B also decreases below V_{\min} while $V_{\rm C}$ increases above V_{\max} , which leads to S_{PVVD} (-1, -1, 1). The same S_{PVVD} is obtained at 5.041 s, which violates the second criterion since the obtained B_{PVVD} is equal to -1. Consequently, the scheme resets at 5.041 s. From this instant on, V_U keeps exceeding SET1. Then, at 5.071 s, S_{PVVD} (-1, -1, 1) is obtained which disqualifies the second criterion, so the scheme resets again. From 5.071 s to 5.079 s, V_U maintains to exceed SET1 with a duration of only 8 ms, which violates the first criterion. Afterwards, V_U keeps less than SET1. Consequently, mal-operation is prevented under this fault scenario.

Besides the foregoing fault disturbance cases, twophase-short-circuit and three-phase fault disturbance scenarios are also simulated with different fault duration

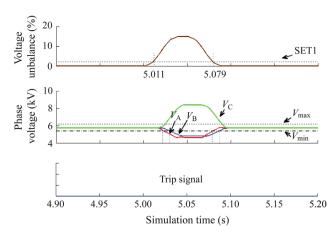


Fig. 6 Islanding detection performance under two-phase-to-ground fault disturbance

setting. Simulation results demonstrate that the proposed scheme can effectively prevent mal-operation under fault disturbance conditions.

6 Conclusion

This paper proposes an islanding detection strategy based on asymmetric tripping of feeder CB in ungrounded power distribution system. Simulation tests demonstrate that the proposed scheme can detect genuine islanding formation. Additionally, the method will not mal-operate under scenarios of normal load variation, induction motor start and system fault disturbances, which improves the reliability of anti-islanding protection. The viability of the method on other types of DGs such as inverter-based DG will be investigated in the next.

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