

Wind turbines output power smoothing using embedded energy storage systems

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Abstract The ability of an energy storage system to improve the performance of a wind turbine (WT) with a fully rated converter was evaluated, where the energy storage device is embedded in the direct current (dc) link with a bidirectional dc/dc converter. Coordinated dc voltage control design of the line-side converter and the energy storage dc/dc converters was proposed using a common dc voltage measurement for smoothing the output power. A transfer function and Bode diagram were introduced to analyze the system performance with different control parameters. MATLAB/Simulink simulations are presented to demonstrate the effectiveness of the proposed methods. It was found that the proposed methods smooth the power output from the WT to the grid and thus improve the quality of the generated power.

Keywords Direct current voltage control, Energy storage system, Power smoothing, Wind turbine

1 Introduction

Wind power fluctuation due to varying wind speed is a serious problem for power network operators, especially in

places where the wind penetration level is high. Most variable-speed wind turbines (WTs) are operated to capture maximum power from wind, which is proportional to the cube of the wind speed. Studies of real wind velocity have shown that most of the wind power fluctuations are located in a very low-frequency range below 1 Hz, and power systems can be very sensitive to these fluctuations [1]. It is thus important to investigate the smoothing of wind power fluctuation.

It is convenient to control the pitch of variable-speed WTs in eliminating low-frequency output power oscillation as no other devices are required [2]. However, this would move the WT away from its optimal operating curve and results in reduced power capture and increased mechanical stress.

Complementing wind with an energy storage system (ESS) has been reported in various cases [3–10]. Currently, there are several kinds of energy storage devices that are suitable for short- to medium-term power exchange, such as a battery, electric double-layer capacitor (EDLC), fly-wheel, and superconducting magnetic energy storage device [3–7]. Of the various storage devices, the EDLC has attracted much attention because of its long life cycle, low maintenance, fast charging/discharging speed, and high energy and power density. Studies have already demonstrated the effectiveness of using the EDLC storage system with wind power [10]. The price of EDLC cells has dropped significantly in recent years, thus making the technology economically feasible.

The main purposes of embedding an ESS into a WT are to improve power quality, enhance fault ride-through ability, dampen short-term power oscillation [11, 12], and in some cases to smooth power fluctuation where the ESS is controlled to absorb or supply power to compensate for the fluctuating output from the generators. The main issues in using an ESS to smooth output power are the ESS topology, capacity requirement, converter control, and ESS

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power reference setting. The power reference is important as it determines the smoothing effect. In general, filters are used to separate the power from the WT generator into the power references for the ESS and the output to the alternating current (ac) network [4, 5]. The level of smoothing strongly depends on the time constant of the filter. A method using the exponential moving average (EMA) of WT-generated power has been proposed [9, 10]. In this method, a formula for the EMA is used to calculate the power output to the network from the previous period's EMA value. The calculated power is then deducted from the captured power to set the reference for the ESS. In the EMA formula, a weighting factor dependent on the calculation period is required and affects the calculated results.

This paper proposes the use of an ESS embedded in the direct current (dc) link of a WT with a fully rated converter for smoothing output power and contributing to dc link voltage control. The paper is organized as follows. A line-side converter (LSC) model and dc link voltage control are discussed in Sect. 2. The ESS and its control system for regulating dc voltage are described in Sect. 3. Section 4 investigates the coordination of the dc voltage controllers of the LSC and ESS. Simulation studies of the proposed methods are carried out with a direct-driven WT using a permanent magnet synchronous generator (PMSG) in Sect. 5. Finally, Sect. 6 draws conclusions.

2 Dc link voltage control

Variable-speed WTs using a fully rated converter are emerging as a preferred technology owing to their superior control ability. Various generator topologies have been used; e.g., induction generators, PMSGs, and electrically excited synchronous generators. Owing to the use of a full-sized back-to-back converter, the generator and ac system are completely decoupled. The converter is usually composed of a generator-side ac/dc converter (GSC), a dc link capacitor and a line-side dc/ac converter. Figure 1 is a schematic diagram of a PMSG-based WT system.

The GSC is directly connected to the generator to control its operation. As the control and operation are well understood [13], no further description is given here. The

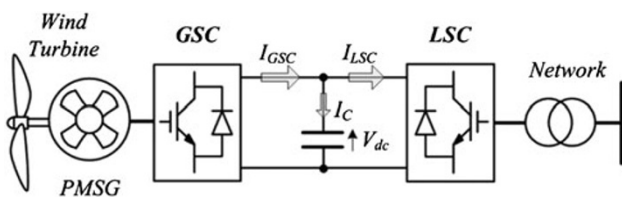


Fig. 1 Schematic diagram of a WT with fully rated converter

capacitor serves as an energy storage device to support the dc link voltage. In addition, the LSC transmits the generated power to the grid so as to maintain a constant dc link voltage. As the dc voltage controller of the LSC is the key part of dc link voltage control, the control of the LSC is discussed below.

2.1 Control of the LSC

Figure 2a, b show the ac and dc equivalent circuits of the LSC where the ac circuit is expressed in the synchronous dq reference frame rotating at the source angular speed of ω_s . V_s and V_c represent the source and converter output voltages, respectively. C is the dc link capacitance. According to Fig. 2a, the system on the ac side can be expressed in the dq reference frame as

$$\begin{cases} v_{cd} = v_{sd} - L \frac{di_{sd}}{dt} - Ri_{sd} + \omega_s Li_{sq}, \\ v_{cq} = v_{sq} - L \frac{di_{sq}}{dt} - Ri_{sq} + \omega_s Li_{sd}. \end{cases} \quad (1)$$

The operation of the LSC requires the current i_{sd} and i_{sq} to follow the varying reference point. Thus, the inner current control loop can be designed as

$$\begin{cases} u_d = \frac{di_{sd}}{dt} = k_{p1}(i_{sd}^* - i_{sd}) + k_{i1} \int (i_{sd}^* - i_{sd}) dt, \\ u_q = \frac{di_{sq}}{dt} = k_{p1}(i_{sq}^* - i_{sq}) + k_{i1} \int (i_{sq}^* - i_{sq}) dt, \end{cases} \quad (2)$$

where k_{p1} and k_{i1} are the proportional and integral gains of the current controller, respectively.

Using the power balance equation and considering the d axis to be fixed to the source voltage V_s , the dc equivalent circuit of the LSC shown in Fig. 2b can be expressed as

$$P_{ac} = \frac{3}{2} v_{sd} i_{sd}, \quad (3)$$

$$P_{dc} = V_{dc} I_{GSC}, \quad (4)$$

$$V_{dc} I_{GSC} = \frac{3}{2} v_{sd} i_{sd} + CV_{dc} \frac{dV_{dc}}{dt}, \quad (5)$$

$$i_{sd} = \frac{2V_{dc} I_{GSC}}{3v_{sd}} - \frac{2CV_{dc}}{3v_{sd}} \cdot \frac{dV_{dc}}{dt}. \quad (6)$$

Similar to the case for the current loop, the controller for the dc voltage can be designed as

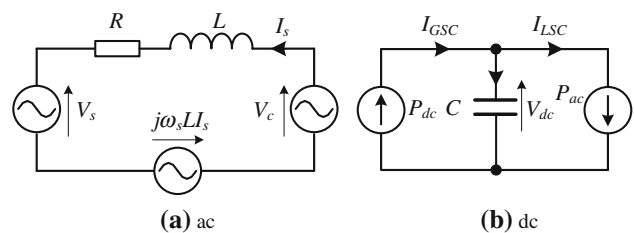


Fig. 2 Equivalent ac and dc circuits of the LSC

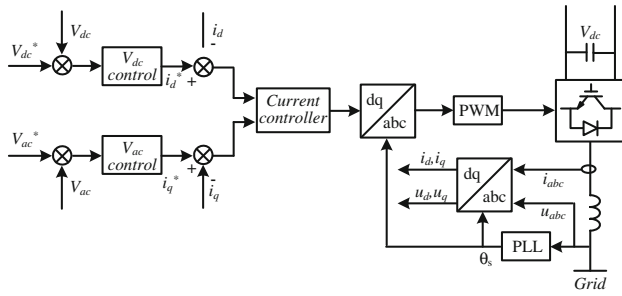


Fig. 3 Control block of the LSC

$$\frac{V_{dc}}{V_{dc}^*} = \frac{sk_{pL} + k_{iL}}{s^2 + sk_{pL} + k_{iL}}$$

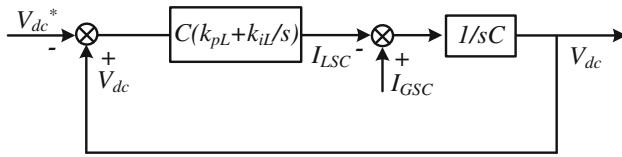


Fig. 4 LSC closed-loop dc voltage controller

$$i_\varepsilon = \frac{dV_{dc}}{dt} = k_{pL}(V_{dc}^* - V_{dc}) + k_{iL} \int (V_{dc}^* - V_{dc}) dt, \quad (7)$$

where k_{pL} and k_{iL} are, respectively, the proportional and integral gains of the voltage controller.

Neglecting the compensation item, the d axis current order for the inner control loop is then given as

$$i_{sd}^* = -\frac{2CV_{dc}}{3V_{sd}} i_\varepsilon. \quad (8)$$

As the reactive power output from the LSC to the system is directly determined by the q axis current, the current order can come from either the reactive power or ac voltage control loop. The current order for the d and q axis are sent to the current controller to produce the modulation voltage, and they then generate the PWM signal for the converter. A simplified schematic diagram of the LSC control system is shown in Fig. 3.

2.2 Dc voltage control dynamics

According to the equivalent circuit in Fig. 2, the output power from the LSC can also be expressed as

$$V_{dc}I_{LSC} = \frac{3}{2} v_{sd} i_{sd}. \quad (9)$$

The dc current fed into LSC I_{LSC} can then be derived as

$$I_{LSC} = \frac{3V_{sd}}{2V_{dc}} i_{sd}. \quad (10)$$

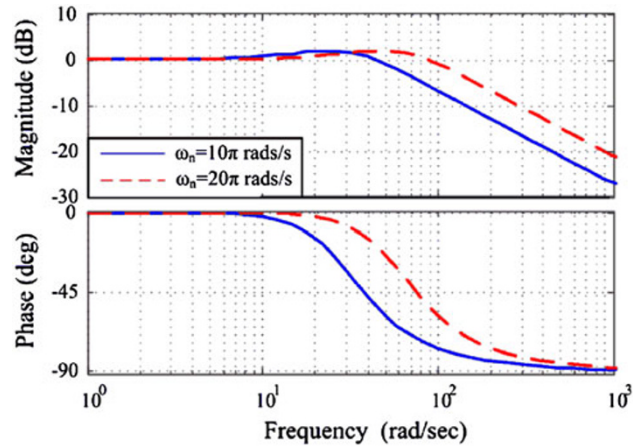


Fig. 5 Bode diagrams for different ω_n

From Eq. (8), the current I_{LSC} can be expressed as

$$I_{LSC} = Ck_{pL}(V_{dc} - V_{dc}^*) + Ck_{iL} \int (V_{dc} - V_{dc}^*) dt. \quad (11)$$

Thus, the block diagram of the dc link voltage controller based on I_{LSC} is obtained as shown in Fig. 4. The proportional–integral (PI) controller has the same parameters as Eq. (7).

According to Fig. 4, the closed-loop transfer function of the dc voltage controller can be expressed as

$$\frac{V_{dc}}{V_{dc}^*} = \frac{sk_{pL} + k_{iL}}{s^2 + sk_{pL} + k_{iL}}. \quad (12)$$

This is a typical second-order control system. Assuming a natural frequency of ω_n and a damping ratio of ζ , the characteristic polynomial can be expressed as

$$p(s) = s^2 + s2\omega_n\zeta + \omega_n^2. \quad (13)$$

Identifying the coefficients gives expressions for the voltage controller PI parameters k_{pL} and k_{iL} as

$$\begin{cases} k_{pL} = 2\omega_n\zeta, \\ k_{iL} = \omega_n^2. \end{cases} \quad (14)$$

The bandwidth of the dc voltage controller is in proportion to the natural frequency, and is limited by the bandwidth of the inner current control loop. The dynamics of the dc voltage loop should be slower than those of the inner current control loop. The damping ratio also affects system stability.

Considering the dc currents fed in from the GSC I_{GSC} and output to the LSC I_{LSC} , according to Fig. 4, the transfer function of the current I_{LSC}/I_{GSC} can be obtained as

$$\frac{I_{LSC}}{I_{GSC}} = \frac{sk_{pL} + k_{iL}}{s^2 + sk_{pL} + k_{iL}}. \quad (15)$$

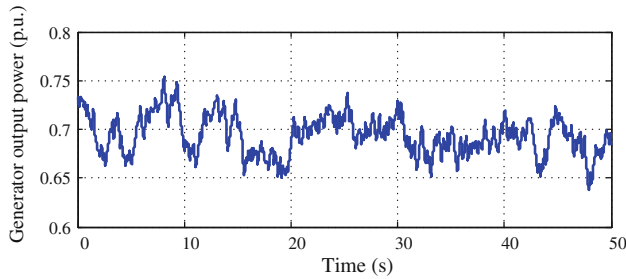


Fig. 6 Generator output power

As seen, Eq. (15) is identical to the dc voltage transfer function shown in Eq. (12). To investigate the control system performance for a different natural frequency, a damping ratio of $1/\sqrt{2}$ and ω_n of 10π and 20π rad/s for the dc voltage controller are taken as an example to investigate the frequency responses of the controller. The Bode diagram of the current transfer function I_{LSC}/I_{GSC} is shown in Fig. 5. It is seen that the controller has a low-pass filter function for the input current I_{GSC} . The cut-off frequency is determined by the natural frequency and damping of the controller and increases with ω_n . In this case, the cut-off frequency at a magnitude of -3 db is 64.5 and 129 rad/s for ω_n of 10π and 20π rad/s, respectively.

Current components contained in I_{GSC} that have frequencies higher than the cut-off frequency mainly flow into the dc link capacitor, resulting in charging and discharging of the capacitor and dc link voltage fluctuation. In an ideal situation, if the wind variation is small, the output power from the generator only contains low-frequency components. Thus, all the generated power will be transmitted to the network through the LSC with negligible high-frequency power flowing into the dc link capacitor, and therefore the dc link voltage will be maintained at a constant value. Thus, the dc link voltage can be used as an indicator of the WT output power fluctuation.

To ensure reliable operation of the converters and to increase the lifetime of the dc capacitors, the fluctuation of the dc link voltage needs to be limited. The Bode diagram of the dc voltage controller is the same as that in Fig. 5. With higher controller bandwidth, the dc voltage controller response is faster, and the power transmitted to the ac network from the LSC can track the input power I_{GSC} better and result in higher ac power fluctuation but smaller dc voltage fluctuation. In contrast, lower bandwidth of the dc voltage control loop results in larger fluctuation of dc link voltage but smaller ac power fluctuation from the LSC.

To validate the analysis, simulations were carried out with MATLAB/Simulink. A 3 MW direct-driven PMSG with fully rated converters was employed to show the results of different controller parameters. The rated dc link voltage was 1.1 kV, and the dc link capacitor was chosen to be 50 mF.

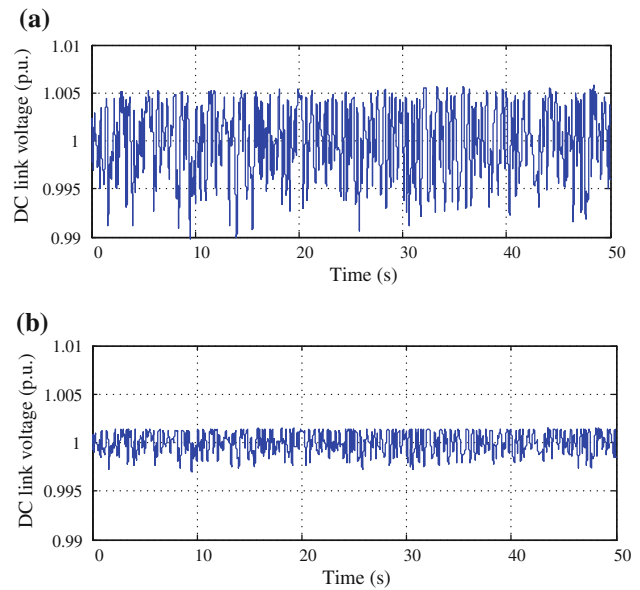


Fig. 7 Dc link voltages of different controller parameters. **a** Dc link voltage with $\omega_n = 10\pi$ rad/s, **b** DC link voltage with $\omega_n = 20\pi$ rad/s

The generator was controlled to produce maximum power from the wind with the GSC, and the LSC was used to control the dc link voltage. The simulated output power from the WT generator is shown in Fig. 6. As shown, owing to the fluctuation of wind velocity, the power output from the generator contains large fluctuation. However, as the fluctuation spectrum is located in a frequency range lower than the cut-off frequency of I_{LSC}/I_{GSC} , the LSC output power (or I_{LSC}) follows the GSC output power (or I_{GSC}), which results in the output power from the LSC having almost the same waveform as the output power from the WT generator shown in Fig. 6. The resultant dc link voltages with different controller bandwidth of 10π and 20π rad/s are shown in Fig. 7a, b, respectively. It is shown that a smaller controller bandwidth results in a larger dc voltage fluctuation.

3 System layout and ESS control

As previously discussed, it is desirable for the WT system to have a very small dc link voltage fluctuation and smoothed LSC output power. However, such objectives cannot be achieved at the same time with the system configuration shown in Fig. 1. This paper proposes an ESS that connects to the dc link of the converters to smooth the LSC power output to the network and to improve the dc link voltage control.

3.1 ESS control and operation

The layout of the system is shown in Fig. 8.

The ESS comprises a bidirectional dc/dc converter and an energy storage device. The high-voltage side is connected

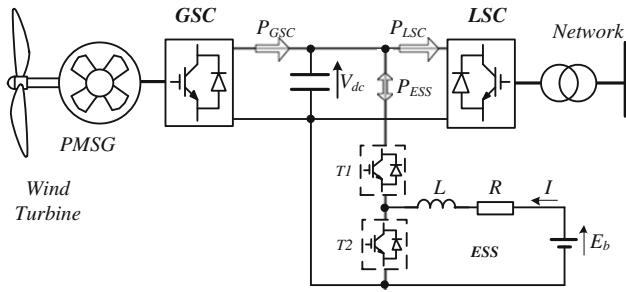


Fig. 8 Layout of the proposed system

to V_{dc} , whereas the low voltage side E_b is connected to the energy storage device. The dc/dc converter contains two insulated gate bipolar transistor switches T1 and T2. The operation of the converter is to alternatively control the switches T1 and T2 to be ON or OFF. When T1 is turned off and T2 is turned on, the converter can be expressed as

$$\frac{dI}{dt} = -\frac{R}{L}I + \frac{E_b}{L}. \tag{16}$$

Conversely, when T1 is turned on and T2 is turned off, the converter can be expressed as

$$\frac{dI}{dt} = -\frac{R}{L}I - \frac{V_{dc}}{L} + \frac{E_b}{L}. \tag{17}$$

Defining the duty cycle $D = t_{on}/T$, where t_{on} is the time when T2 is turned on and T is the switching period, and combining Eqs. (16) and (17) yields

$$\frac{dI}{dt} = -\frac{R}{L}I - \frac{(1-D)V_{dc}}{L} + \frac{E_b}{L}, \tag{18}$$

$$D = 1 - \frac{E_b - RI - L\frac{dI}{dt}}{V_{dc}}. \tag{19}$$

Defining $U_d = dI/dt$ and neglecting the resistance R , the duty cycle can be expressed as

$$D = 1 - \frac{E_b - LU_d}{V_{dc}}. \tag{20}$$

Similar to the case for the LSC dc voltage controller, the error in the current is processed by a PI controller designed as

$$\frac{dI}{dt} = U_d = k_p(I_d^* - I_d) + k_i \int (I_d^* - I_d) dt, \tag{21}$$

where k_p and k_i are the proportional and integral gains. The duty cycle is compared with a triangle carrier wave to generate the switch signals. When $I > 0$, the ESS discharges and operates as a source to supply active power. Conversely, when $I < 0$, the ESS is controlled in a charging state and serves as a sink to absorb active power.

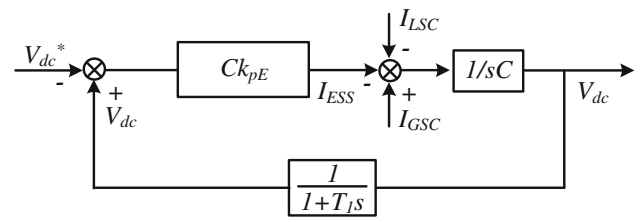


Fig. 9 ESS dc voltage controller

3.2 Dc voltage control using the ESS

As previously analyzed, the dc link voltage can be used as an indicator of power fluctuation. Thus, the ESS is proposed to control the dc link voltage to increase the dc voltage control bandwidth and to contribute to power smoothing. A droop controller is employed to produce the current order for the controller. The ESS absorbs power when the dc link voltage increases, and conversely releases power when the dc link voltage decreases. The current order for the dc/dc converter is

$$I_{ESS}^* = C \cdot k_{pE} \cdot (V_{dc} - V_{dc}^*). \tag{22}$$

Equation (22) has a format similar to that of (11) to make it easier to rationalize the selection of k_{pE} . For the ESS control system, the response of the outer dc voltage controller is slower than that of the inner current controller; thus, the dynamics of the inner controller are neglected when investigating the outer dc voltage controller. The complete controller block of the ESS is shown in Fig. 9. The droop constant of the ESS controller should be large enough to ensure the controller has enough control bandwidth to compensate for the high-frequency power fluctuation. However, the large- k_{pE} system may become unstable as the dc link voltage can contain high fluctuation. A low-pass filter is thus included to eliminate the feedback fluctuation of the dc link voltage. In this example, a

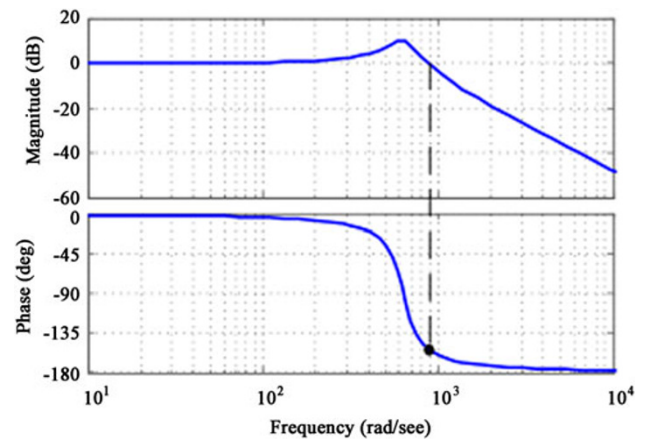


Fig. 10 Bode diagram of I_{ESS}/I_{GSC} with a low-pass filter only

low-pass filter with bandwidth of 200 rad/s (e.g., $T_1 = 0.005$) is chosen.

The transfer function of I_{ESS}/I_{GSC} can be obtained from Fig. 9 as

$$\frac{I_{ESS}}{I_{GSC}} = \frac{k_{pE}}{T_1 s^2 + s + k_{pE}} \quad (23)$$

The Bode diagram of the current transfer function is obtained as shown in Fig. 10. The parameter k_{pE} is chosen to be 2,000 in this example, and it is shown that the ESS has a larger current pass band. The cut-off frequency is 966 rad/s at a magnitude of -3 db for $k_{pE} = 2,000$. However, owing to the relatively large k_{pE} , such a system may be poorly damped and can have oscillation problems. It is shown in the phase frequency diagram of Fig. 10 that the phase margin is small, around 25° . To increase system damping, a proportional-derivative controller $(1 + T_2 s)$ is added to the low-pass filter (i.e., a lead-lag compensator) in the feedback, and the transfer function of Eq. (23) becomes

$$\frac{I_{ESS}}{I_{GSC}} = \frac{T_2 k_{pE} s + k_{pE}}{T_1 s^2 + (1 + T_2 k_{pE})s + k_{pE}} \quad (24)$$

The Bode diagram of (24) is shown in Fig. 11 with $T_2 = 0.001$. The diagram shows a higher phase margin.

By incorporating the ESS, the dc link voltage fluctuation can be reduced by increasing the current cut-off frequency. However, as the aim of both the ESS and LSC controllers is to control the dc link voltage, this could lead to conflict and the controllers need to be properly coordinated through the design of their controller parameters.

4 Power smoothing using the ESS

Combining the dc voltage controllers of the LSC and ESS, the complete block diagram of the dc system is shown in Fig. 12.

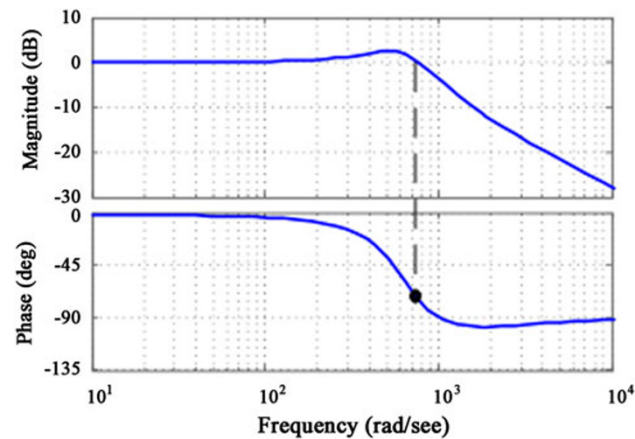


Fig. 11 Bode diagram of I_{ESS}/I_{GSC} with a lead-lag compensator

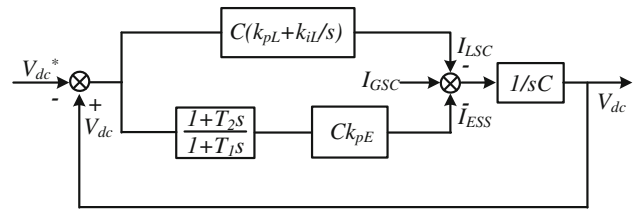


Fig. 12 Closed-loop control system of the dc voltage

To investigate the power flow in the dc link, various currents in the dc link are analyzed. The transfer function of the current I_{ESS}/I_{GSC} and I_{LSC}/I_{GSC} can be obtained according to Fig. 12 as

$$\frac{I_{LSC}}{I_{GSC}} = \frac{T_1 k_{pL} s^2 + (T_1 k_{iL} + k_{pL})s + k_{iL}}{T_1 s^3 + (1 + T_1 k_{pL} + T_2 k_{pE})s^2 + (k_{pL} + k_{pE} + T_1 k_{iL})s + k_{iL}} \quad (25)$$

$$\frac{I_{ESS}}{I_{GSC}} = \frac{T_2 k_{pE} s^2 + s k_{pE}}{T_1 s^3 + (1 + T_1 k_{pL} + T_2 k_{pE})s^2 + (k_{pL} + k_{pE} + T_1 k_{iL})s + k_{iL}} \quad (26)$$

The Bode diagrams of the current transfer functions are obtained as shown in Fig. 13.

As both the ESS and LSC are designed to control the dc link voltage, to compensate for most of the power fluctuation, the dynamic response of the ESSs dc voltage control loop needs to be significantly faster than the LSCs. Thus, the natural frequency of the LSC voltage controller is chosen to be 10π rad/s, and the parameter k_{pE} is 2,000 for the ESS droop controller, which corresponds to an equivalent natural frequency of 1,000 rad/s. It is shown in Fig. 13 that incorporating the ESS and associated droop controller affects the power flow in the dc link; i.e., the

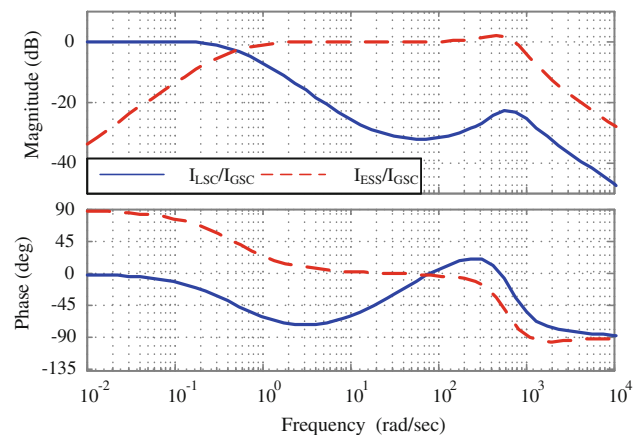


Fig. 13 Bode diagrams of I_{LSC}/I_{GSC} and I_{ESS}/I_{GSC}

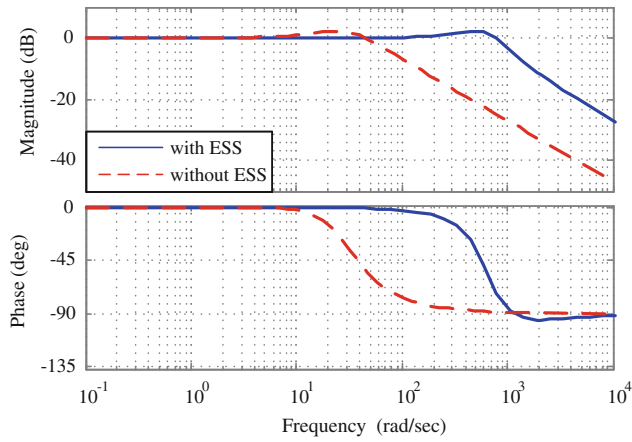


Fig. 14 Bode diagram of the dc voltage control loop

lower power fluctuation is transmitted to the network through the LSC indicating smoothing of the output power; the higher power fluctuation is compensated for by the ESS, and the remainder flows to the dc capacitor. The cross frequency of the LSC and ESS determines the smoothing level of the LSC power output to the ac network and can be calculated by setting

$$\frac{I_{LSC}}{I_{GSC}} = \frac{I_{ESS}}{I_{GSC}} \quad (27)$$

From (27), the cross frequency is calculated to be 0.5 rad/s for this case.

From Fig. 14, the dc voltage transfer function V_{dc}/V_{dc}^* can be derived as

$$\frac{V_{dc}}{V_{dc}^*} = \frac{(T_2 k_{pE} + T_1 k_{pL})s^2 + (k_{pE} + k_{pL} + T_1 k_{iL})s + k_{iL}}{T_1 s^2 + (1 + T_2 k_{pE} + T_2 k_{pL})s^2 + (k_{pE} + k_{pL} + T_1 k_{iL})s + k_{iL}} \quad (28)$$

The corresponding Bode diagram of the voltage transfer function is obtained as shown in Fig. 14. To compare with the WT without the ESS, the Bode diagram of the dc controller without the ESS is also shown in the figure. It is seen that with the ESS and associated droop controller, the bandwidth of the dc voltage controller is significantly improved.

To obtain a satisfactory result of the smoothed output power of the LSC and the dc link voltage, the controller parameters need to be carefully selected. The influence of the LSC and ESS controller parameters on the cross frequency and dc voltage cut-off frequency can be calculated. It is found that the cross frequency decreases with a decrease in the LSC controller bandwidth. The cross frequency also reduces with an increase in k_{pE} . Thus, the LSC bandwidth can be selected to have a relatively low value to provide a better smoothing result, whereas the ESS can

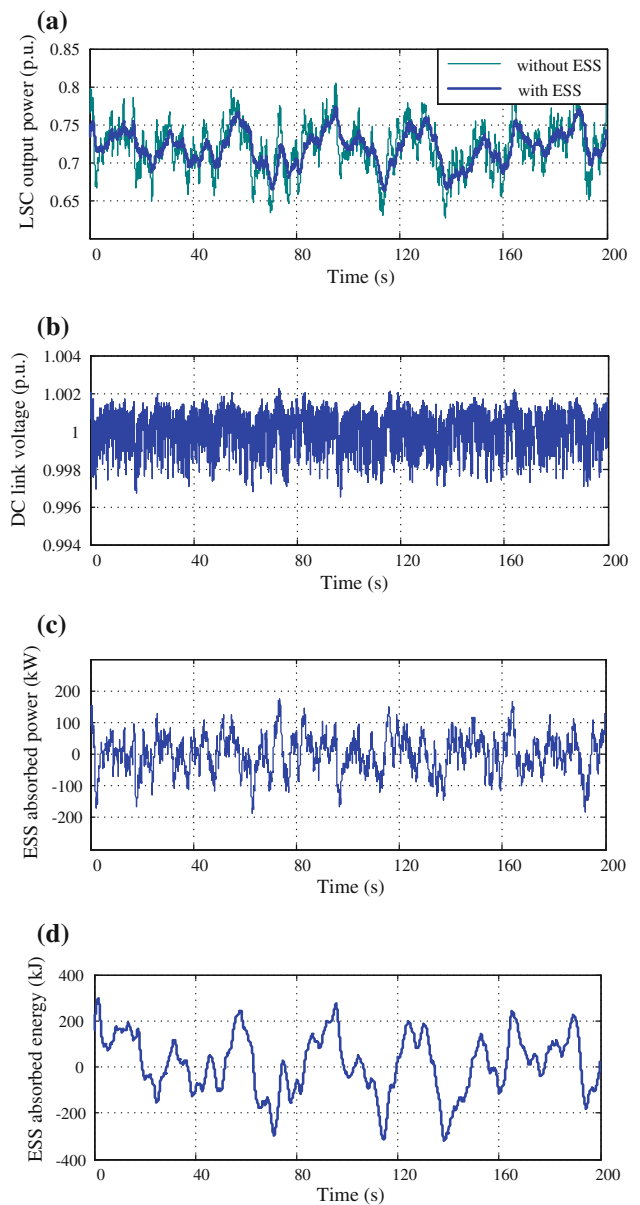


Fig. 15 Simulation results with $\omega_n = 10\pi$ rad/s for the LSC and $k_{pE} = 2,000$ for the ESS. **a** LSC output power, **b** DC link voltage, **c** ESS absorbed power, **d** ESS absorbed energy

increase the dc voltage controller bandwidth of the whole system.

5 Simulation results

To verify the effectiveness of the proposed methods, simulations were carried out with the aforementioned WT system. The ESS connected to the dc link is rated at 300 kW, which is only 10 % of the PMSG capacity.

Simulation results of the ESS using dc voltage control are shown in Figs. 15 and 16.

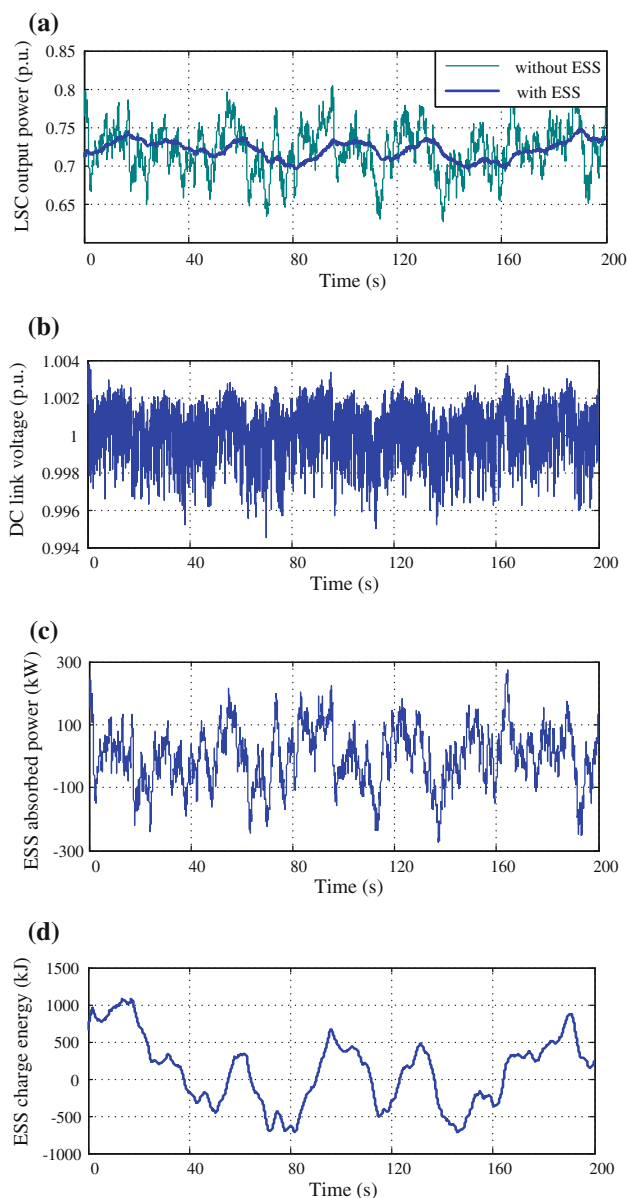


Fig. 16 Simulation results of $\omega_n = 4\pi$ rad/s for the LSC and $k_{pE} = 2,000$ for the ESS. **a** LSC output power, **b** DC link voltage, **c** ESS absorbed power, **d** ESS absorbed energy

Figure 15 shows the results of $\omega_n = 10\pi$ rad/s for the LSC and $k_{pE} = 2,000$ for the ESS droop controller. Because the ESS contributes to the dc voltage control, the natural frequency of the LSC controller can be low. To compare the results for different LSC bandwidths, Fig. 16 shows the results of $\omega_n = 4\pi$ rad/s for the LSC and $k_{pE} = 2,000$ for the ESS droop controller. As seen from Figs. 15a and 16a, the LSC output power is significantly smoothed in the latter case. Comparing the LSC output power shown in Figs. 15a and 16a, it is seen that lower LSC bandwidth has better smoothing results. Comparing the dc link voltage shown in Figs. 7a and 15b, it is seen that for the same LSC dc voltage control bandwidth, the use of

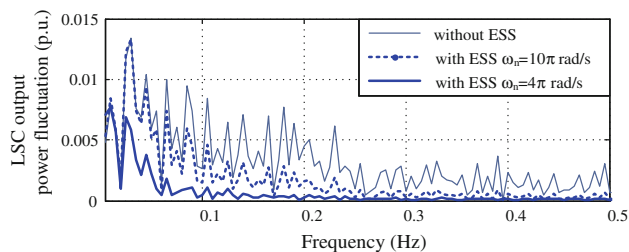


Fig. 17 Frequency spectra of the LSC output power

the ESS for dc voltage control increases the overall control bandwidth of the dc voltage, and thus results in lower fluctuation of the dc link voltage. The ESS absorbed power and energy are shown in Figs. 15c, d and 16c, d. It is shown that in both cases, the power and energy required are small, but to have a better smoothing effect, larger ESS capacity is required. The requirement of ESS capacity is mainly affected by the wind velocity pattern.

Figure 17 shows the spectrum of the LSC output power under different controller parameters. It is shown that by carefully selecting the control parameters, most of the power fluctuations can be smoothed.

6 Conclusion

This paper proposed an ESS to improve the performance of WTs with fully rated converters. A simple power smoothing method based on dc voltage measurement and a coordinated dc voltage controller of the LSC and ESS was proposed. The effect of control parameters on power smoothing was discussed. Simulations were carried out to demonstrate the operation of the system. Different dc voltage control parameters of the LSC and ESS were used to illustrate their effects on system performance. It was shown that the proposed coordinated dc voltage control method not only smoothes the output power from the LSC but also contributes to the dc link voltage control. Moreover, it operates without requiring any communication between the different parts of the system and is therefore robust and reliable.

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