Effect of Heat Transfer during the Vacuum Directional Solidification Process on the Crystal Quality of Multicrystalline Silicon

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Directional solidification (DS) is the most popular technique for massive production of multicrystalline silicon (mc-Si) in the solar industry. Constant improvement of the quality of silicon ingot production remains a research focus. In this work, the temperature distribution, thermal stresses, and melt–crystal (m/c) interface during the DS process with different pulling-down rates were studied by transient numerical simulation and verified by experiment. The results show that the thermal stresses and interface shape during crystal growth play an equally important role in the control of crystal quality, requiring an appropriate pulling-down rate to achieve thermal conditions in the furnace that provide an ideal temperature field in the silicon with lower thermal stresses and a suitable growth interface. Based on these results, an mc-Si ingot grown at 10 μm/s in a pilot-scale DS process had a larger grain size, vertical columnar structure, fewer defects, and a longer minority-carrier lifetime above 3 μs. This suggests that improvement of the quality of mc-Si ingots for solar cells requires comprehensive consideration of the effect of the thermal field conditions on the thermal stresses and grain orientation in the solidification process.

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I. INTRODUCTION

BECAUSE of its low production cost and the relatively higher conversion efficiency of the resulting solar cells, multicrystalline silicon (mc-Si) has become the main material in the photovoltaic market,[1,2] and directional solidification (DS) technology has become the main method for its large-scale production. However, it is a well-known fact that DS-grown mc-Si contains many defects, such as randomly oriented grain boundaries, impurities, and dislocations. These defects, especially the dislocations, limit the lifetime of minority carriers and significantly affect solar cell performance.[3–6] As a result, to obtain satisfactory crystal quality as well as higher energy efficiency, one of the main tasks in mc-Si ingot production is minimization of dislocations during the DS process.[7–9]

The thermal stresses and melt–crystal (m/c) interface shape of mc-Si in the DS process are important since they affect the grain size and crystal growth direction of the grown ingot. Both the thermal stresses and m/c interface shape are primarily determined by the heat transport in the furnace. Therefore, the thermal field plays a very important role in the solidification process, and its improved control by influencing the temperature gradient in a beneficial way will improve the quality and yield of mc-Si. Experimental results on mc-Si obtained from the DS process have been widely and intensively reported.[10–14] However, the generation of dislocations is related to nonuniform thermal deformation, since the thermal stresses are induced by the inhomogeneous temperature distribution in a silicon ingot during solidification. The value and distribution of thermal stresses are difficult to obtain by measurement. However, if the effective stress exceeds the critical resolved shear stress (CRSS) of the material, dislocations will easily exist in the crystal, resulting in increased grain boundaries and grain refinement.[15–19] Similarly, the macroscopic interface shape controls the direction of crystal growth and also strongly influences the generation and propagation of defects during DS.[20] Constant improvement of the quality of silicon ingots during the DS process is our main task, including minimization of defects and impurities, which requires accurate information on the temperature and visible solidification process of the growing ingot. Numerical

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simulation has now become a powerful tool to reveal invisible processes, and many studies have been carried out on the analysis and optimization of the solidification process of crystalline silicon for solar cells.[21–27] Recently, this has also been seen as an effective technique for exploration of the stress or interface of mc-Si. Liu *et al.*[28–30] performed numerical simulations and reported several improvement measures for the DS furnace based on the thermal field. They also obtained the thermal stresses for different solidification durations, finding that the thermal stresses could be reduced by using a longer solidification time and a crucible with high thermal expansion coefficient. Fang *et al.*[31] investigated the influence of furnace design on the thermal stresses during DS of mc-Si. The results implied that the dislocations in the growing ingot can be reduced by optimizing the design of the DS furnace, e.g., by decreasing the distance of bottom insulation to the heat exchanger block, decreasing the side insulation thickness, and increasing the top insulation thickness. Chang[32] confirmed that the m/c interface shape can be adjusted by changing the temperature of the heaters. Miyazawa *et al.*[33–35] numerically investigated the many factors influencing the interface shape in the DS process, and Delannoy *et al.*[36] simulated an mc-Si furnace using a three-dimensional (3D) dynamic mesh and proposed some methods for control of the interface, aiming to improve the crystal quality.

Although there have been some reports on studies of the thermal stresses or m/c interface related to the thermal field, the results of these reports are incomplete, not considering all the factors influencing crystal quality. In this work, a transient numerical model was applied to simulate the DS process of mc-Si under different pulling-down rates, and the evolution rules for the stress field as well as the interface shape under different thermal conditions were carefully researched. At the same time, analysis of experimental results was performed to evaluate the relationship between the thermal stresses, interface shape, and dislocations, and to improve the solidification technology and crystal quality. We hope that these results will improve understanding of the reasons for low efficiency and enhance the application of mc-Si materials in industry.

II. MODEL DESCRIPTION

An axisymmetric furnace is shown schematically in Figure 1. The growth system consists of the silicon feedstock, crucible, resistive heater, insulation shield, water-cooled heat exchange block, and furnace walls. The silicon feedstock is loaded into the crucible with diameter of 0.13 m and height of 0.25 m, and heated to melting by the resistive heater at 1750 K (1477 °C). The heater is toroidal with diameter of 0.24 m, wrapped by a thermal insulation layer with thickness of 0.025 m. The inner chamber of the furnace is divided into a hot zone in the upper part and a cold zone in the lower part.

In the solidification process, the crucible is pulled down from the hot zone to the cold zone and the change of silicon material is shown in Figure 2. In general,

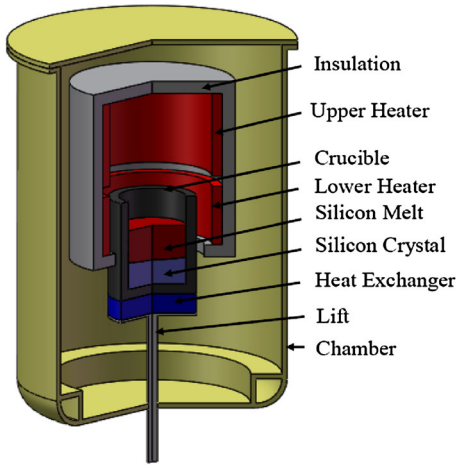

Fig. 1—Model configuration for the cross-sectional area of the vertical furnace system.

during the DS process, a suitable growth temperature gradient is achieved by adjusting the heating power and pulling the moving components (crucible and water-cooled heat exchange block) downwards from the hot zone into the cold zone at a constant rate. In some DS furnaces, there are top and/or bottom heaters. Such systems are more flexible for control of the interface shape and facilitate reduction of the level of von Mises stresses, leading to higher furnace cost and more complex control of the growth process. In our case, since the pulling-down rate is the easiest technical parameter to adjust and control, we only investigated the effect of the thermal field on the solidification process and thermal stresses under different pulling-down rates, so the heating temperature was fixed, and we set a constant boundary temperature of 313 K (40 °C) at the bottom of the heat exchanger to maintain a consistent heat exchange cooling condition. The reasonable assumptions in this model are as follows: (1) The flow in the silicon melt is mainly natural convection caused by density changes. Its maximum velocity is not more than 0.04 m/s, and it has little effect on the m/c interface and no dominant heat transfer effect. Moreover, to facilitate convergence of the simulations, the flow in the silicon melt was ignored; (2) All radiative surfaces are diffuse-gray. In addition the system is under vacuum (0.01 Pa), so the gas flow effect in the furnace was ignored.

Based on the above discussion, the governing equations for conductive heat transfer in all components can be described as follows:

$$\rho C_{\mathrm{p}} \frac{\partial T}{\partial t} = \nabla \bullet (k \nabla T) + Q, \qquad [1]$$

where ρ, C_{p}, and T are the density, specific heat capacity, and temperature, respectively. The parameter k is the thermal conductivity, and Q is the heat source term. The radiative heat exchanges between all gray and diffuse surfaces in the furnace were calculated by the following equations:

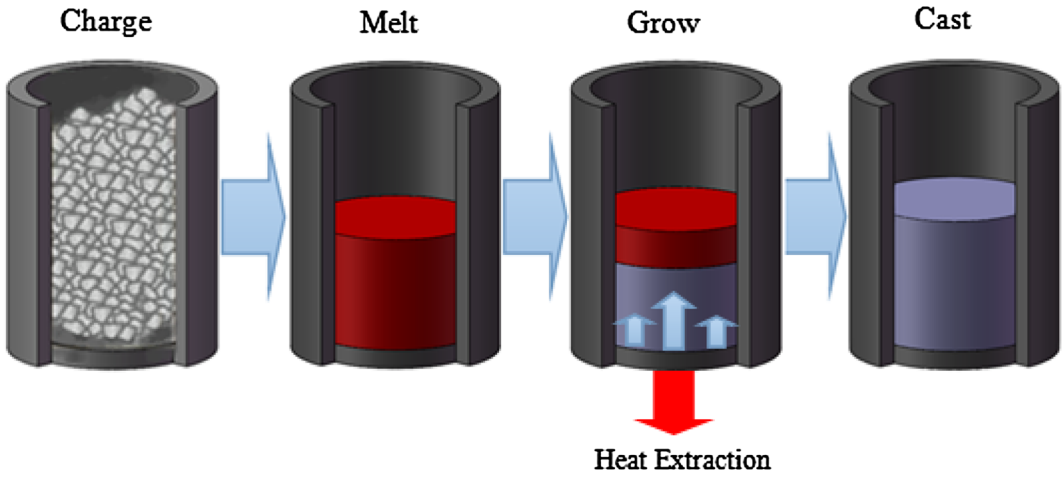

Fig. 2—Directional solidification of mc-Si in the vertical furnace.

$$-\vec{n} \bullet (-k\nabla T) = \varepsilon(G - \sigma T^4), \quad [2]$$

$$(1-\varepsilon)G = J - \varepsilon\sigma T^4, \quad [3]$$

where ε is the emissivity, σ is the blackbody radiation constant, G is the irradiation, and J is the radiosity. Since the relative position between the radiative surfaces will change as solidification progresses, the changes of the radiation angle factor between the radiative surfaces was considered in the calculation of the radiative heat transfers by the simulation software. It is very important to accurately simulate the m/c interface for transient simulation of the DS process. As a result, the m/c interface shape was obtained by a dynamic interface tracking method, which included calculation of the solidification latent heat. During the phase transition, a mixture of both solid and molten material coexists in the "mushy" zone. A Gaussian curve was defined to represent the portion of phase change, given by

$$\delta = \frac{\exp[-(T - T_m)^2/(\Delta T)^2]}{\Delta T\sqrt{\pi}}, \quad [4]$$

where T_m is the melting point and ΔT denotes half of the transition temperature span, which was set to 0.01 K (0.01 °C) in this case. The release of latent heat was considered through the change in enthalpy, ΔH. In addition, the specific heat capacity C_p also changes considerably during the transition. To account for the latent heat related to the phase transition, we replaced C_p in the heat equation with $(C_p + \delta\Delta H)$, where ΔH is the latent heat of the transition. The change in specific heat can be approximated as $\Delta C_p = \Delta H/T$, being represented using the software's built-in smoothed Heaviside step function. Dynamic interface tracking was implemented using the fraction of liquid phase B, given by

$$B = \begin{cases} 1, & T > T_m + \Delta T \\ (T - T_m + \Delta T)(2\Delta T), & (T_m - \Delta T) \le T \le (T_m + \Delta T) \\ 0, & T < T_m - \Delta T \end{cases} \quad [5]$$

The stress–strain relation for a thermoelastic solid body can be given by the following formulation:

$$\begin{pmatrix} \sigma_r \\ \sigma_z \\ \sigma_\theta \\ \tau_{rz} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{13} & 0 \\ C_{12} & C_{22} & C_{23} & 0 \\ C_{13} & C_{23} & C_{33} & 0 \\ 0 & 0 & 0 & C_{44} \end{pmatrix} \begin{pmatrix} \varepsilon_r - \alpha_r(T - T_{ref}) \\ \varepsilon_z - \alpha_z(T - T_{ref}) \\ \varepsilon_\theta - \alpha_\theta(T - T_{ref}) \\ \gamma_{rz} \end{pmatrix} \quad [6]$$

In the above equation, α_r, α_z, and α_θ are the thermal expansion coefficients with $\alpha_r = \alpha_z = \alpha_\theta = 2.6 \times 10^{-6}\ K^{-1}$, and C_{ij} are the elastic coefficients of silicon crystal. Silicon crystal has a cubic structure, and there are only three elastic coefficients C_{11}, C_{12}, and C_{44}. So, all other coefficients can be expressed as $C_{11} = C_{22} = C_{33}$ and $C_{12} = C_{13} = C_{23}$.[32] Thermoelastic stress analysis in the axisymmetric cylindrical coordinate system can be performed by using a displacement-based model,[37] and the magnitude of gravity in the crystal is negligible compared with that of the thermal stresses, so the axisymmetric elastic stresses are governed by the following equilibrium equations:

$$\frac{1}{r}\frac{\partial}{\partial r}(r\sigma_r) + \frac{\partial \tau_{rz}}{\partial z} - \frac{\sigma_\theta}{r} = 0, \quad [7]$$

$$\frac{1}{r}\frac{\partial}{\partial r}(r\tau_{rz}) + \frac{\partial \sigma_z}{\partial z} = 0, \quad [8]$$

where σ_r, σ_z, and σ_θ are the normal stresses in the radial, axial, and azimuthal directions, respectively, and τ_{rz} is the shear stress. The strain–stress relationships are required for closure of the model, and can be denoted as

$$\varepsilon_r = \frac{\partial u}{\partial r}, \quad \varepsilon_z = \frac{\partial v}{\partial r}, \quad \varepsilon_\theta = \frac{u}{r}, \quad \varepsilon_{rz} = \frac{\partial u}{\partial z} + \frac{\partial v}{\partial r}, \quad [9]$$

where u and v are the displacement components in the radial and axial direction, respectively. The thermal stress equations can be calculated associated with the

boundary conditions. The m/c interface can move freely and was treated as a no-traction boundary, $\vec{\sigma} \bullet \vec{n} = 0$. The axisymmetric boundary condition $v = 0$, $\partial u/\partial n = 0$ was applied to the axial center. The ingot/crucible wall interfaces were rigid boundaries, and the displacements u and v on the interface were set to zero, meaning that the crucible constraint is strict. After calculation of the stress components, the von Mises stress for an axisymmetric geometry can be obtained as

$$\sigma_{\text{von}} = \sqrt{\frac{(\sigma_r - \sigma_z)^2 + (\sigma_\theta - \sigma_r)^2 + (\sigma_\theta - \sigma_z)^2 + 6\tau_{\text{rz}}^2}{2}}. \quad [10]$$

The calculation of the CRSS for silicon was as given in References 38, 39], i.e., $\sigma_{\text{crss}} = [\exp(10.55 + 10{,}147/T)] \times 10^{-7}$. When $\sigma_{\text{von}} \le \sigma_{\text{crss}}$, the excess stress $\sigma_{\text{ex}} = 0$; while for $\sigma_{\text{von}} > \sigma_{\text{crss}}$, one has $\sigma_{\text{ex}} = \sigma_{\text{von}} - \sigma_{\text{crss}}$. Based on this calculation, σ_{crss} is rather small compared with σ_{von}, so we use the von Mises stress directly to represent the stress level during the solidification process. The material thermophysical properties used in the current simulation are listed in Table I. Some properties were provided by manufacturers.

Table I. Material Properties Used in the Simulation

Physical Property	Value	Unit
Silicon solid		
Density	2,330	kg/m^3
Thermal conductivity	75	W/mK
Specific heat	1,000	J/kgK
Latent heat	1,800	kJ/kg
Young's modulus	170	GPa
Poisson's ratio	0.28	
Emissivity	0.5	
Silicon melt		
Density	2,520	kg/m^3
Thermal conductivity	60	W/mK
Specific heat	890	J/kgK
Crucible		
Density	1,710	kg/m^3
Thermal conductivity	100	W/mK
Specific heat	1,800	J/kgK
Emissivity	0.8	
Insulators		
Density	200	kg/m^3
Thermal conductivity	0.045	W/mK
Specific heat	500	J/kgK
Emissivity	0.2	
Heater		
Density	1,800	kg/m^3
Thermal conductivity	100	W/mK
Specific heat	1,800	J/kgK
Emissivity	0.9	
Chamber		
Density	7,900	kg/m^3
Thermal conductivity	15	W/mK
Specific heat	477	J/kgK
Emissivity	0.2	
Cool water		
Density	1,000	kg/m^3
Thermal conductivity	60	W/mK
Specific heat	4,185	J/kgK

III. RESULTS AND DISCUSSION

Numerical solution of the transient simulation was realized to analyze the DS process at different pulling-down rates of 5, 10, and 15 μm/s using the commercial software COMSOL Multiphysics 4.2a. Based on an actual furnace, a 1:1 model was built to ensure that the process was consistent with the actual situation. Due to the nonlinear results combined with the moving grid in this model, an adequate mesh had to be found and some boundary meshes were refined several times. In addition, to prove the validity of the model, we set several temperature monitoring points in the model, corresponding to thermocouple positions in our experimental system. Comparing the temperatures at these points in the numerical simulation with those obtained by experiment, we found deviations in the range of ± 5 K (± 5 °C). According to the simulation, the growth conditions under different pulling-down rates of the pilot-scale mc-Si ingots were investigated by analysis of experimental results as well.

A. *Thermal Stresses and Temperature Distribution for Solidification Process*

Comparing the simulation results, it was found that the stress distributions and contour line shapes were similar because the temperatures were also similar for the three conditions. We took the stress distribution characteristics at four different solid fractions of silicon for the 5 μm/s condition to represent the other conditions. As shown in Figure 3, it was found that stresses occurred during the whole solidification process, and the stress levels were higher in the peripheral and bottom region than in the internal region at each time step; along with solidification of the melt, the maximum stresses gradually concentrated to the peripheral region, i.e., adjacent to the crucible inner wall. The time solution also revealed that the thermal stresses increased as the melt solidified because the temperature difference in the ingot increased. Figure 4 shows the stresses at different solidification fractions of silicon under different pulling-down rates. We can conclude that the maximum stresses also increased as the pulling-down rate increased; i.e., the maximum von Mises stress values were larger for faster pulling-down rate (15 μm/s) and smaller for slower pulling-down rate (5 μm/s).

Figure 5 shows the temperature distributions in the vertical direction along the centerline of the silicon at different solidification fractions. It was found that the slope of the temperature distribution lines was smaller with a slower pulling-down rate, and accordingly the temperature difference on the centerline of the silicon ingot defined as $T_{\text{d}} = T_{\text{max}} - T_{\text{min}}$ was relatively smaller at different solid fractions, as shown by the accurate results in Figure 6. After completion of solidification, namely when the solidification fraction was 1.0, the maximum temperature gradient in the silicon ingot was

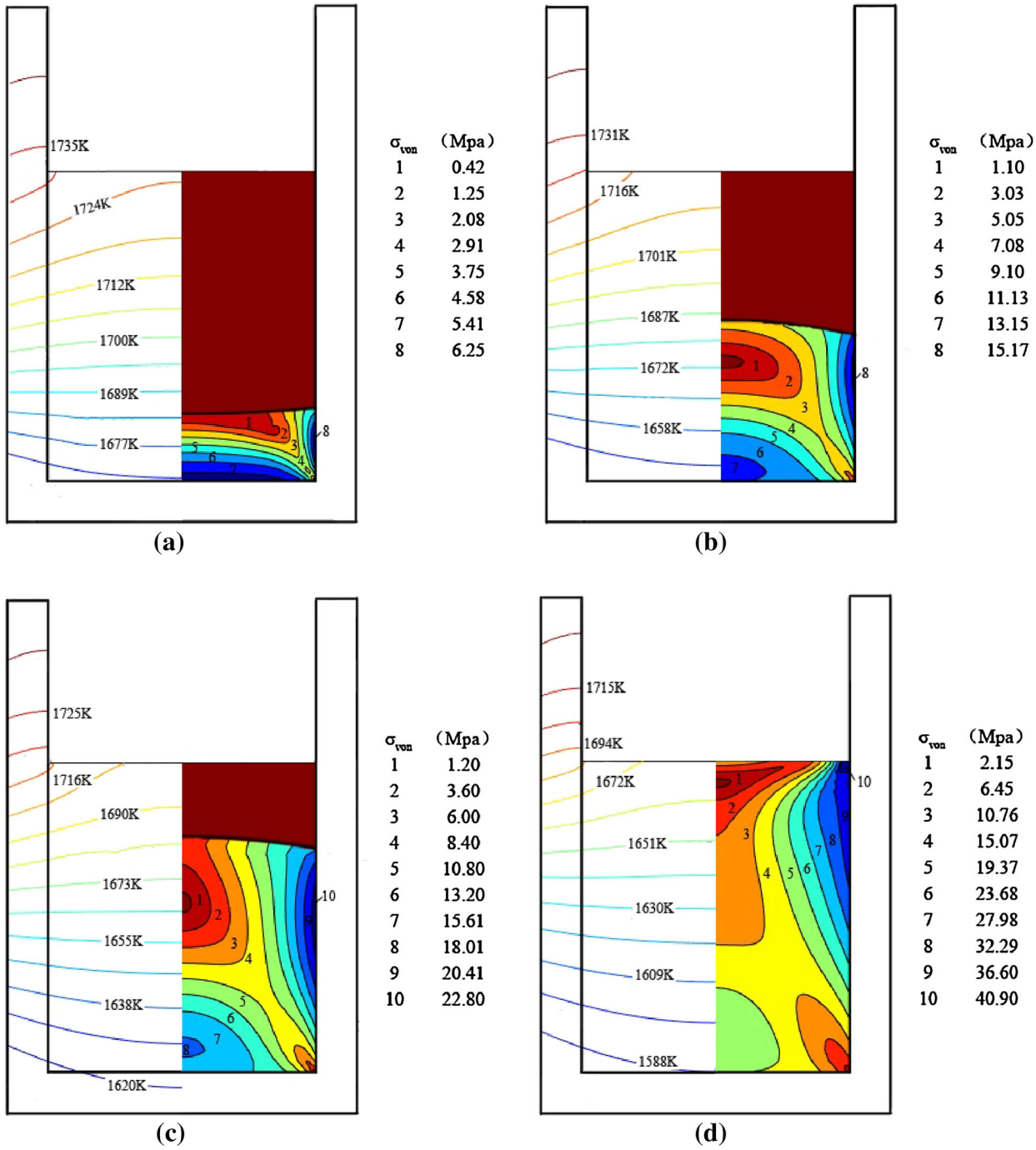

Fig. 3—Temperature (left part) and von Mises stress (right part) distributions in the silicon ingot during solidification process at different solid fractions: (*a*) 0.25, (*b*) 0.5, (*c*) 0.75, and (*d*) 1.0.

about 5.4, 6.2, and 7.4 K/cm for 5, 10, and 15 μm/s, respectively. In addition to the overall expansion stresses caused by the constraint of the crucible walls, due to the uneven temperature distribution inside the silicon ingot, uneven expansion of adjacent parts of the crystal also induced stresses by their mutual restraint; That is, when the temperature changes unevenly, different parts of the silicon ingot should expand to different degrees. Since the silicon ingot is a continuum, its internal neighboring particles will constrain each other from free expansion. Thus, the larger the temperature differences within the silicon ingot, the larger the temperature gradient, the greater the differences between the expansion scales of different parts within the silicon ingot, and accordingly the greater the thermal stresses.[9] These results therefore suggest that reducing the temperature difference in a silicon ingot enables growth of high-quality silicon ingots with low thermal stresses and few dislocations,

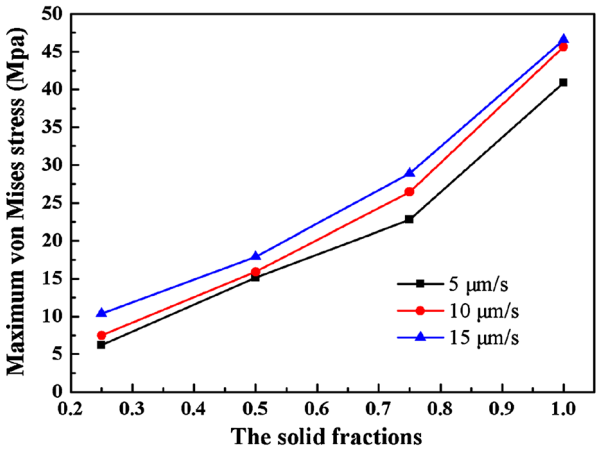

Fig. 4—Maximum von Mises stresses of silicon at different solidification fractions under different pulling-down rates.

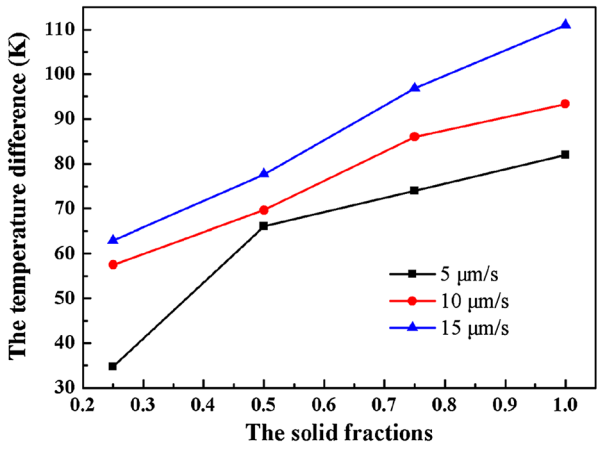

Fig. 6—Temperature differences of silicon at different solidification fractions under different pulling-down rates.

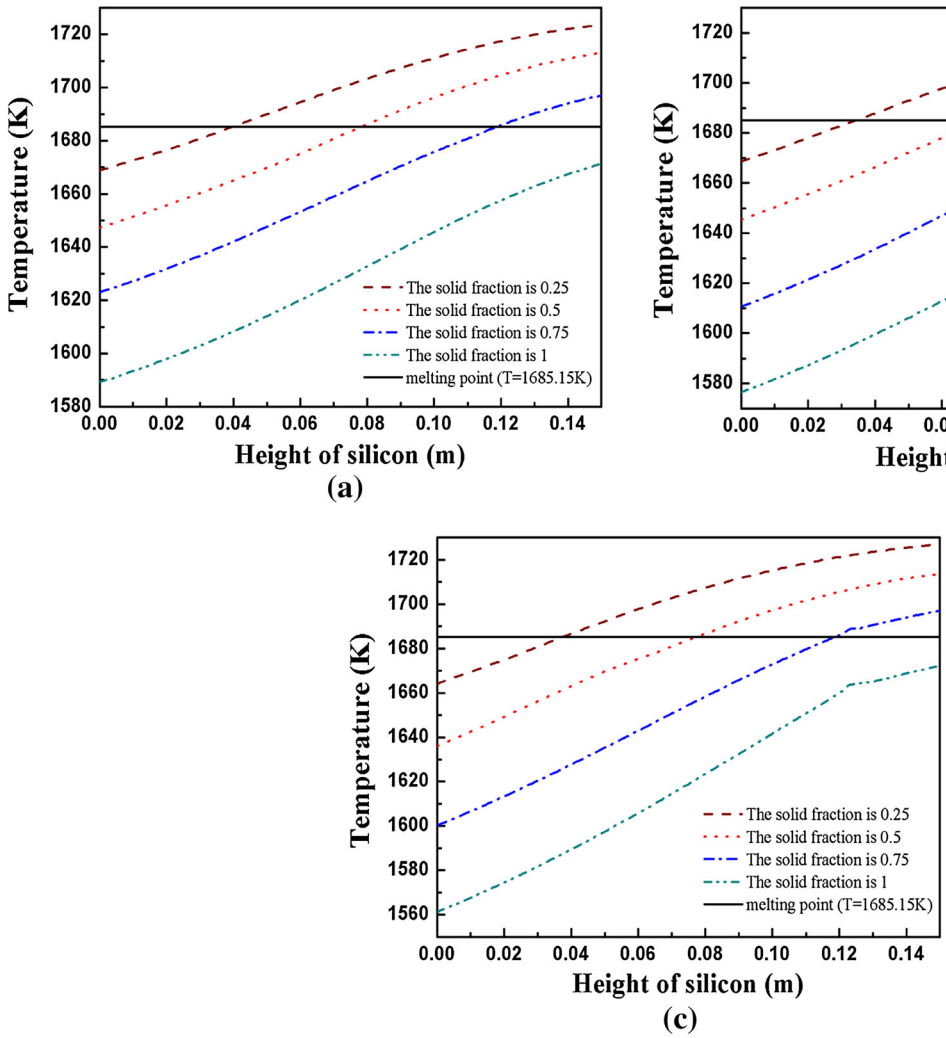

Fig. 5—Temperature distributions in the vertical direction along the centerline of the silicon at different solidification fractions: (*a*) 5 μm/s, (*b*) 10 μm/s, (*c*) 15 μm/s.

and a slow pulling-down rate should be selected to produce the silicon ingot.

B. *M/c Interface Shape and Crystal Growth Orientation*

It is well known that a slightly convex and less varying interface shape is favorable for the mc-Si DS process. Such an interface can not only push away impurities from the solidification front to the corner region of the ingot, but also reduce parasitic nucleation from the crucible wall and enable silicon crystals to grow in the most central area of the crucible bottom to enlarge consistently into columnar crystals. Figure 7 displays the shapes of the m/c interface for solidification fractions of 0.25, 0.5, and 0.75 under different pulling-down rates. This will help us to determine the grain growth orientation under different pulling-down rates and further analyze the temperature field inside the furnace. It was seen that the m/c interface was concave at the beginning of solidification, and then gradually became convex for the 5 μm/s pulling-down rate (Figure 7(a)). Such an m/c interface would make the grain growth direction change a lot, which is not conducive to the formation of columnar crystals and may even cause grain fracture under the effect of stresses, resulting in grain refinement and increase of defects in the transitional period of the interface. In the condition of 15 μm/s, the m/c interface retained a slightly convex shape during the

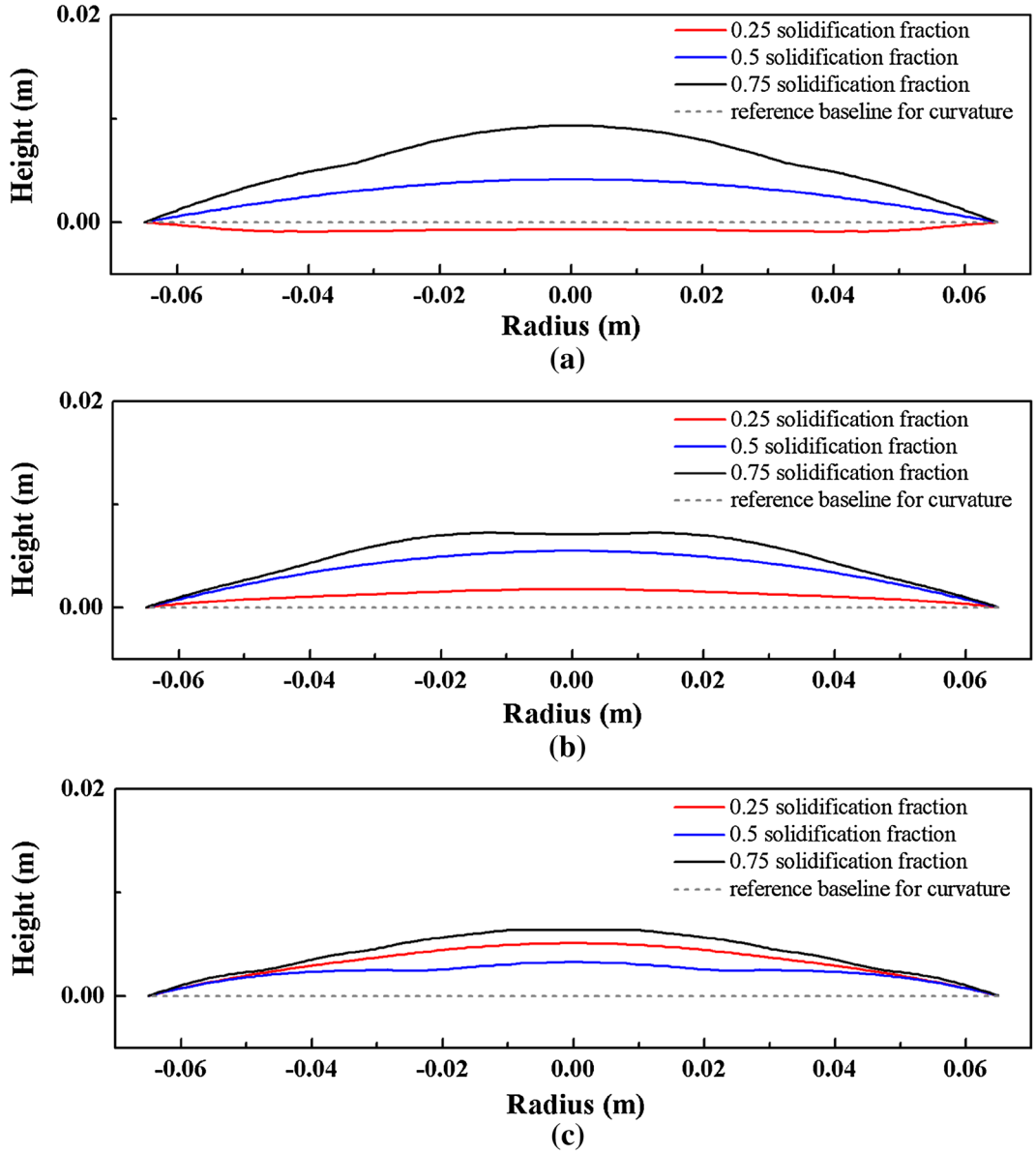

Fig. 7—M/c interface shape for 0.25, 0.5, and 0.75 solidification fractions under different pulling-down rates: (*a*) 5 μm/s, (*b*) 10 μm/s, (*c*) 15 μm/s.

whole process, but as can be seen from Figure 7(c), the m/c interface was more convex at the solidification fraction of 0.25 than at 0.5. The m/c interface experienced a change from convex to flat and again to convex, again being unfavorable for grain growth. When the pulling-down rate was 10 μm/s, the m/c interface was relatively flat in the early stages of the process and then became slightly convex gradually; the variation was smaller, as was the curvature, as shown in Figure 7(b). Such a slightly convex and steady interface shape would provide conditions for grain enlargement and meets the crystal morphology requirements for solar-grade (SoG)-Si.

Columnar grains are oriented approximately parallel to the heat flux direction within the Si, or, in other words, in the direction normal to the m/c interface. The m/c interface shape will be identified approximately by the shape of the T_m isotherm, which will be normal to the heat flux lines at T_m and influenced by all transfer into and out of the crucible, specifically being determined by the ratio of the lateral and bottom heat dissipation of the crucible. In our case, the cooling condition at the bottom of the crucible is fixed. So, based on the shape of the m/c interface, we can analyze the lateral heat dissipation of the crucible and the temperature field inside the furnace under different pulling-down rates. When the lateral heat dissipation is greater than that at the bottom, the melt close to the crucible wall can solidify faster, resulting in a concave m/c interface. Because the increase of the heat transfer area in unit time is smaller, the temperature of the cold zone and the furnace inner wall would not increase quickly enough when the crucible is pulled down from the hot zone to the cold zone at a slower rate, leading to a larger temperature difference between the crucible wall and inner furnace wall and relatively larger lateral heat dissipation at the beginning of solidification. As the portion of the crucible in the cold zone increases to a certain extent, the accumulated heat dissipation of the crucible in the furnace becomes relatively higher for a slower pulling-down rate, which will enhance the effect of heating the cold zone. Thus, increasing the temperature in the furnace leads to weakening of the lateral heat dissipation of the crucible and the convexity of the m/c interface. Therefore, determining the optimum technological parameters associated with the thermal characteristics is a key factor to control a high-quality Si ingot manufacturing process.

C. *Crystal Quality of the Silicon Ingots*

Based on the simulation results, a vacuum DS furnace was used to produce mc-Si at different pulling-down rates of 5, 10, and 15 μm/s. To minimize the effects of impurities on ingot casting, unified raw silicon materials with purity of about 99.99 pct and high-purity graphite crucibles with stable physical properties were used for the experiment. Figure 8 shows the crystal morphology in longitudinal cross-sections of the middle part of the silicon ingots after being cut and cleaned, with the grain growth directions marked by arrows. It was found that the silicon ingot produced at pulling-down rate of 10 μm/s exhibited a more satisfactory crystal morphology (Figure 8(b)). Its crystal grains grew larger along the growth direction, and many fewer grains grew from the sidewall, mainly due to the slightly convex and more stable m/c interface (Figure 7(b)), yet there were obvious cracks on the silicon surface near the crucible wall (marked with black circles in Figure 8(b)), which were possibly caused by high thermal stresses. By contrast, the grains were refined at the beginning of solidification and the crystal grew from the bottom to top in a divergent shape for the 5 μm/s condition along the direction normal to the m/c interface based on the thermal field (Figure 7(a)), thus many fine grains grew from the crucible bottom in the silicon ingots. In the same way, it can also be noted that there were cracks in the same place of the silicon ingot (marked with black circles in Figure 8(a)). This may be an indicator that the maximum stresses were concentrated in the upper peripheral region of the silicon ingot, similar to the results of the simulation shown in Figure 3. What can be noticed firstly in Figure 8(c) is that the grains were significantly refined over the whole cross-section, even if there were no cracks in the silicon surface near the crucible wall. The refined grains may be caused by the pressing from greater thermal stresses and the unstable interface, likely indicating that the temperature field inside the furnace at this rate was no longer suitable for crystal growth. These results suggest that the pulling-down rate should be less than 15 μm/s for this furnace type and conditions.

Silicon ingots were divided into six equal parts, from bottom to top, and we took parts 2/6, 3/6, 4/6, and 5/6 of the ingot for measurements and statistical analysis. The grain sizes at the different positions in the axial direction are presented in Table II. The average grain sizes for the three conditions increased gradually from the bottom to the top of the silicon ingots, especially for the conditions of 5 and 10 μm/s. In all three cases, from the simulation results, we know that crystals grow in the appropriate temperature conditions and crystal grains expand more evenly under a smaller temperature gradient. So, the grain boundary and grain amount were significantly reduced along the growth direction; accordingly, the defects, particularly the dislocation densities, decreased gradually along the growth direction as well based on the statistical results of metallographic analysis. Whereas the thermal conditions for 15 μm/s suppressed grain growth, and even led to multiplication of defects, eventually the average grain sizes in the Si ingot were minimized. These results are in keeping with the above simulation results and analysis.

Figure 9 shows the minority-carrier lifetime of the mc-Si ingot. The measurement was carried out using a wafer tester system (Semilab, model WT-1000B). To achieve reliable results, we executed a multipoint measurement operation and averaged the measured values. The results show that the ingot fractions from 2/6 to 5/6 exhibited higher carrier lifetimes, with values reaching around 3 μs or even longer near the axis of symmetry for 5 and 10 μm/s. The decreased lifetimes in the bottom and edge regions are related to diffusion of impurities and defects caused by thermal stresses.[23] These regions are actually inevitable and would be cut off before the Si

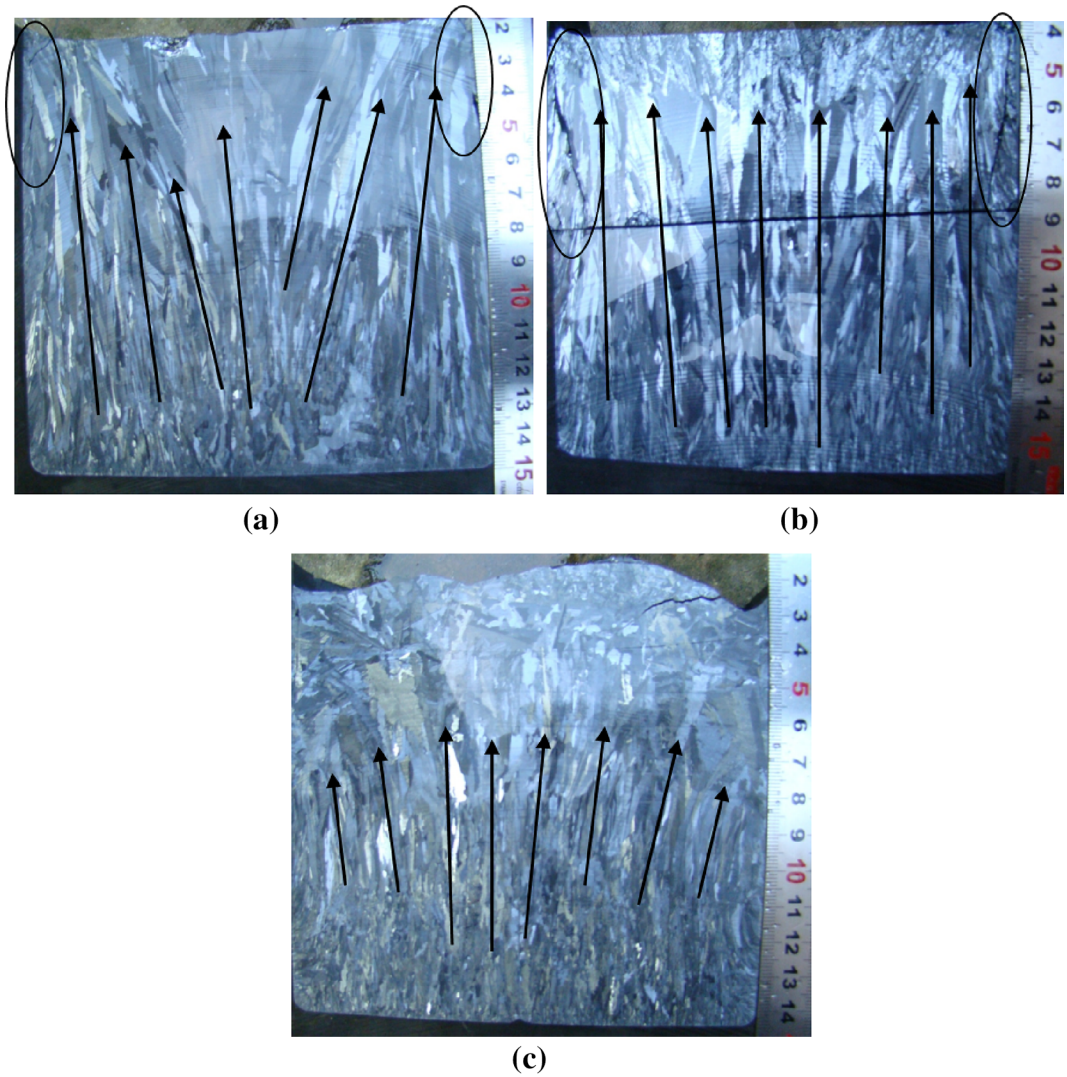

Fig. 8—Crystal morphology of silicon ingots in a longitudinal sectional at different pulling-down rates: (*a*) 5 μm/s, (*b*) 10 μm/s, (*c*) 15 μm/s.

Table II. Grain Sizes at Different Positions in Axial Direction of Silicon Ingots at Different Solidification Rates

	Grain Size (mm)			
Rate (μm/s)	2/6 of Ingot	3/6 of Ingot	4/6 of Ingot	5/6 of Ingot
5	1.88	2.06	2.36	2.71
10	2.03	2.44	2.83	3.10
15	1.31	1.48	1.71	2.00

wafer manufacturing process. Considering the above results, we can conclude that such mc-Si ingots grown by the DS process by selecting suitable technical parameter values could be used as Si wafers for solar cells. From the results of simulation and experiment, we can conclude that columnar crystals with the largest grain size and longest carrier lifetime grew under the condition of the 10 μm/s solidification rate. In addition, a short process time is also important for commercial purposes. Hence, the relevant conditions must be determined to combine high production throughput and high material quality, and 10 μm/s is still the preferred pulling-down rate for the system. We anticipate that investigation and analysis will provide advice for the industrial process to improve the quality and reduce the cost of solar cell wafers.

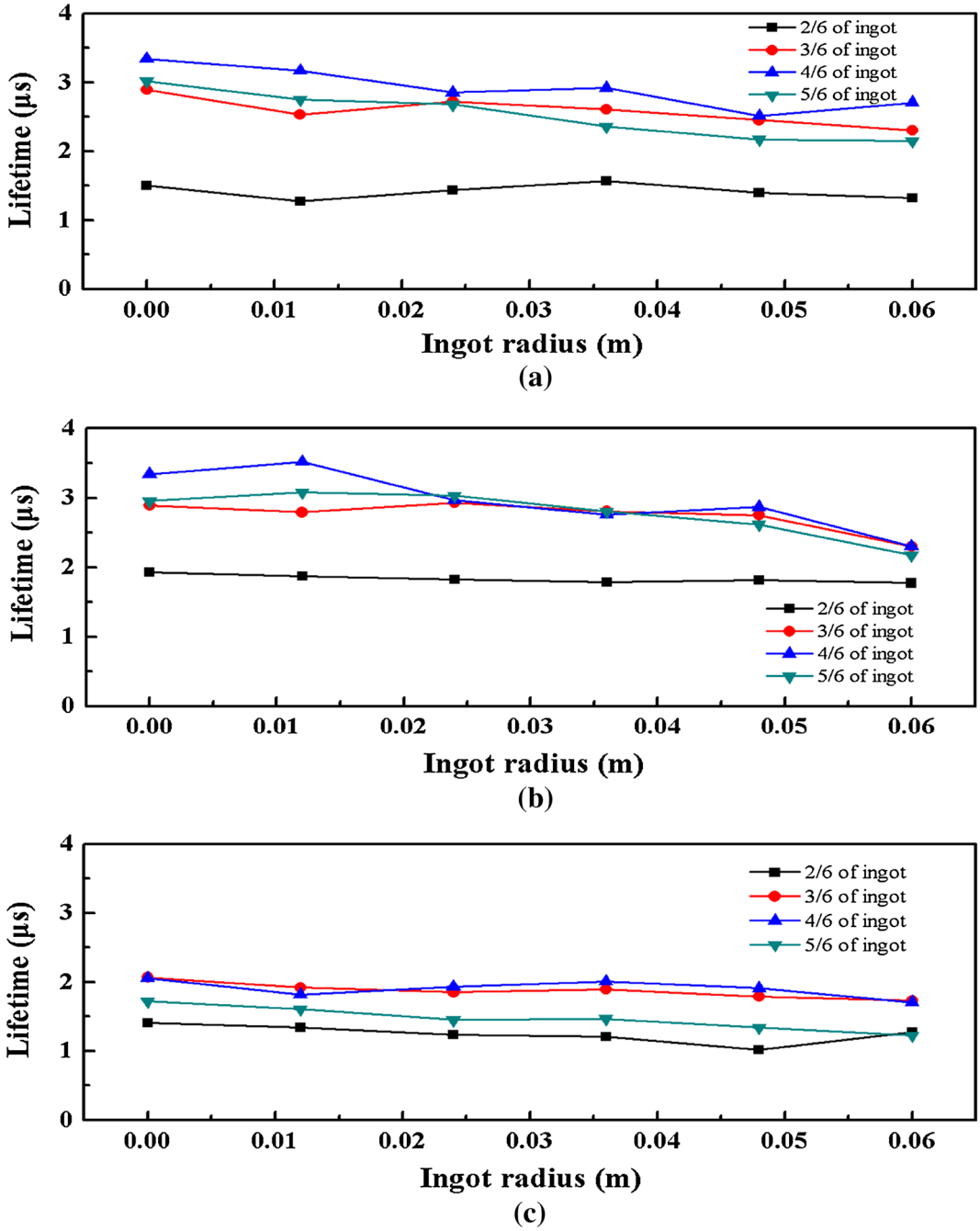

Fig. 9—Minority-carrier lifetime distribution of the mc-Si ingot: (*a*) 5 μm/s, (*b*) 10 μm/s, (*c*) 15 μm/s.

IV. CONCLUSIONS

The evolution of the temperature distribution, thermal stresses, and interface was determined by transient numerical simulation to investigate the effect of the thermal field on the solidification process under different pulling-down rates and to demonstrate the thermal characteristics of the DS process used to grow Si ingots. Both the numerical simulation and experimental results show that a slow pulling-down rate with a small temperature gradient can reduce the thermal stresses in the silicon ingot during the solidification process, while an appropriate pulling-down rate is required to achieve a temperature distribution in the furnace that provides a suitable m/c interface shape for crystal growth. In our case, the rate of 10 μm/s was particularly suitable for growth of high-quality mc-Si, meaning that the m/c interface shape also plays an important role in control of crystal quality. Therefore, we can expect to manipulate the crystal quality of silicon ingots for solar cells by controlling the thermal stresses and crystallographic orientations during the solidification process.

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REFERENCES

1. J.M. Kim and Y.K. Kim: *Sol. Energy Mater. Sol. Cells*, 2004, vol. 81, pp. 217–24.
2. D.I. Kim and Y.K. Kim: *Sol. Energy Mater. Sol. Cells*, 2006, vol. 90, pp. 1666–72.
3. K. Yang, G.H. Schwuttke, and T.F. Ciszek: *J. Cryst. Growth*, 1980, vol. 50, pp. 301–10.
4. G. Dour, F. Durand, and Y. Brechet: *Modell. Simul. Mater. Sci. Eng.*, 1997, vol. 5, p. 275.
5. R.B. Ganesh, B. Ryningen, M. Syvertsen, E. Øvrelid, I. Saha, H. Tathgar, and G. Rajeswaran: *Energy Proc.*, 2011, vol. 8, pp. 371–76.
6. B. Wu, N. Stoddard, R.H. Ma, and R. Clark: *J. Cryst. Growth*, 2008, vol. 310, pp. 2178–84.
7. B. Gao, S. Nakano, H. Harada, Y. Miyamura, T. Sekiguchi, and K. Kakimoto: *J. Cryst. Growth*, 2012, vol. 352, pp. 47–52.
8. T. Luo, G.Q. Lv, W.H. Ma, K.X. Wei, X. Yang, and S.Y. Li: *J. Cryst. Growth*, 2013, vol. 384, pp. 122–28.
9. X. Yang, W.H. Ma, G.Q. Lv, K.X. Wei, T. Luo, and D.T. Chen: *J. Cryst. Growth*, 2014, vol. 400, pp. 7–14.
10. T.Y. Wang, S.L. Hsu, C.C. Fei, K.M. Yei, W.C. Hsu, and C.W. Lan: *J. Cryst. Growth*, 2009, vol. 311, pp. 263–67.
11. K.M. Yeh, C.K. Hseih, W.C. Hsu, and C.W. Lan: *Prog. Photovolt.*, 2010, vol. 18, pp. 265–71.
12. T.F. Li, K.M. Yeh, W.C. Hsu, and C.W. Lan: *J. Cryst. Growth*, 2011, vol. 318, pp. 219–23.
13. T.F. Li, H.C. Huang, H.W. Tsai, A. Lan, C. Chuck, and C.W. Lan: *J. Cryst. Growth*, 2012, vol. 340, pp. 202–08.
14. C.W. Lan, W.C. Lan, T.F. Lee, A. Yu, Y.M. Yang, W.C. Hsu, B. Hsu, and A. Yang: *J. Cryst. Growth*, 2012, vol. 360, pp. 68–75.
15. I. Demirdzic and D. Martinovic: *Comput. Methods Appl. Mech. Eng.*, 1993, vol. 109, pp. 331–49.
16. R. Ma, H. Zhang, D.J. Larson, and K.C. Mandal: *J. Cryst. Growth*, 2004, vol. 266, pp. 216–23.
17. H.L. Zhang, C. Nie, Y.H. Xiong, D.M. Xie, and Y.Z. Yu: *Int. J. Therm. Sci.*, 2012, vol. 53, pp. 100–107.
18. M.P. Bellmanna, E.A. Meese, M. Syvertsen, A. Solheim, H. Sørheim, and L. Arnberg: *J. Cryst. Growth*, 2011, vol. 318, pp. 265–68.
19. M.P. Bellmann, H. Dalaker, M. Syvertsen, S. Gouttebroze, and M. M'Hamdi: *J. Cryst. Growth*, 2013, vol. 362, pp. 38–41.
20. I. Takahashi, N. Usami, K. Kutsukake, G. Stokkan, K. Morishita, and K. Nakajima: *J. Cryst. Growth*, 2010, vol. 312, pp. 897–901.
21. L.J. Liu and K. Kakimoto: *Int. J. Heat Mass Transf.*, 2005, vol. 48, pp. 4481–91.
22. J. Wei, H. Zhang, L. Zheng, C. Wang, and B. Zhao: *Sol. Energy Mater. Sol. Cells*, 2009, vol. 93, pp. 1531–39.
23. J.W. Shur, B.K. Kang, S.J. Moon, W.W. So, and D.H. Yoon: *Sol. Energy Mater. Sol. Cells*, 2011, vol. 95, pp. 3159–64.
24. H.S. Fang, J. Tian, Q.J. Zhang, Y.Y. Pan, and S. Wang: *Int. J. Heat Mass Transf.*, 2012, vol. 55, pp. 8003–09.
25. H.S. Fang, Y.Y. Pan, L.L. Zheng, Q.J. Zhang, S. Wang, and Z.L. Jin: *J. Cryst. Growth*, 2013, vol. 363, pp. 25–32.
26. A. Black, J. Medina, A. Piñeiro, and E. Dieguez: *J. Cryst. Growth*, 2012, vol. 353, pp. 12–16.
27. W.C. Ma, L.L. Zhao, G.Q. Ding, Y. Yang, T.Z. Lv, M. Wu, and L.J. Liu: *Int. J. Heat Mass Transf.*, 2014, vol. 72, pp. 452–60.
28. X.J. Chen, S. Nakano, L.J. Liu, and K. Kakimoto: *J. Cryst. Growth*, 2008, vol. 310, pp. 4330–35.
29. L. Sun, L.J. Liu, Z.Y. Li, and W.H. Zhao: *Materials for Renewable Energy and Environment (ICMREE), 2011 International Conference on, IEEE 2011*, vol. 1, pp. 95–99.
30. Z.Y. Li, L.J. Liu, X. Liu, Y.F. Zhang, and J.F. Xiong: *J. Cryst. Growth*, 2014, vol. 385, pp. 9–15.
31. H.S. Fang, S. Wang, L. Zhou, N.G. Zhou, and M.H. Lin: *J. Cryst. Growth*, 2012, vol. 346, pp. 5–11.
32. C.E. Chang and W.R. Wilcox: *J. Cryst. Growth*, 1974, vol. 21, pp. 135–40.
33. H. Miyazawa, L. Liu, S. Hisamatsu, and K. Kakimoto: *J. Cryst. Growth*, 2008, vol. 310, pp. 1034–39.
34. H. Miyazawa, L.J. Liu, and K. Kakimoto: *J. Cryst. Growth*, 2008, vol. 310, pp. 1142–147.
35. H. Miyazawa, L. Liu, and K. Kakimoto: *Cryst. Growth Des.*, 2009, vol. 9, pp. 267–72.
36. Y. Delannoy, F. Barvinschi, and T. Duffar: *J. Cryst. Growth*, 2007, vol. 303, pp. 170–74.
37. J. Fainberg and H.J. Leister: *Comput. Methods Appl. Mech. Eng.*, 1996, vol. 137, pp. 167–74.
38. N. Miyazaki, H. Uchida, T. Munakata, K. Fujioka, and Y. Sugino: *J. Cryst. Growth*, 1992, vol. 125, pp. 102–111.
39. N. Miyazaki and S. Okuyama: *J. Cryst. Growth*, 1998, vol. 183, pp. 81–88.