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Designing majority gate-based nanoscale two-dimensional two-dot one-electron parity generator and checker for nano-communication

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Abstract

At the present time, logic circuits design prototypes with quantum-dot cellular automata (QCA) have been comprehensively researched. The confines of orthodox CMOS technology induce to the breakthroughs of different technologies, one of which is QCA. Thoughtlessly, because of the deficiency of advance assembly support, QCA circuits frequently agonize from several sorts of manufacture shortcomings and variations and, hence, are error prone and defective. QCA technology is forming its aspect due to extreme effectiveness and rapidity with lesser area requirement. This study, a novel architecture of parity generator and checker, is proposed based on two-dot one-electron cells. Parity generator and checker assist in impeccable binary information communication from point to point. With the outlined parity generator and checker circuit, a nano-communication architecture is designed. The designed architecture is rationalized with a competently established standard mathematical operation based on Coulomb's theory. All the outlined design contains a minimum number of cells, extent, and energy compared to existing four-dot two-electron QCA designs. The outlined designs comprehend minimum majority gate and latency. Besides, power depletion by the designs is measured and it is perceived that the total energy and power required to operate these designs are incredibly low.

Keywords Quantum-dot cellular automata · Parity generator · Parity checker · Nano-communication · Power depletion

Introduction

By reason of its excessive speed and cohesive layout potential, the CMOS archetype may perhaps control the digital realm for the previous eras. However, according to contemporary analyses specified in [1], the typical CMOS archetype is about to agonize from several scaling deficits in the proximate future. A few eminent scaling confines of CMOS archetype assimilate dimensional constraint, reducing switching frequency, off-status leakage current, etc. The impulse for extreme-functioning digital outlines in nanoscale is assumed to be the prime encounter with CMOS archetype. Therefore, an obligation of reasonable,

competent nanostructure as QCA arises into play being a substitute of CMOS archetype which is adept of extreme thickness, noticeable speed in nanoscale outlines with minimal power depletion. Several prevailing alternatives of QCA are, for instance, molecular [2] and magnetic quantum cellular automata [3], 4-dot 2-electron QCA [4–7] and 2-dot 1-electron QCA [8]. This study emphasizes on the metal dot offset part of QCA. The 4-dot 2-electron version of QCA is utterly studied. A number of studies have been done in this area till now for instance [9–15]. The 2-dot 1-electron QCA can decode the binary data with electron formation inside the cell. Data can be conducted from one cell to another with cell-to-cell interface. Some of the earlier studies on 2-dot 1-electron QCA is organized in [8, 16]. Like 4-dot 2-electron QCA architecture, the essential paradigms of 2-dot 1-electron are majority gate, planar wire crossing wires and inverter that are classified in [8]. The two-dimensional 4-dot 2-electron cell is a square structure. Where, four "dots" at the four positions contain two electrons which can relocate between neighboring dots of the identical cell and acquire the transversely reverse positions owing to Coulomb's repulsion

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[17]. In 2-dot 1-electron QCA, overall dots and electrons quantity per cell are nearly lessened by half. Besides, the four formations out of $^4C_2$ that are obscure are eradicated [8]. Furthermore, the wiring technique is less intricate, and the data in the binary form are delivered from a cell to the next cell by following the Coulomb's principle. The material comprehension of QCA in inclusive could be realized at cryogenic temperature assortment as of now [18]. In this study, a novel outline of parity generator and parity checker is presented, and based on this outline, a nano-communication architecture is formed. All these designs dissipate very low power. In Section "Briefing to 2-dot 1-electron QCA", an outline of 2-dot 1-electron QCA is presented. In Section "Proposed parity generator and checker for nano-communication", the formations of proposed parity generator, parity checker and nano-communication architecture are organized. Depleted power assessment of 2-dot 1-electron architecture is reviewed in Section "Derivation of electron's inner energy with depleted power analysis". In Section "Analysis of the outlined design", the outlined design has been studied. Later, energy and power supplies by the designs are presented in Section "Energy and power utilization for the proposed

design" and finally, in Section "Conclusion", the conclusion is thru.

Briefing to 2-dot 1-electron QCA

The outline of the cells is oblong in 2-dot 1-electron QCA, besides two dots at the two edges and single electron allowed to shift between the quantum dots of the uniform cell.

The formations of the cells per the polarities are put on display in Fig. 1. The clocking mechanism and the basic gates are discussed as follows. The design hypotheses of all 2-dot 1-electron QCA are majority gate, wires, inverter and planar crossing of wires [8] that are presented in Fig. 2.

In typical CMOS designs, clocking operates the principle of synchronization. But for QCA design, clocking operates to justify two essential requirements. QCA clocking is operated to manage the data stream direction and to empower drained signals. So, the clocking process of QCA is totally separate from traditional clocking process of CMOS. The clocking mechanism of QCA 2-dot 1-electron keeps on the related approach of 4-dot 2-electron QCA. The entire clocking mechanism is a pseudo-adiabatic procedure. QCA composition involves four basic clock segments. Each segment of QCA comprises four levels, explicitly, switch, hold, release, and relax.

The switching phase is known as raising phase. In this segment, the signal scale is amplified, and the electrons become empowered and lead to de-localize. The hold segment is typically the top phase. In this part, the signal scale is of the utmost use and the electrons attain their highest latent energy. Hence, QCA cells fully drop their polarity. In this stage, the cells are specified to achieve void phase.
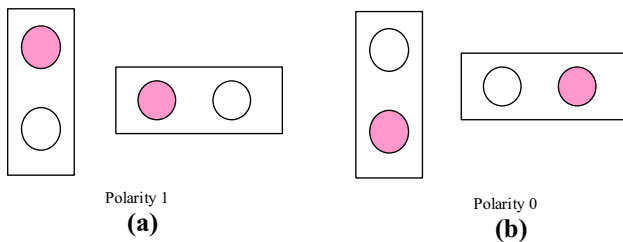

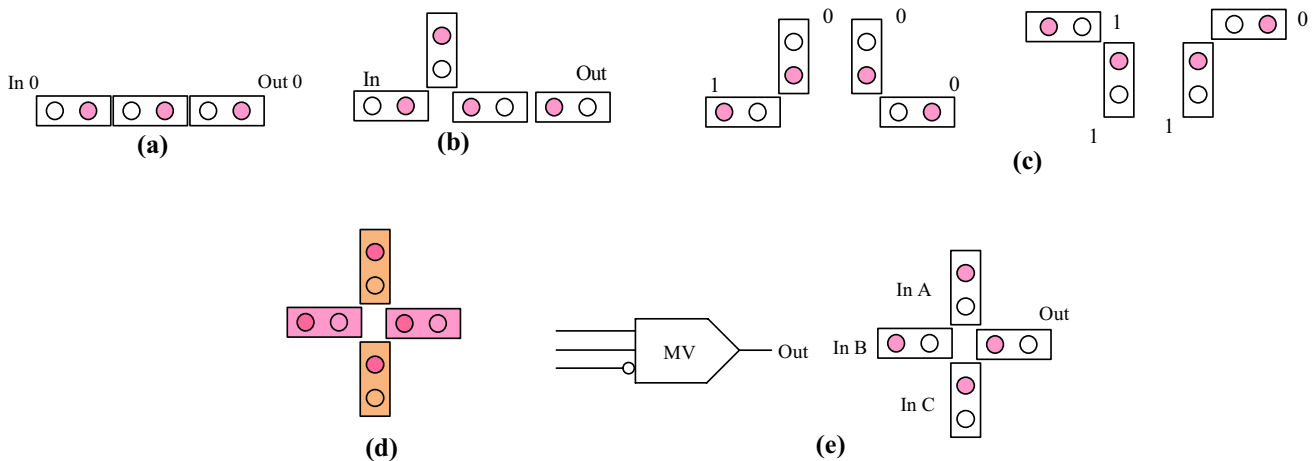**Fig. 1** Cell organization of QCA vertically and horizontally

Fig. 2 Fundamental QCA blocks; binary wires **a** 90°, **b** 45°, **c** inverted/non-inverted junctions, **d** planar crossing of wire (e) majority gate attainment

The release part is the up to a down phase. Definite computation is complete in this segment. The energy of electron begins to get inferior in this segment and the cells turn into polarized. The relaxing part is the down phase where the cells have certain polarity. Every single of the clock phases is π/2 out of phase with the succeeding clock segment as exhibited in Fig. 3. There subsist some distinct clocking mechanisms in QCA that are described earlier for separate
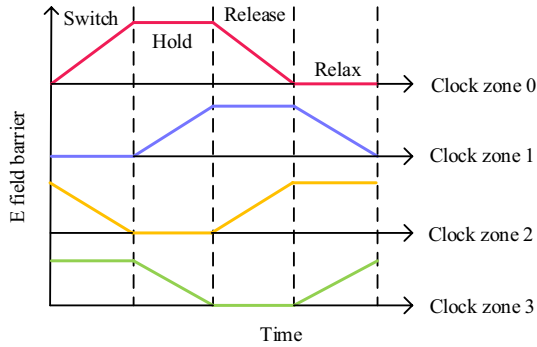
QCA systems, for instance, magnetic [3] and molecular QCA [19]. The typical color code of separate phases is presented in Fig. 3.

Proposed parity generator and checker for nano-communication

Once information is passed on from the broadcasting to the receiving point, a defect may arise. Parity perceives such defects. It is affixed to the data to be transmitted so that the figure of 1s turns into either even or odd. The even one is called even parity and odd one as odd parity. On the receiving point, the information along with the parity bit is verified; if the parity does not resemble the one referred, then a defect is spotted. The parity generator produces the parity at the broadcast point, though the checker tests out the parity at the receiving point.

The circuit diagram of the parity generator with QCA block scheme is exhibited in Fig. 4 and the truth table is presented in Table 1. Figure 5 presents the proposed circuit and block diagram of parity checker and the truth table is in
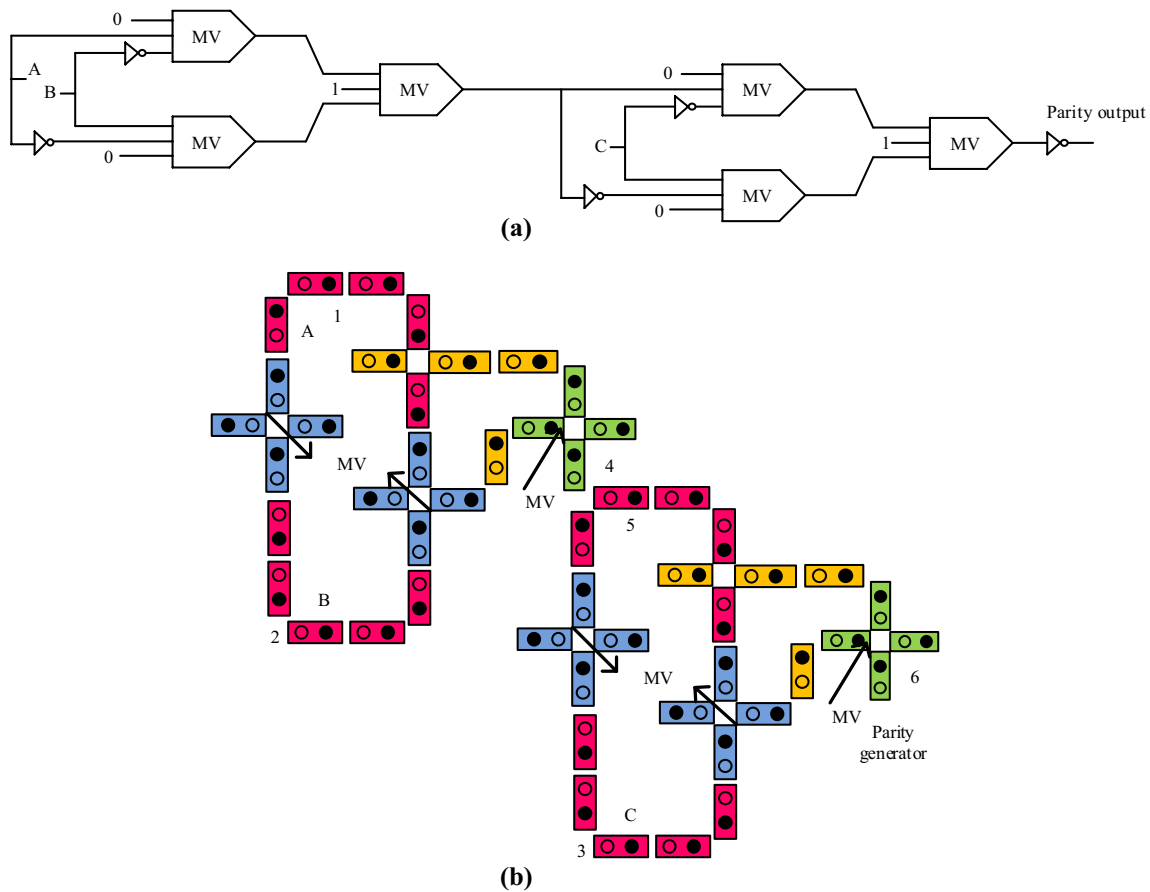

Fig. 3 Four-phase pseudo-adiabatic clocking in QCA

Fig. 4 The outlined parity generator: **a** QCA schematic; **b** QCA design

Table 1 Truth table of the parity generator

Binary input			Parity bit	
A	B	C	Odd	Even
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Table 2. Figure 6 illustrates the circuit and block diagram of a nano-communication outline with the proposed parity generator and checker circuit. The nano-communication design operates as the following procedures:

On the broadcast site, the parity generator uses the data as a key or input and produces the parity bit. The data and the produced parity bit are afterward referred through the transmission medium to their endpoint, where they are shifted within the parity checker. On the receiver end, the parity checker verifies the parity bit which was filled out inside the data for fault recognition.

An inaccuracy arises through broadcast if the parity bit out of the four bits is even, as the transferred binary data were
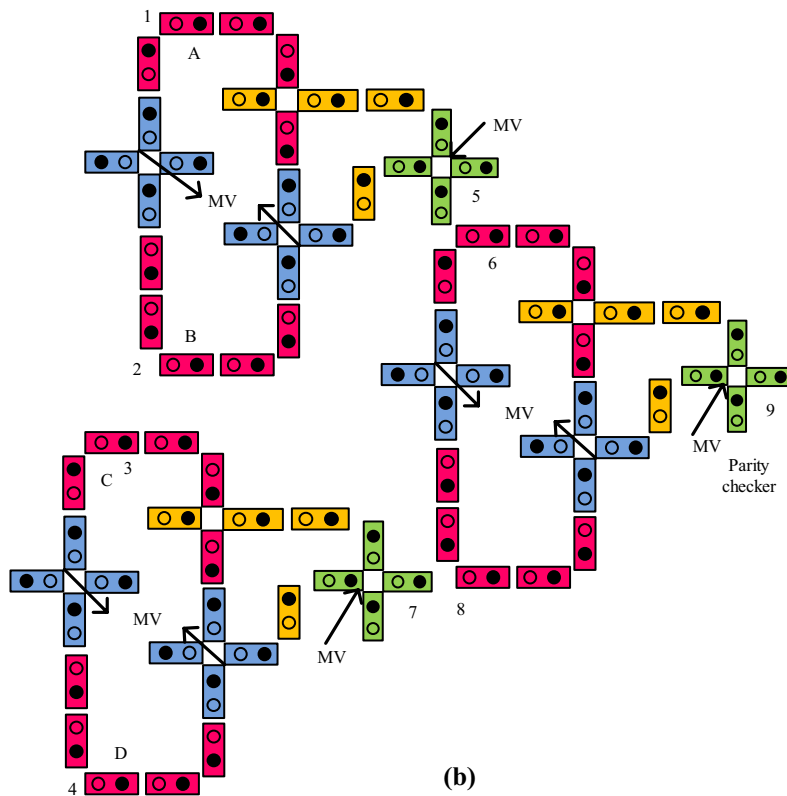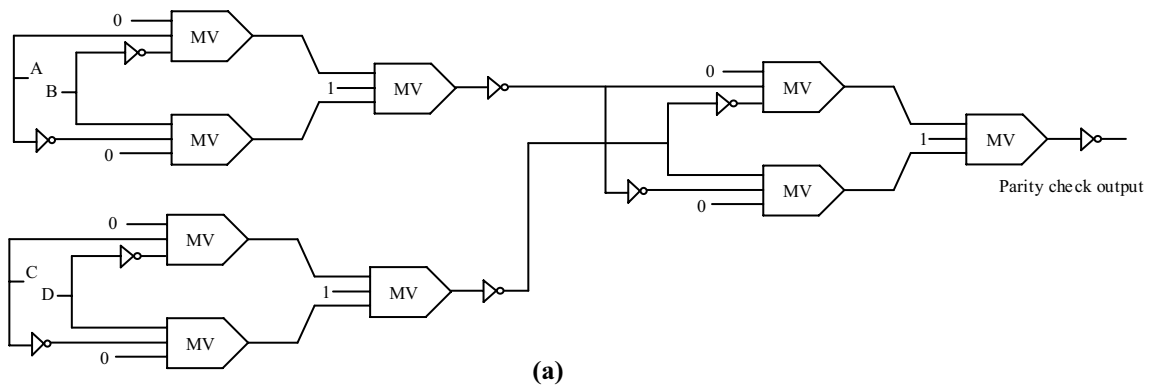

Fig. 5 The outlined parity checker: **a** QCA schematic; **b** QCA design

Table 2 Truth table of the parity checker

Binary input				Parity bit	
A	B	C	D	Odd	Even
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

formerly odd. The truth table of the outlined architecture is attained by respecting the values of the parity bit presented in Table 1. The truth table is justified in Table 3. Hence, the responses to the source of the outlined nano-communication design are similar as in Table 1 that reasons all the results of the checker bit at the receiver point to be zero. The QCA representation of the outlined architecture is presented in Fig. 6. The proposed parity generator and checker can be used in many hardware applications like small computer system interface, peripheral component interconnect or microprocessors. Besides, the circuits can be used to design nanoscale composite low-energy lossless nano-communication architectures such as nano-transmitters and nano-receivers. The proposed nano-communication design can be used as a transmission channel for secured information stream.

Derivation of electron's inner energy with depleted power analysis

From substantial properties, a 4-dot 2-electron cell with 2-electron is twice of a 2-dot 1-electron corresponding, wherein every single cell contains unique electron. In accordance with de Broglie's principle [20], an electron can be quantified as a movement of electromagnetic effects rather as a super-sited stance of waves with discrete wave magnitudes. Systematically, the Fourier illustration of a super-sited wave is presented in Eq. 1

$$\psi(u) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{+\infty} \phi(k)e^{iku} dk, \tag{1}$$

where $\psi(u)$ is the quantity of particles flowing along u direction, $\varphi(k)$ is the amplitude of the wave quantity, $k = \frac{2\pi}{\lambda}$ is the transmission frequency of an electron, λ is the wave dimension. Wave quantity can be presented through Eq. 2.

$$\varphi(k) = \int_{-\infty}^{+\infty} \psi(u)e^{-iku} du. \tag{2}$$

If $x = 0$, then electron in a 2-dot cell confined at any of the two conceivable dots. From Eq. 1, it is perceived that the charge of $\psi(u)$ is in proportion to $\varphi(k)$ multiplied by several charges of e^{iku}. Therefore, $\psi(u)$ matches the routine of a cosine wave consenting its negative value at $\frac{x}{2}$. Furthermore, this precise routine can be recognized in case of $\varphi(k)$. This parameter is termed as a probabilistic interpretation of Born [21]. In the quantum approach, the maximum regular practice is to appraise the energy as the volume of the system latent energy and the dynamic energy. Hence, the total energy is indicated here by $\vec{P}$ and reported in Eq. 3.

$$\vec{P} = \vec{T} + \vec{K}, \tag{3}$$

where $\vec{T}$ signifies the system latent energy and $\vec{K}$ represents the dynamic energy of the 2-dot QCA configuration. The incentive operator $\vec{P}$ in the point depiction $\vec{r}$ is present in Eq. 4 as attained in [22].

$$\left\langle \vec{r} \middle| \vec{P} \middle| \psi \right\rangle = -i\hbar \vec{\nabla} \left\langle \vec{r} | \psi \right\rangle, \tag{4}$$

where $\langle\rangle$ is the Dirac illustration outlining quantum settings in quantum mechanics, $\hbar$ signifies the condensed Planck's constant, $\vec{\nabla}$ is the incline operator, and i is $\sqrt{-1}$ [22]. So, $\vec{P}$ in place illustration can be stated by Eq. 5.

$$\vec{P} = -i\hbar \vec{\nabla}, \tag{5}$$

where the Cartesian ingredient of ∇ in one-dimensional plan is $\partial/\partial x$. The dynamic energy $K = -\frac{\vec{P}^2}{2m}$, where m elucidates the outline of an electron [22]. Therefore, the Hamiltonian operator can be organized in Eq. 6.

$$\hat{H} = -\frac{\vec{P}^2}{2m} + \hat{C}(\vec{r}) = -\frac{\hbar^2}{2m}\nabla^2 + \hat{C}(\vec{r}), \tag{6}$$

where ∇^2 is the Laplacian estimate with Cartesian factor in the two-dimensional plot as

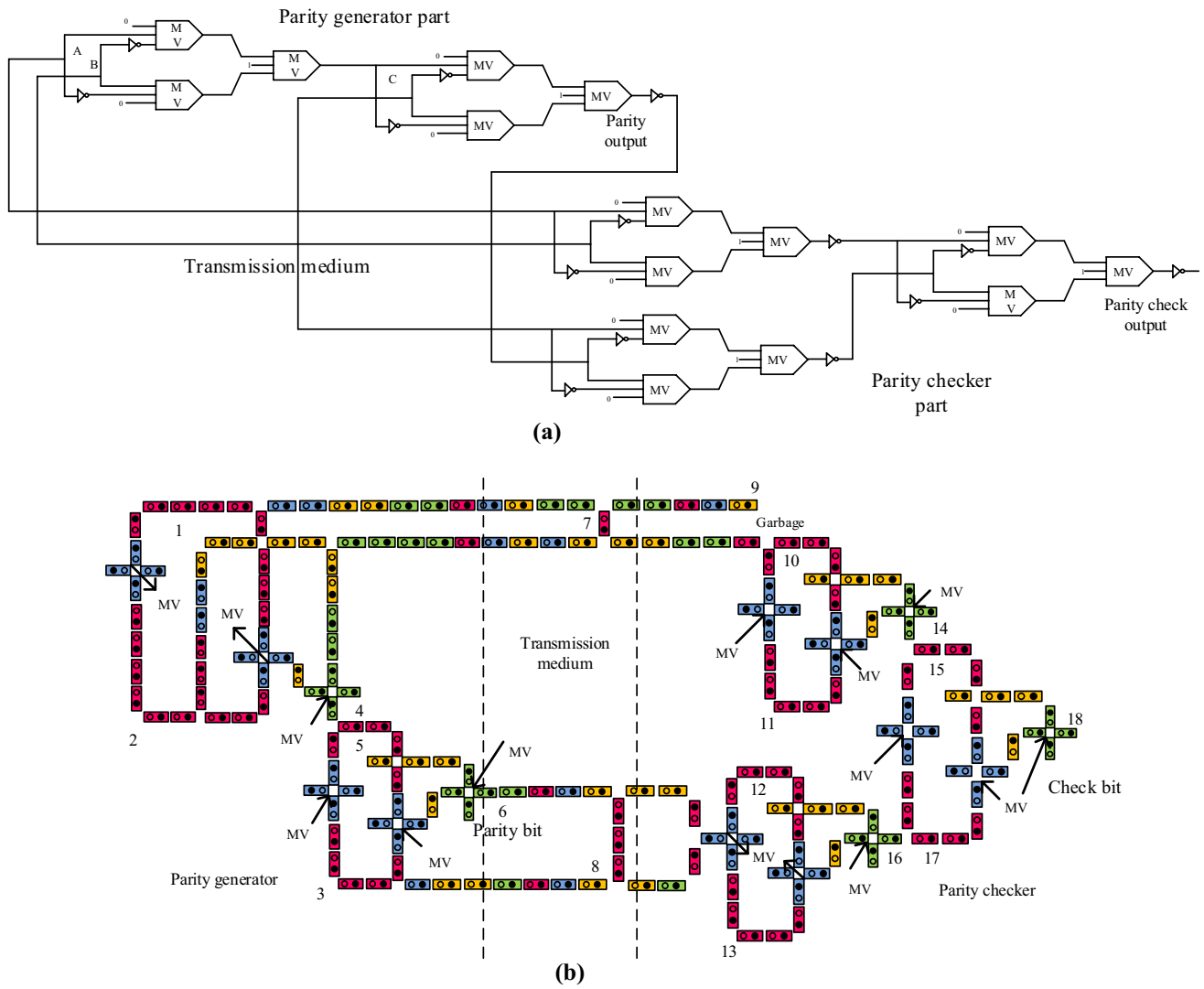$$\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial x^2}.$$

Parity generator part

(a)

(b)

Fig. 6 The outlined nano-communication design: **a** QCA schematic; **b** QCA design

Table 3 Truth table for proposed nano-communication design

Parity generator				Parity checker				
Binary input			Parity bit	A	B	C	Parity bit	Checker bit
A	B	C						
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0
0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	0	0	0
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	0	1	0
1	1	1	0	1	1	1	0	0

$\hat{C}(\vec{r})$ is the Coulomb hypothetical energy between two electrons in any two 2-dot cells m and n, apiece of which holds charge e. Hence, $\hat{C}(\vec{r})$[22] can be attained in Eq. 7.

$$\hat{C}(\vec{r}) = \frac{|e^2|}{4\pi\varepsilon_o\varepsilon_r\vec{r}}, \tag{7}$$

where ε_o is the available area permittivity and ε_r is the permittivity of the 2-dot 1-electron cell. So, the possible energy of an electron [23] because of the effect of all its neighbors is presented in Eq. 8.

$$\hat{C}(\vec{r}) = \sum_{i\neq j} e\phi(r_i) = \frac{1}{4\pi\varepsilon_o\varepsilon_r} \sum_{i=1}^{2} \cdot \sum_{j=1}^{2} \frac{e_i^m e_j^n}{|r_i - r_j|}. \tag{8}$$

So, for a 2-dot 1-electron outline holding N such cells, the overall possible energy will be organized [23] in Eq. 9.

$$\hat{C}(\vec{r}) = \sum_{m=1}^{N} \times \sum_{n=1}^{N-1} \frac{1}{4\pi\varepsilon_o\varepsilon_r} \sum_{i=1}^{2} \cdot \sum_{j=1}^{2} \frac{e_i^m e_j^n}{|r_i - r_j|} \tag{9}$$

Thus, for a particular cell, the possible energy [23] is formed in Eq. 10.

$$E_P = \frac{1}{N}\hat{C}(\vec{r}) = \frac{1}{N} \sum_{m=1}^{N} \cdot \sum_{n=1}^{N-1} \cdot \frac{1}{4\pi\varepsilon_o\varepsilon_r} \sum_{i=1}^{2} \cdot \sum_{j=1}^{2} \frac{e_i^m e_j^n}{|r_i - r_j|}. \tag{10}$$

Now, the total energy of the system is developed [23] in Eq. 11

$$E_C = -\frac{\hbar^2}{2} \sum_{j=1}^{N} \times \frac{\hat{V}_j^2}{m_j} \times \psi(\vec{r}) + \sum_{m=1}^{N} \cdot \sum_{n=1}^{N-1} \cdot \frac{1}{4\pi\varepsilon_o\varepsilon_r} \sum_{i=1}^{2} \cdot \sum_{j=1}^{2} \frac{e_i^m e_j^n}{|r_i - r_j|}. \tag{11}$$

The energy of the outline achieved from Eq. 11 marks the electrons of the cells to change throughout the channels of the specific cells.

In 2-dot QCA layout, both internal flow and external flow of power are met by each 2-dot cell. Let E_s and E_p be immediate signal energy and distinctive power energy because of feedback signal $x_i(t)$, where power assessments are arranged over the intermission $|t| < T$, where T is partial of the time gap. Then, the immediate signal energy E_s [22] can be indicated with Eq. 12

$$E_s = \lim_{T\to\infty} \int_{-T}^{+T} |x_i(t)|^2 dt. \tag{12}$$

The distinctive power energy E_p [22] can be projected with Eq. 13

$$E_p = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{+T} |x_i(t)|^2 dt. \tag{13}$$

The conjoined power and energy owing to all the feedback signals connected to the input cells can be specified in Eqs. 14 and 15, respectively.

$$E_{en1} = \sum_{i=1}^{n} E_p, \tag{14}$$

$$E_{en2} = \sum_{i=1}^{n} E_s, \tag{15}$$

where E_{en1} and E_{en2} are the power and signal energy, consistently, offered from the circumstances to the 2-dot 1-electron QCA outline, n is the figure of response lines into the circuit. This power and energy ought to increase all through the architecture and this is attained over the connection effect of 2-dot 1-electron QCA. In 2-dot 1-electron QCA, the two dots, specifically the wells, are linked by channel with a capacitor at its focus. It has an outward area A, a space between two plates is d and voltage V. Thus, the capacitance is $C \approx \epsilon A/d$, where ϵ denotes the permittivity of free area. The electric base in the gap has potency $E = V/d$. Thus, the impediment energy in the electric base [22] is presented below in Eq. 16

$$E_c \approx \frac{1}{2}CV^2 = \gamma, \tag{16}$$

where γ is the channeling energy. This energy γ is termed as barrier latent energy. An electron can move between two separate energy points if the quantity of the two quantum figures of the particular energy points is an odd number. Tunneling is not permitted if both the quantum figures are not odd numbers [22]. Therefore, minimal energy provided by a clock wave to a 2-dot 1-electron outline through N cells [22] is specified by Eq. 17,

$$E_{min} = \frac{\lceil n_{min} \rceil^2 \pi^2 \hbar^2 N}{2ma^2}. \tag{17}$$

Electron depletes a particular quantity of energy once it changes from upper energy to lower energy level. The total of energy depleted through an electron [22] will be as follows in Eq. 18

$$\nabla E = \frac{\lceil n_{min} \rceil^2 \pi^2 \hbar^2}{2ma^2} - \frac{\pi^2 \hbar^2}{2ma^2} = \frac{\pi^2 \hbar^2}{2ma^2}\left(\lceil n_{min} \rceil^2 - 1\right) \tag{18}$$

So, the minimal energy provided by the clock wave to a 2-dot 1-electron QCA [22] by N cells is shown in Eq. 19,

$$h\nu = \frac{N\pi^2 \hbar^2}{2ma^2}\left(\lceil n_{min} \rceil^2 - n^2\right), \tag{19}$$

where ν is the instance frequency of energy, n_{min} is the total number of quantum to attain the least energy to override

barrier. In Eq. 20, the power utilization in a 2-dot 1-electron QCA [22] is organized

$$P_{\mathrm{u}} = \lim_{\tau \to \infty} \frac{2}{\tau} \int_0^{\tau} |x_{\mathrm{u}}(t)|^2 \mathrm{d}t, \tag{20}$$

where $x_{\mathrm{u}}(t)$ is the functional signal amplitude. In a while, once an electron moves from upper energy to ground energy level, it depletes particular expanse of energy. The complete energy depleted by a structure [22] including N many 2-dot 1-electron cells will be organized in Eq. 21

$$h\nu_0 = \frac{N\pi^2\hbar^2}{2ma^2}\left(\lceil n_{\min}\rceil^2 - 1\right), \tag{21}$$

where ν is the depleted frequency of energy. To process the collective depleted power from an architecture of 2-dot 1-electron cell, the depleted power for each one of the cells must be assessed. The depleted power of a 2-dot 1-electron QCA is through $x_{\mathrm{d}}(t)$ being the depleted signal amplitude [22]. Equation 22 presents the depleted power of 2-dot 1-electron QCA through $x_{\mathrm{d}}(t)$.

$$P_{\mathrm{d}} = \lim_{\tau_0 \to \infty} \frac{2}{\tau_0} \int_0^{\tau_0} |x_{\mathrm{d}}(t)|^2 \mathrm{d}t. \tag{22}$$

Thus, the collective depleted power of an architecture [22] of 2-dot 1-electron QCA with N such cells is presented in Eq. 23

$$P_{\mathrm{cl}} = \sum_{d=1}^{N} P_{\mathrm{d}} \tag{23}$$

As per the theory of quantum mechanics, there endures a viewpoint of reflection from the barrier latent energy though the process energy overrides the barrier energy, i.e., $E_{\mathrm{b}} \leq N_{E_{\mathrm{c}}}$. The reflection measurement [22] can be stated as follows through Eq. 24

$$T = \frac{1}{1 + \frac{E_{\mathrm{c}}^2 N^2}{4E_s (N \times E_{\mathrm{c}} - E_s)} \sinh^2 \beta d}, \tag{24}$$

where d is the space between the capacitor slots and β is a constant. From Eq. 24, it can be realized that $T \neq 0$. Hence, permanently there is a possibility of interaction which rests on E_{c} and d. Thus, it can be obtained from Eq. 24 [22] and presented in Eq. 25

$$T = \frac{16E_s (E_{\mathrm{c}} - E_s)}{E_{\mathrm{c}}^2} \, \mathrm{e}^{-2\beta d}. \tag{25}$$

Now, it is obvious that the stand of QCA rests on the Columbic impact between electrons. A cell includes electrons with quantum dots. The situation of electron defines the status of the cell. The influence of the adjacent cells on a cell modifies the polarity of the cell. The energy also inflicts some influence on cell polarity. A weak feedback is not sufficient to polarize a cell and so the volume of energy deficit is to be provided outwardly. This energy assists the electrons to override the latent energy γ of the channel and achieve the polarity. A point is to reduce the power and energy utilization along with lessening wastage. Incidentally, a significant issue which shows a vital function is the switching rate. If the switching rate is amplified, then further energy will be essential for concise length of time. Thus, the electrode voltage needs to be static at a point. So that the switching rate becomes stable and dissipates lower energy. So, for the effective functioning of 2-dot 2-dot 1-electron architecture, the depleted energy must be minimal and the switching period must be lesser.

Analysis of the outlined design

For modifying the outputs of the proposed outline, mathematical operations are used [17], as no simulator for 2-dot 1-electron 1-electron QCA is attainable [8]. The energies for all conceivable locations of the electron in the output cell are estimated and the location with minimum possible energy is measured. Let d_0 be the space between the instant charges q_1 and q_2. Afterwards, between them, the conceivable energy [17] is as follows in Eq. 26

$$E_{\mathrm{c}} = \frac{kq_1q_2}{d_0}. \tag{26}$$

In the Eq. 26, E_{c} is the number of conceivable energies of the adjoining electrons and k is Coulomb's constant. From Eq. 26, Eq. 27 can be presented as follows

$$kq_1q_2 = 9 \times 10^9 \times (1.6)^2 \times 10^{-38}. \tag{27}$$

The overall energy of an electron [17], considering the properties of all the adjacent electrons, is shown in Eq. 28

$$E_{\mathrm{T}} = \sum_{t=1}^{n} E_{\mathrm{c}}. \tag{28}$$

The output statuses of the parity generator, checker and nano-communication architecture are presented in Tables 4, 5 and 6, correspondingly. The estimates of the conceivable

Table 4 Output position of 2-dot 1-electron parity generator

Cell	Explanations
1, 2, 3	Input cell
4	Output polarity is achieved
5	Polarity of cell 4 is achieved
6	Output polarity is achieved

Table 5 Output position of 2-dot 1-electron parity checker

Cell	Explanations
1, 2, 3, 4	Input cell
5	Output polarity is achieved
6	Polarity of cell 5 is achieved
7	Output polarity is achieved
8	Polarity of cell 7 is achieved
9	Output polarity is achieved

Table 6 Output position of 2-dot 1-electron nano-communication architecture

Cell	Explanations
1, 2, 3	Input cell
4	Output polarity is achieved
5	Polarity of cell 4 is achieved
6	Output polarity is achieved
7, 8	Transmission medium cell
9	Garbage cell
10, 11, 12, 13	Polarity of input cell is achieved
14	Output polarity is achieved
15	Polarity of cell 14 is achieved
16	Output polarity is achieved
17	Polarity of cell 16 is achieved
18	Output polarity is achieved

energies of these three designs are exhibited in Tables 4, 5 and 6 consistently.

A design is even when all the responses to a majority gate get into the access with identical force at the similar time and the output is gained in the similar or succeeding zone. The architectures in Figs. 4b, 5b and 6b assure both

the circumstances. Therefore, constancies of the outlined architectures are confirmed. Let x be the extent and y be the breadth of a 2-dot 1-electron QCA correspondingly. For the parity generator, 51 cells are essential; and for parity checker, 77 cells are needed; and nano-communication architecture required 202 cells. The spaces enclosed essentially are 51 xy nm^2, 77 xy nm^2, and 202 xy nm^2, correspondingly. We can review that the quantity of cells required for the nano-communication architecture is 202, extent enclosed is 158,908 nm^2, the overall majority gate needed is 15 and clock phases required is 8.

Energy and power utilization for the proposed design

The terminologies for the power and energy associated issues are specified in [24] and outlined in Table 7. In the table, quantum number is signified by n, the diminished constant of Plank's is specified by $\hbar$, size of the electron is m, the area is a^2, the overall quantity of cells in the layout is N and clock segments consumed are k. In the outline, $n = 10$ and $n_2 = 3$.

In Table 8, a reasonable analysis has been formulated and outlined study with 2-dot 1-electron has been assessed with the present effort using 4-dot 2-electron QCA [12, 25–42] considering the figures of cell, extent coverage and energy utilized. From [8], we acquire $x = 13$ nm and $y = 5$ nm. From Table 8, it can express that the quantity of cells needed for the 2-dot 1-electron designs is considerably fewer than that in case of their 4-dot 2-electron complements, accordingly, the area consumption also becomes lower. Besides, the energy essential to force the designs is significantly less in case of 2-dot 1-electron designs as

Table 7 Values of different factors in 2-dot 1-electron QCA

Features	Concern	Parity generator	Parity checker	Nano. architecture
$E_m = \frac{n^2\pi^2\hbar^2 N}{ma^2}$	Provided energy to the layout	1.812×10^{-18} J	2.713×10^{-18} J	4.558×10^{-18} J
$E_{dep} = \frac{\pi^2\hbar^2}{ma^2}(n^2-1)N$	Energy depletion	1.762×10^{-18} J	2.680×10^{-18} J	4.542×10^{-18} J
$v_1 = \frac{\pi\hbar}{ma^2}(n^2-n_2^2)N$	Incident frequency of energy	4.812×10^{15} Hz	7.082×10^{15} Hz	1.198×10^{16} Hz
$v_2 = \frac{\pi\hbar}{ma^2}(n^2-1)N$	Incidence of depletion energy	5.224×10^{15} Hz	7.772×10^{15} Hz	1.309×10^{16} Hz
$v_1 - v_2 = \frac{\pi\hbar}{ma^2}(n_2^2-1)N$	Variance frequency	4.120×10^{14} Hz	6.900×10^{14} Hz	2.507×10^{16} Hz
$\tau_1 = \frac{1}{v_1} = \frac{ma^2}{\pi\hbar(n^2-n_2^2)}N$	Time required to extend the quantum level	2.078×10^{-16} s	1.412×10^{-16} s	8.347×10^{-17} s
$\tau_2 = \frac{1}{v_2} = \frac{ma^2}{\pi\hbar(n^2-1)}N$	Dissipate time to arrive at lenient state	1.914×10^{-16} s	1.287×10^{-16} s	7.639×10^{-17} s
$\tau = \tau_1 + \tau_2$	Instant that cells in a clock extent needed to move to the successive polarization	3.992×10^{-16} s	2.699×10^{-16} s	1.598×10^{-16} s
$t_p = \tau + (k-1)\tau_2 N$	Time needed to proliferate thru the layout	6.564×10^{-14} s	6.547×10^{-14} s	6.448×10^{-14} s

Table 8 Reasonable analysis of nano-communication layout, parity generator and checker with two variations of QCA

Features	Outline	Cell number	Covered extent (μm^2)	Entailed energy
Nano-communication architecture	Design in [12]	275	0.410	Reasonably higher due to 550 electrons
	Design in [25]	419	0.624	Reasonably higher due to 838 electrons
	Design in [26]	4026	13.810	Reasonably higher due to 8052 electrons
	Design in [27]	4436	6.900	Reasonably higher due to 8872 electrons
	Design in [28]	Not known	4.39 (approx.)	Not known
	Design in [29]	293	0.479	Reasonably higher due to 586 electrons
	Design in [30]	382	1.020	Reasonably higher due to 764 electrons
	Design in [31]	483	0.035	Reasonably higher due to 966 electrons
	Design in [32]	679	0.035	Reasonably higher due to 1358 electrons
	Design in [33]	744	0.889	Reasonably higher due to 1488 electrons
	Proposed	202	0.158	Reasonably lower due to 202 electrons
Parity generator	Design in [29]	72	0.078	Reasonably higher due to 144 electrons
	Design in [34]	60	0.052	Reasonably higher due to 120 electrons
	Design in [35]	99	0.170	Reasonably higher due to 198 electrons
	Design in [36]	64	0.090	Reasonably higher due to 128 electrons
	Design in [37]	87	0.100	Reasonably higher due to 174 electrons
	Design in [38]	104	0.140	Reasonably higher due to 208 electrons
	Design in [39]	53	0.075	Reasonably higher due to 106 electrons
	Design in [42]	159	0.260	Reasonably higher due to 318 electrons
	Proposed	51	0.020	Reasonably lower due to 51 electrons
Parity checker	Design in [29]	130	0.143	Reasonably higher due to 260 electrons
	Design in [34]	117	0.136	Reasonably higher due to 234 electrons
	Design in [35]	145	0.280	Reasonably higher due to 290 electrons
	Design in [36]	94	0.110	Reasonably higher due to 198 electrons
	Design in [38]	214	0.436	Reasonably higher due to 428 electrons
	Design in [40]	299	0.530	Reasonably higher due to 598 electrons
	Design in [41]	84	0.080	Reasonably higher due to 168 electrons
	Design in [42]	136	0.250	Reasonably higher due to 272 electrons
	Proposed	77	0.035	Reasonably lower due to 77 electrons

the figure of electrons occupied is uniform as the figure of cells; while in case of 4-dot 2-electron outlines as the figure of electrons occupied are just the twice of the figure of cells figure and from [24], the energy requisite is precisely relational to the number of cells concerned.

Overall energy dissipation by the proposed and existing designs is presented in Table 9. Several methods have been introduced so far to find energy dissipation by any QCA circuit. Most familiar are QCADesigner-Energy [43], QCAPro [44, 45] and Power Consumption by Hamming distance [46].

Conclusion

The architecture of parity generator and checker is organized in this study and based on these layouts, a nano-communication transmission channel is proposed using 2-dot 1-electron QCA. Because of the unavailability of a 2-dot 1-electron QCA simulator, potential energy resolution technique based on Coulomb's revulsion theory has been applied to determine the outputs. The outlined layouts are studied properly and then the overall essential energy depletion is analyzed. It is presented that the proposed design dissipates very low energy. From the layouts, it is coherent that the 2-dot 1-electron QCA parity generator, checker and nano-communication architecture are considerably more proficient

Table 9 Power depletion comparison by the proposed and existing designs

Design	Outline	Overall energy depletion (meV)
Nano-communication architecture	Design in [12]	778.60
	Design in [25]	567.80
	Design in [26]	Not known
	Design in [27]	2092.84
	Design in [28]	1348.80
	Design in [29]	781.00
	Design in [30]	687.80
	Design in [31]	722.00
	Design in [32]	1302.60
	Design in [33]	898.80
	Proposed	2.84×10^{-5}
Parity generator	Design in [29]	329.80
	Design in [34]	239.20
	Design in [35]	237.20
	Design in [36]	241.20
	Design in [37]	359.78
	Design in [38]	0.56994
	Design in [39]	389.40
	Design in [42]	931.40
	Proposed	10.99×10^{-6}
Parity checker	Design in [29]	479.60
	Design in [34]	419.20
	Design in [35]	479.20
	Design in [36]	358.80
	Design in [38]	1.11543
	Design in [40]	690.87
	Design in [41]	210.20
	Design in [42]	961.60
	Proposed	16.72×10^{-6}

regarding size and power depletion than the identical with 4-dot 2-electron QCA.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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