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ORIGINAL ARTICLE

A novel efficient full adder–subtractor in QCA nanotechnology

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Abstract
Quantum-dot cellular automata (QCA) is a new nanotechnology which facilitates computation paradigms with extremely low energy dissipation. In this paper, a novel efficient full adder–subtractor in QCA nanotechnology is proposed. First, one bit full adder with minimum delay cell is designed. Then the proposed full adder is used to design an efficient full adder–subtractor with minimum number of cells. The proposed circuit does not need any rotated cells and only uses one layer. Therefore, manufacturability of the design significantly improves. In addition, our design achieves 44 cell in full adder and only 83 cell in full adder–subtractor. The proposed full adder–subtractor only occupies 0.09 μm^2 area.

Keywords Full adder-subtractor · Quantum-dot cellular automata · Delay · Energy dissipation

Introduction

The size of CMOS transistors keep shrinking to increase the density on chip in accordance with Moore's Law. The scaling affects the device performance due to constraints like heat dissipation and power. Quantum dot cellular automata (QCA) technology is one such alternative, that can overcome the scaling issue and offer high frequency up to terahertz, high density, and low power consumption. On the other hand, current transistor-based IC fabrication technology faces many trivial issues such as those of excess power dissipation, expensive fabrication and short channel effects at very low device size.

To overcome the limitations of CMOS technology, quantum cellular automata (QCA) which is a solid-state nanoelectronic technology is developed as a possible alternative to conventional CMOS circuits [1]. The processing of data in a quantum cellular automata is based on a columbic transcription between similar cells. Each of these cells consists of four–six electron locations (quantum dot), which are connected to each other through tunneling junctions.

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The design of computing circuits in QCA technology has always been the focus of attention in the past years [2, 3]. A large number of circuits, such as adders and multipliers, have been presented in 4–6. In this paper, a new structure for full adder will be proposed. Then, we will provide a full adder–subtractor circuit based on the resulting circuits. All circuits are designed in one layer and will be optimized for the structure and number of cells. Each circuit uses two XOR gates and a majority gate as the main components, and the full adder–subtractor circuit has only one more majority gate. Finally, QCA Designer software will be used to evaluate the accuracy of circuit's functioning and also power analysis will be done by QCAPro software.

Adder implementation

Imagine a full adder with three inputs (A, B, and C). The C input will act as the carry bit which is transferred from the previous stage. The implementation function of a full adder is as follows:

$$\text{Sum} = A \oplus B \oplus C, \tag{1}$$

$$\text{Carry} = AB + AC + BC. \tag{2}$$

As can be seen from (1) and (2), each full adder has two outputs (Sum and Carry) and the Sum output is the result of XOR of circuit inputs. According to (2) it should also be noted that carry can be defined as an output of 3-input majority gate (with A, B and C as its inputs). Hence, we

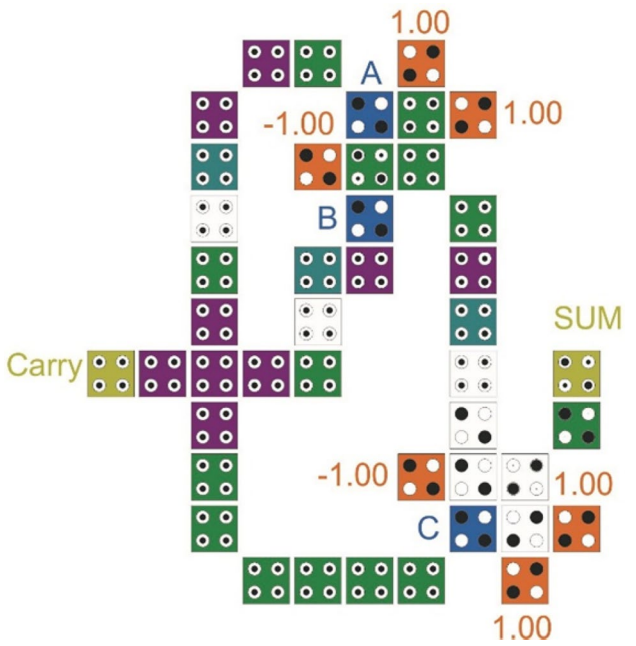

Fig. 1 Implementation of the proposed full adder in QCA technology

Table 1 QCA full adder comparison

Design	Number of cells	Area (μm^2)	Latency (clock cycles)	Layer type
[4]	79	0.05	1.25	Multilayer
[5]	71	0.06	1.5	Coplanar
[6]	102	0.09	2	Coplanar
Proposed	44	0.06	1.25	Coplanar

can design an optimal full adder in QCA technology with this simple reason. The implementation of this full adder is shown in Fig. 1. This figure shows that the occupied space and the used cells in the proposed circuit are fewer than the circuits using only three-input and five-input majority gates.

Table 1 shows the results related to the comparison of a few optimal full adders and the proposed circuit. According to this table, we can conclude that the proposed structure is an optimal circuit in terms of occupied space and the number of cells (while it has a standard delay) in comparison to other circuits. In addition, it should be mentioned that the proposed full adder is designed in coplanar method and has an acceptable delay. As can be seen from Fig. 1, the proposed design can be generalized to more bit full adder design in the coplanar method. This is another advantage of the proposed full adder.

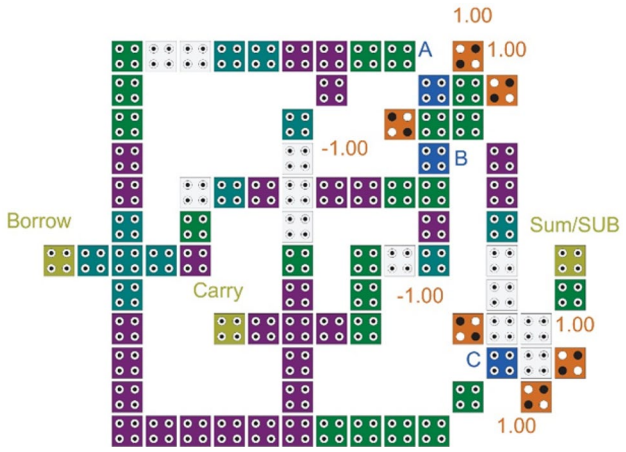

Fig. 2 The proposed circuit for full adder–subtractor in QCA

Table 2 QCA full adder–subtractor comparison

Design	Cells	Area (μm^2)	Latency	Layer type
[7]	186	0.132	2	Multilayer
[8]	90	0.11	1	Coplanar
[9]	228	0.4	1.5	Coplanar
Proposed	83	0.09	1.5	Coplanar

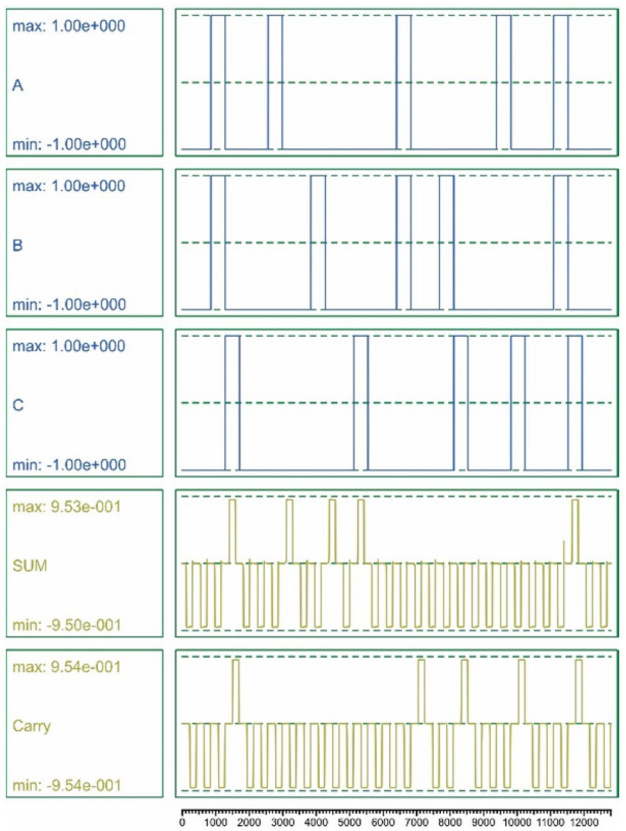

Fig. 3 Result of the full adder circuit

Implementation of full adder–subtractor

A full subtractor circuit composed of three inputs like the full adder. Sub and Borrow outputs of full subtractor are as follows:

$$\text{Sub} = A \oplus B \oplus C, \tag{3}$$

$$\text{Barrow} = \bar{A}B + \bar{A}C + BC. \tag{4}$$

Since the Sub output of full subtractor is the same as Sum in full adder [see (1) and (3)], implementing full adder–subtractor circuit in one integrated structure will be reasonable. Again it should be mentioned that from (2) and (4) to generate Carry and Borrow we need a majority gate. Since both circuits have the same inputs and use the majority and similar XOR gates, it is possible to design an integrated circuit for both operations. Therefore, in this section, a new full adder–subtractor structure with minimum quantum cells will be introduced. Figure 2 shows the implementation of the proposed circuit. As it is obvious in the figure, this circuit makes use of all gates in the proposed adder. Although inverter gate and one majority gate are added to the circuit, it is more efficient in comparison to other circuits in terms of number of cells and area consumption.

The accuracy of the above issues is shown in Table 2. In this table, number of cells, area and delay of the proposed circuit has been compared with previous full adder–subtractor circuits. As can be seen, the proposed full adder–subtractor has fewer number of cells, smaller area with good delay performance in comparison with related works.

Simulation and results

In this paper, we presented an optimal design for some computational circuits in QCA technology. Initially, a one bit full adder circuit was presented and its accuracy was evaluated by QCA Designer software. It should be mentioned that to have proper performance for proposed circuit, input C should be applied to circuit one cycle later than A and B inputs in both full adder and full

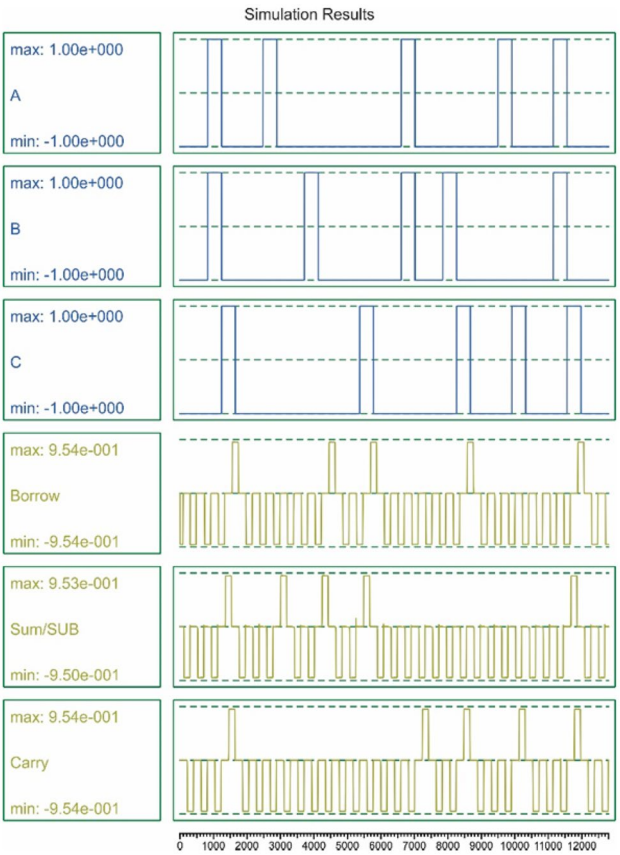

Fig. 4 Result of the full adder–subtractor circuit

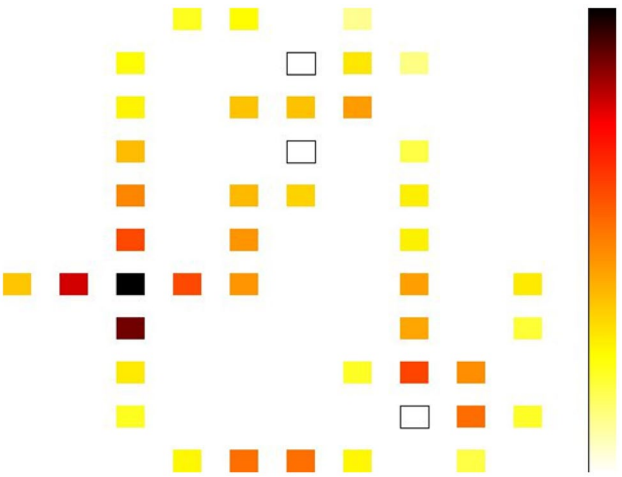

Fig. 5 Energy diagram of proposed full adder

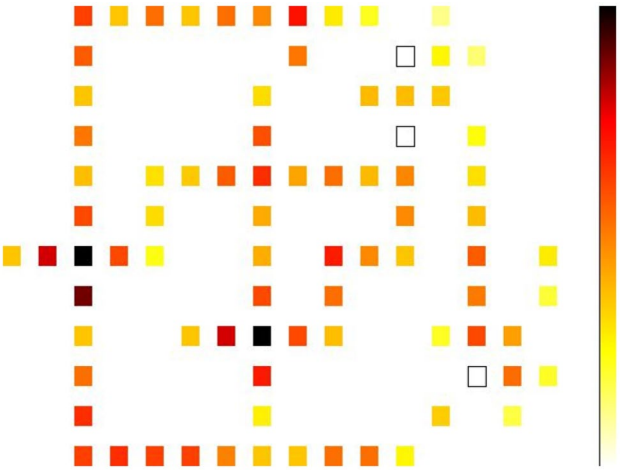

Fig. 6 Energy diagram of proposed full adder–subtractor

Table 3 Average leakage energy dissipation and average switching energy dissipation of proposed designs for different E_k

Design	Average leakage energy dissipation (eV)			Average switching energy dissipation (eV)		
	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
Proposed full adder	0.018	0.046	0.077	0.037	0.031	0.026
Proposed full adder–subtractor	0.029	0.084	0.144	0.100	0.085	0.071

adder–subtractor design. Figure 3 shows the result of the full adder circuit. Figure 4 shows the accuracy of the proposed full adder–subtractor circuit. The input diagram of these two circuits are tested and evaluated in all forms via the vector table. This shows that the proposed circuits will have a better performance for computational purposes. According to the results obtained, we can conclude that the proposed circuits have a better performance in comparison to single layer circuits offered in other studies and it is also able to compete with multilayer circuits. In addition, simulations are done by QCAPro software to evaluate the energy dissipation of proposed designs. Figure 5 shows energy diagram of the proposed full adder of Fig. 1. In addition, Fig. 6 sketches the energy diagram of the proposed full adder–subtractor of Fig. 2. In these figures, darker points show nodes with higher energy dissipation. In addition, amount of switching energy and leakage for different E_k (kink energy) are abbreviated in Table 3.

Conclusion

In this paper, we have proposed a full adder–subtractor in a single layer based on QCA technology. Our proposed designs are competitive with coplanar and multilayer design and have fewer delay cells with reasonable delay.

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