HARDWARE Implementation of Step-Switched SVCs to Correct Power factor and Mitigate Harmonics for Large DC Variable Loads

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Abstract The objective of this paper is to develop and implement a complete system for reactive power compensation in railways or high DC power consuming industries. Very high current harmonics are generated, when AC supply is converted to DC to run DC machines, e.g., railway locomotives. Generally, for such applications, static VAr compensators (SVC) are used in combination with passive harmonics filters for mitigating different orders of harmonics. By default, such systems take power factor to high leading side, which must be corrected. To achieve acceptable results, manufacturers switch large inductors and feed chopped voltage waveform to achieve required inductive reactive power to compensate the leading reacting power present at any time in the SVC. This is done at high voltage using thyristors or GTOs, i.e., 11 kV or 33 kV. It is technically a complicated, very expensive technology and needs highly skilled engineers to run and maintain such system. Looking at those problems, better, reliable and technically superior solution is developed to give desired results at much reduced cost. A hardware prototype is developed for 433 V, three phase, 20 A load to obtain satisfactory experimental results.

Keywords Harmonic · Harmonics filters · High voltage · Reactive power compensation · Static VAr compensators

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Introduction

The load of DC power consuming equipment like railway locomotives, electrolysis, DC welding, etc. is of very fast variable nature. Most of these loads in power system are nonlinear and create harmonics, poor voltage regulation, low PF and high reactive power demand. Normally, the PF of power electronics equipment is very low with very high current harmonics [1–4]. Due to large variation in current of such loads, create very fast changes in reactive power. Looking at those problems, better, reliable and technically superior solution is developed to give desired results at much reduced cost. An active filter or dynamic static compensator (DSTATCOM) is used to maintain PF and for mitigation of harmonics. However, due to very large reactive power demand, the essential rating required of the voltage source converter (VSC) working as active filter or DSTATCOM increases significantly, resulting in very high capital investment. Even though there are combinations used called hybrid filters [5–10], usually the parallel combination of a shunt connected passive filters with active filter or DSTATCOM for such type of loads are preferred to reduce the rating of the single active filter. In such type of techniques, dominant harmonics are absorbed by passive filter and a part of reactive power compensated by DSTATCOM and bulk by passive filter. However, DSTATCOM is more complex, to control and costlier than SVC considering the same power rating. Such systems work satisfactorily for low and medium voltages. So, further investigation is required to find relatively simpler and economic solution with SVC [11–16].

The proposed SVC system is designed in such a way to avoid problems like self-generated harmonics, which happens in conventional SVC's technology. Due to switching at HV, the cost of conventional SVCs is very high. To

fulfill objective, the system HV is stepped down to a workable low voltage of 433 V, 600 V and 750 V from HV, where commonly available switching devices can be used. Passive harmonics filters of desired capacity to mitigate particular orders of harmonics present in the network are installed. Passive filters have unwanted side effect of taking the whole PF on leading side, which needs to be de-compensated to bring it near to unity. To achieve this goal, adequate reactors are required. It is convenient to divide a single large reactor into a number of reactors each of small rating. This allows use of low voltage and current rated thyristors, which are easily available in Indian market. Thyristors are used to switch reactors ON/OFF to fully compensate the capacitive energy at a very fast rate at zero crossover. The proposed methodology has low capital and maintenance cost which is about 40%–50% of conventional SVCs.

Prototype Design

To validate the results, a prototype for this model is developed at 433 V, 3- ϕ with 20 A load connected via variable frequency drive (VFD). In this paper, 6-pulse VFD is used to generate required frequencies to supply the load. VFD contains bridge rectifier, DC link and inverter for desire operation. The bridge rectifier/inverter convert AC/DC or DC/AC by desired switching of devices and at any instant only two devices are in conduction one from upper group and another from lower group. The output of rectifier or at the DC side contains only ripples having six times of fundamental frequencies as given in below equation

$$h = n \times p \quad (1)$$

where p is number of pulses, n is integer and h is the order of harmonics. The harmonics at DC side are of 6, 12, 18, 24 and so on. Most of the rectifier based loads are having symmetrical waveform (except half wave rectifier) especially for even harmonics, which means positive half is a mirror image of negative half, so all are cancel out. The rms value of the h th order harmonic in DC voltage is given by:

$$V_h = V_{do} \frac{\sqrt{2}}{h^2 - 1} [1 + (h^2 + 1) \sin^2 \alpha]^{1/2} \quad (2)$$

where V_{do} is the average maximum DC voltage across the converter, α is the firing angle. The output voltage V_d of the converter consists of a DC component and a ripple whose frequency is determined by the pulse number. Due to the cancellation of even harmonic or ripple, will leave only odd harmonics at AC side, the order of AC harmonics is 5, 7, 11, 13 and higher. Here, fifth and seventh are predominating and further improvement in harmonics order's magnitude drops quickly. The harmonics

contained in the current waveform at AC side are of the order given by Eq. (3). The input current waveform in one phase of bridge rectifier as shown in Fig. 1.

$$h = n \times p \pm 1. \quad (3)$$

The fundamental (I_1) and rms (I) value of current is given by Eqs. (4) and (5)

$$I_1 = \frac{1}{\sqrt{2}} \frac{2}{\pi} \int_{-\pi/3}^{\pi/3} I_d \cos \theta \cdot d\theta = \frac{\sqrt{6}}{\pi} I_d \quad (4)$$

$$I = \sqrt{\frac{2}{3}} \cdot I_d. \quad (5)$$

The rms value of h th harmonics current is given by Eq. (6)

$$I_h = \frac{I_1}{h} \quad (6)$$

The Electricity Board has also imposed regulations on generation of harmonics by the consumer for maintaining pollution free distribution at point of common coupling (PCC). In addition, Electricity Board consider only input side harmonics at PCC so the design of filters or desired solution according to input side measurement only [17–25]. This paper discusses a model of parallel combination of shunt connected passive filters and TCR. The system has two basic problems first is high leading PF due to capacitors in the filters and second is high harmonics. To improve PF and minimize harmonics, TCR and passive filters are used. The hardware of proposed scheme and its circuit diagram are shown in Fig. 2 and in Fig. 3, respectively.

Control and Design of TCR

In the previous publication [26], a case study of 25 kV, 1- ϕ railways for design and control of passive filters and step-switched TCR for are discussed and proposed by using

Fig. 1 Input current waveform in one phase of bridge rectifier

Fig. 2 A prototype for system

Fig. 3 System circuit diagram

MATLAB simulation. In this article, a hardware prototype by using same of switching control of TCR is developed in an industry to validate the previous publication results obtained from MATLAB.

The designed TCRs de-compensate the capacitive currents taken by filters. At no load, the system requires 12 kVAR (inductive) for full compensation of capacitive

power. Here, only four switchable inductors connected in parallel with load are 8 kVAR, 4 kVAR, 2 kVAR and 1 kVAR taken. This is a binary method of using inductors with best resolution to maintain a target PF in between 0.95 and 0.99 lagging. The TCR branch inserts in steps as per the kVAR requirement so no variations in firing angle are required

Fig. 4 Sensors and APFC relay

Fig. 5 Thyristor firing circuit diagram

Fig. 6 PCB, thyristors with heat sink and APFC relay **Fig. 7** Input current waveform with THDi

due to 180° firing angle, so self-generated harmonics are not generated at system input.

The voltage and current are measured by potential and current transformer and output is given to automatic power factor correction (APFC) relay decides, which shunt branches of TCR will be active. The APFC's in-built program calculates and generates actuating signals to match the leading or lagging reactive power present and fire required TCR branch accordingly in the network as shown in Figs. 4 and 5. This model is capable of

compensating low PF independently and automatically within a very short time period of one second. The PCB layout for firing circuit of TCR with APFC relay is shown in Fig. 6.

System Performance: Experimental Results

Power quality and its data analysis performed and all readings were taken at 100%, 50% and 25% of full load.

Measurements with Only Load

The measurements have been taken, when system is connected with nonlinear load via VFD only. The following points have been observed:

1. The measured THDi is about 25%–28% as shown in Figs. 7 and 8, PF is varying from 0.45 to 0.15 lagging, and all predominating harmonics are high as given in Table 1.
2. The THDv of input voltage is within recommended level as shown in Fig. 9. The maximum of 4500 VAR leading reactive power is required to compensate lagging reactive power as shown in Fig. 10.

Table 1 Measured parameters when connected with load

Particular	Percentage in all phases			Load condition	Power factor	Total wattage
	R phase	Y phase	B phase			
Third	6.1	4.6	5.8	Full load	0.45 Lag	2292.6 W
Fifth	24.1	23.2	22.8			
Seventh	11.2	12.4	11	Half load (H.L)	0.24 Lag	1076.2 W
Ninth	0.9	0.9	0.5			
Eleventh	2.7	2.1	2.2	Partial H.L	0.15 Lag	709.6 W
Thirteenth	1.1	1.2	1.2

Fig. 8 THDi measurement

Fig. 9 Input voltage with THDv

Measurements When System is Connected with Load and Passive Filters

In this case, the following points have been observed:

1. The THDi is also reduced from the range of 25%–28% to 8% (approx.) as shown in Figs. 11 and 12. The THDi level can be further reduced by better fine-tuning of passive filter.
2. The current magnitude in supply is now increased from 7 to 15 A to fulfill the demand of passive filters as shown in Fig. 13.

3. The measured PF is varying from 0.34 to 0.11 leading and all predominating harmonics are below 5% as given in Table 2.
4. The system required leading reactive power of 9300 VAR to 10,000 VAR due to passive filters to compensate as shown in Fig. 14. This 10 kVAR value is variable and changes at very fast rate. The TCRs of 8 kVAR, 4 kVAR, 2 kVAR and 1 kVAR are controlled by APFC relay working in the intelligent mode and it selects the right combination of reactors to maintain the PF near to unity.

4.3. Measurements When System is Connected with Passive Filters and TCRs

At this case, the following points have been observed:

1. The current in supply is now again decreased from 15 to 7A and the total current THDi is maintained below 7% as shown in Figs. 15 and 16.
2. The inductive reactive power required for the system is now decreased from 10 kVAR to 400 VAR as shown in Fig. 17.
3. PF is varying from 0.97 to 0.96 lagging as shown in Fig. 18, and all predominating harmonics are below 3% as given in Table 3.

Fig. 10 Reactive power demand

Fig. 11 Input current with THDi

Comparison of Available Technologies for Compensation in DC Variable Load at HV

At present, there are three major technologies available to compensate reactive power and mitigate harmonics for DC variable load at HV specifically, conventional, active and hybrid methods. The comparison chart for all three with proposed method based on performance and cost-effectiveness is given in Table 4.

The active methods use VSC or DSTATCOM only; hybrid methods combine a passive device and DSTATCOM and in conventional methods, which practices passive, means and SVC. All the required specifications of the components to implement the hardware for proposed

Fig. 12 Input current THDi variation with passive filter

Table 2 Measured parameters with passive filter

Particular	Percentage in all phases			Load condition	Power factor	Total wattage
	R phase	Y phase	B phase			
Harmonic order						
Third	1.7	2.2	4.2	Full load	– 0.11 Lead	3417.5 W
Fifth	4.5	3.7	4.1			
Seventh	3.9	3.8	3.2	Half load (H.L)	– 0.20 Lead	2014.8 W
Ninth	0.5	0.4	0.9			
Eleventh	3.1	4.2	5.1	Partial H.L	– 0.34 Lead	1039.6 W
Thirteenth	2.7	3.8	3.5

Fig. 13 FFT analysis for harmonics

methods are given in Table 5. All the practices and recommended levels for harmonics are according to the IEEE standards [28, 29].

Fig. 15 Input current with THDi

Conclusion

At HV, the active methods suffer from high kVA rating, more switching losses and high cost; hence, hybrid systems are developed but still required research to reduced complexity and cost. The conventional SVCs are stagnant major concern and used for reactive power compensation at

Fig. 14 Reactive power demand

Table 3 Measured parameters when passive filter and SVC are connected

S. No.	Particular Harmonic order	Percentage in all phases			Load condition	Power factor	Total wattage
		R phase	Y phase	B phase			
1	Third	1.1	1.2	1.6	Full load	0.97 Lag	3238.4 W
2	Fifth	1.5	1.9	2.1			
3	Seventh	2.1	1.8	2.5	Half load (H L)	0.97 Lag	2182.1 W
4	Ninth	0.3	0.3	0.5			
5	Eleventh	1	1	1.4	Partial H L	0.96 Lag	1217.5 W
6	Thirteenth	1.3	1.5	1.9

Fig. 16 Input current THDi variation with passive filter and TCR

HV. The comparison of all available technologies based on cost and performance has been discussed. The proposed SVC system prototype has given desired results. Those give consistent results for very long time. Breaking up a single large inductor into many small inductors is a unique idea and works very satisfactorily. All passive harmonic filters are connected on HV side and step down transformer is used to bring down the voltage to 433 V, where small rated inductors or reactors are switched as per the requirement. This has done to avoid switching of one single large reactor by applying chopped voltage waveform. This is the main criterion behind reducing the complexity and heavily economizing the entire project. There is huge

saving in the initial cost with minimum maintenance and no dependency on the manufacturer. This type of cost-saving scheme is beneficial and easily acceptable by developing country like India. The proposed SVCs use small rating inductors in parallel instead of single large inductor, which are much closed together in terms of their value. The firing of each thyristor at zero crossing makes a harmonics free system, which is produced by SVCs itself. Also, it maintains PF very smoothly as similar to continuous firing. This scheme of firing is as good as continuous firing for PF correction.

Fig. 17 Reactive power demand

Fig. 18 Improved power factor

Table 4 Comparison of available technologies for compensation in DC variable load

Method	Required solution	Purpose	Cost	Remark
Active method	DSTATCOM: Shunt connected	For harmonics mitigation as well as for reactive power compensation	Highest among all method The cost of DSTATCOM is 5–6 times of the passive filters of same rating	Implementation of active filter at HV is extremely cost ineffective and usually preferred for low or medium voltages Power rating is a major limitation because switches withstand only few kV Series/parallel combination is also possible for switches but difficult to implement and cost ineffective Difficulty in high switching frequency of devices for fast and dynamic compensation at HV Maintenance cost and HV switching losses are high HVs switching becomes problematic and very costly Required high kVA rating DSTATCOM and size also increase proportionally [27]
Hybrid method	Passive filters DSTATCOM: Shunt connected	For harmonics mitigation as well as maximum required reactive power compensation Only for minimum required reactive power compensation	Higher than conventional methods and lower than active methods	It is a trade-off between filter performance, rating, cost and size kVA rating of DSTATCOM as well as initial cost is reduced [27] DSTATCOM only used for minimum required reactive power compensation in the system at HVs DSTATCOM maintenance cost is high and every time dependence on engineer from manufacturer is essential For developing countries like India, importing such technology is very costly
Conventional method	Passive filters TCR: Single reactor	For harmonic mitigation Supplying required reactive power to improve PF	Higher than proposed method, in this paper A conventional SVC of about 15 MVar rating cost amount \$ 46,000 approximately	Require HV switching of capacitors and inductors need expensive technology HV switching technology is only with few companies and hence is protected Due to single reactor of large size delays in turn on and commutation time of power switches High capital & maintenance cost At the time of fault, dependence on manufacturers, engineers, services is required Still conventional SVCs are preferred in India due to availability

Table 4

Proposed method	Passive filter TCRs: instead of single reactor, use of different small reactors in parallel	Mitigation of harmonics very satisfactorily Reactive power compensation The required HV like 11 kV or 33 kV, etc. reduced to convenient working voltages of say 33 V, 600 V and 750 V	Lowest among all The capital cost is about 40%–50% of conventional SVCs	Voltage rating of switching devices (TCR) is reduced hence easy to handle Lower voltages are very easy to handle and the devices are easily available in local markets, so no premium cost for HV switching devices is needed Several parallel reactors of smaller ratings in TCRs instead of high rating single large reactor reduce the cost Low capital and maintenance cost All components are easily available indigenously with known technology End users trained engineers can carry out regular maintenance without support of manufacturer
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Table 5 Specification of components for hardware implementation

S. No.	Component	Rating
1	Voltage source	433 V, 3- ϕ
2	Source inductance	6 mH, 3- ϕ
3	CT_R, CT_Y, CT_B	100/5 A
4	MCB, 3- ϕ	20 A-02 nos., 16 A-01 nos
5	L_5	4 mH, 3- ϕ
6	C_5	103 μ F for each phase
7	L_7	4 mH, 3- ϕ
8	C_7	52 μ F for each phase
9	$L1_{SVC}$	43 mH, 8 kVAr, 3- ϕ
10	$L2_{SVC}$	86 mH, 4 kVAr, 3- ϕ
11	$L3_{SVC}$	170 mH, 2 kVAr, 3- ϕ
12	$L4_{SVC}$	346 mH, 1 kVAr, 3- ϕ
13	VFD	3- ϕ , 5.5 KW, 3 H.P, 433 V, 11.2 A
TCR firing scheme component rating		
14	R_1, R_7	47 k Ω
15	R_2	220 Ω
16	R_3, R_6	10 Ω
17	R_4	2.2 Ω
18	C_1	680 pF
19	C_2	1000 μ F, 25 V
20	Darlington pair (Q)	TL 188
21	APFC relay	14 step

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