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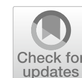

Optimization of Transistor Characteristics and Charge Transport in Solution Processed ZnO Thin Films Grown from Zinc Neodecanoate

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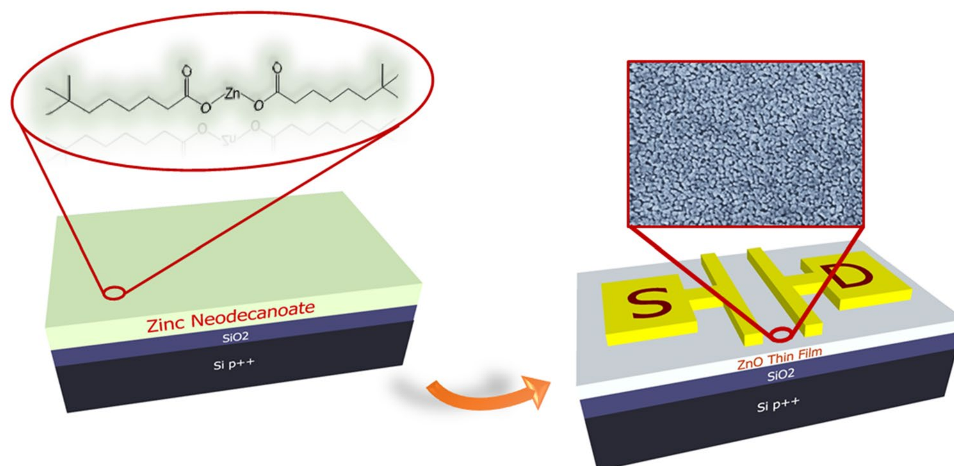
Abstract
Solution processing of metal oxide-based semiconductors is an attractive route for low-cost fabrication of thin films devices. ZnO thin films were synthesized from one-step spin coating-pyrolysis technique using zinc neodecanoate precursor. X-ray diffraction (XRD), UV–visible optical transmission spectrometry and photoluminescence spectroscopy suggested conversion to polycrystalline ZnO phase for decomposition temperatures higher than 400 °C. A 15 % precursor concentration was found to produce optimal TFT performance on annealing at 500 °C, due to generation of sufficient charge percolation pathways. The device performance was found to improve upon increasing the annealing temperature and the optimal saturation mobility of 0.1 $cm^2 V^{-1} s^{-1}$ with I_{ON}/I_{OFF} ratio ~ 10^7 was achieved at 700 °C annealing temperature. The analysis of experimental results based on theoretical models to understand charge transport envisaged that the grain boundary depletion region is major source of deep level traps and their effective removal at increased annealing temperature leads to evolution of transistor performance.

Graphic Abstract
Single-step spin coating-pyrolysis synthesis of ZnO thin films from non-aqueous precursor zinc neodecanoate has been investigated for transistor applications.



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Keywords Zinc oxide · Thin film transistors · Solution processing · Zinc neodecanoate

1 Introduction

Over the past 15 years, the area of oxide semiconductors has caught increasing attention for applications in the domain of large area electronics, flexible electronics and flat panel displays [1]. This has been mainly driven by the superior properties of oxide semiconductors compared to its conventional inorganic counterparts like a-Si:H [2, 3]. Among various oxide semiconductors, zinc oxide (ZnO) in particular has seen tremendous interest due to its versatile properties. Being a direct bandgap semiconductor with a wide-bandgap of ~ 3.3 eV, it is transparent to visible light [4, 5]. Additionally, its nontoxicity, high electron mobility and stability makes it an attractive candidate for a variety of functional applications [5, 6]. Moreover, its suitability as matrix material for doping with number of elements such as aluminium [7], indium [3, 8–11], gallium [3, 9, 10], tin [11–13], magnesium [14] allows for modulation of its properties. This has resulted in ZnO being utilized for a number of applications such as gas sensing [15–18], photovoltaics [14, 19], UV photodetectors [20–22], non-volatile memories [23–25], and piezoelectric generators [18, 19, 26].

The interest in ZnO TFTs accelerated after the reports that the carrier mobility of ZnO TFTs outperform that of a-Si:H [27–29]. Initially, majority of ZnO TFTs were primarily fabricated using vacuum based deposition techniques such as ion beam sputtering [27], RF magnetron sputtering [28, 29], pulsed laser deposition [30] and atomic layer deposition [31]. However, more recently low cost solution based techniques such as spin coating [6, 32], spray coating [5, 33] and ink-jet printing [34, 35] have also been explored to yield performance level comparable with vacuum based devices. Solution processed thin films of ZnO have been achieved either by utilizing a suspension of ZnO nanoparticles or by decomposition of Zn precursors [36]. However, methods involving spin coating of nanoparticle suspension yielded poorer performance due to inter-particle voids which limits percolation [37]. Hence, precursor materials like zinc acetate [5, 6, 9, 12, 17] and zinc nitrate [9, 32, 34] have been widely utilized to obtain ZnO films by decomposing the precursors. In addition to this a number of novel processing chemistry based on combustion synthesis [13, 38], metal alkoxide precursor [10], single source tailored organo-complex precursors [39, 40] and photosensitive precursors [11, 12, 41, 42] have also been demonstrated to exhibit excellent performance in metal oxide devices. Towards this end, we explore the usability of non-aqueous precursor zinc neodecanoate, referred henceforth as Zn(NDN), as a novel precursor material for ZnO based electronics with further prospects of fabrication steps being compatible with nanoscale direct-writing through electron-beam exposure [43, 44].

In this work, due to the simplicity of fabrication as well as suitability to various optical and electrical characterizations, we investigate the development of thin films and TFTs, using relatively unexplored Zn(NDN) precursor. Zn(NDN) being a non-aqueous processable precursor, avoids formation of hydrolyzed intermediate species that could affect ZnO grain growth, unlike widely pursued aqueous precursors [43, 44]. Moreover, formation of hydrolyzed species at the semiconductor-dielectric interfaces leads to electron trapping that hinders n-type transport [45]. Previous reports of ZnO TFT devices prepared from Zn(NDN) have been limited to processes which involved multiple steps of spinning and decomposition in order to increase the ZnO film thickness and prepare a void-free thin film [43, 44]. However, multiple spin-decompose method is unsuitable for developing direct write techniques, where alignment accuracy in multiple patterning steps becomes challenging specially for scaling down the devices to 100 nm dimensions and below. Here we employ a single spin-decompose method, leading to thinner ZnO films and performed a detailed study of evolution of ZnO film properties and their correlation to the device physics of ZnO TFTs. We report the effect of process variation on structural and optical properties of ZnO thin films, using X-ray diffraction (XRD), UV–visible optical transmission spectroscopy and photoluminescence (PL) spectroscopy. Furthermore, performance of the TFTs at various processing parameters is considered in order to find optimal fabrication conditions. The transport mechanism is then explored to obtain phenomenological understanding of the factors limiting the charge transport in these class of devices.

2 Results and Discussion

2.1 Structural Characterization of ZnO Thin Films

We performed structural characterization of the ZnO thin films fabricated from Zn(NDN), (chemical structure shown in Fig. 1a), by subjecting them to different annealing temperatures (400–700 °C) to understand the evolution in crystalline quality of the ZnO films. Typical SEM image of a ZnO thin film prepared from 15 % Zn(NDN) solution is shown in Fig. 1b. X-ray diffraction measurements were performed on ZnO films prepared by drop casting Zn(NDN) solution and annealed under different processing condition. The XRD peaks (Fig. 1c) obtained from the measurements were

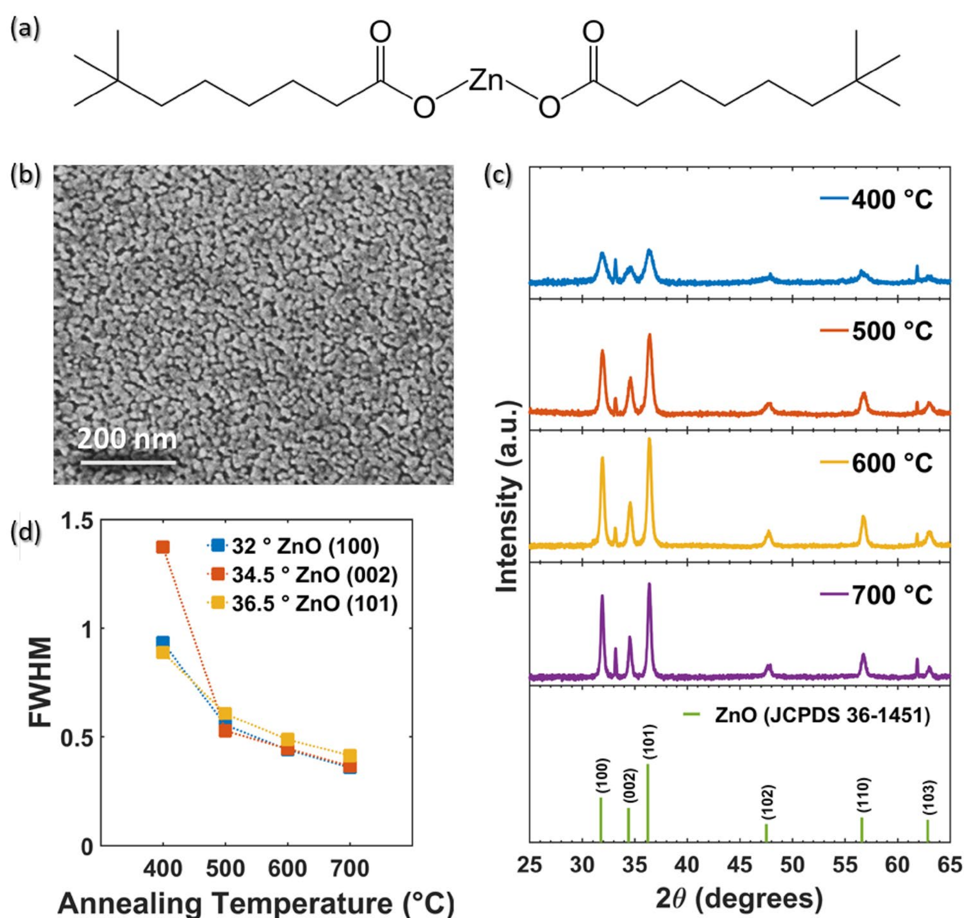

Fig. 1 **a** Chemical structure of Zn(NDN) Molecule **b** SEM image showing polycrystalline morphology in ZnO thin film prepared from 15 % Zn(NDN) annealed at 500 °C **c** X-ray diffraction measurements of ZnO films prepared by drop casting 15 % Zn(NDN) and annealed at different temperatures depicting polycrystalline nature of the films. The intensity of the corresponding XRD peaks can be seen to increase with annealing temperature. **d** Variation in the FWHM of the ZnO XRD peaks (100), (002) and (101) suggesting improvement in the crystalline quality with annealing temperature

indexed using polycrystalline wurtzite/zincite ZnO JCPDS card No. 36-1451 and the peaks at 2θ angles of 32°, 34.5° and 36.5° were assigned to (100), (002) and (101) orientation of ZnO, respectively [46, 47]. The peak at 33° may be attributed to contamination peak, similar to the case of zinc naphthenate [48]. From the XRD pattern shown in Fig. 1c, ZnO crystalline peaks are present over all the annealing temperatures clearly suggesting the formation of polycrystalline ZnO films from the decomposition of the precursor at all temperatures [43]. Furthermore, upon increasing the calcination temperature, a monotonous decrease in the FWHM (Fig. 1d) can be clearly seen for all three peaks, implicating increase in the average grain size of the ZnO films [5]. It should be noted that within our measurement range of 2θ angles (from 25° to 65°) the Si (100) peak (2θ ~ 70°) from the substrate is not seen.

2.2 Spectroscopic Characterization of ZnO Thin Films

As a next step, UV–visible spectroscopy was carried out on ZnO films fabricated from 15 % precursor concentration and annealed at different temperatures. Nearly 100 % transmittance across visible range signifies the presence of transparent ZnO phase (Fig. 2a). A prominent onset in the spectra can be seen between 350 nm and 400 nm. As the annealing temperature increases from 400 to 700 °C stronger absorption is observed below ~ 370 nm, which can be attributed to the improvement in the crystal quality of ZnO films and decrease in the impurity composition, consistent with the XRD measurements (Fig. 1c). Tauc plots were then utilized to estimate the bandgap of the ZnO films, using the expression $T = e^{-\alpha t}$ correlating the transmittance (T) to the optical absorption coefficient (α), where 't' is the thickness of the thin film. In a direct bandgap semiconductor the optical bandgap (E_g) of the thin film material can be related to α, using the expression $(\alpha h\nu)^2 = A\left(h\nu - E_g\right)$ where h is Planck's constant and ν is frequency of photons corresponding to incident light [49, 50]. Figure 2b shows the Tauc plots for ZnO films annealed at different temperature. The thicknesses of the ZnO films estimated using ellipsometry measurements are shown in Table S2. The bandgap of ZnO films estimated from the Tauc plots were in the range of 3.2–3.3 eV, with a higher bandgap obtained for films annealed at lower temperature. These bandgap values are in agreement with previous reports on solution processed ZnO thin films [5, 51, 52]. The observed variation in the bandgap with the processing temperature can be attributed to the

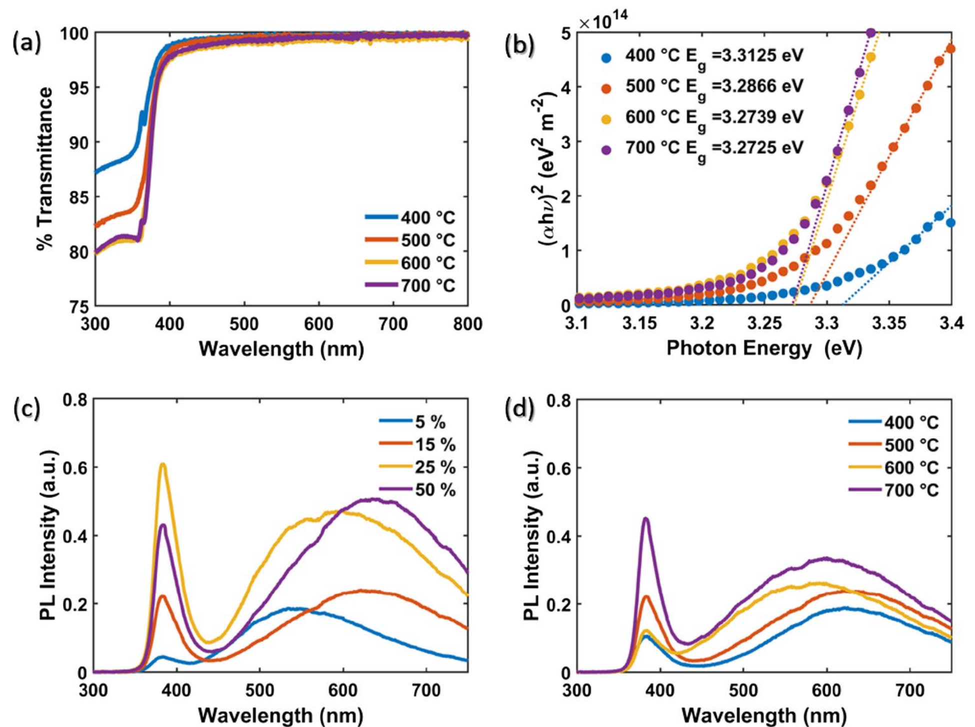

Fig. 2 Optical characterization of ZnO films prepared from Zn(NDN) **a** Transmission spectra of ZnO film prepared from 15 % Zn(NDN) and annealed at different temperatures **b** Tauc Plot extracted from transmission spectra with linear fits for the estimated bandgap Eg **c** PL spectra of ZnO films prepared from different concentrations of Zn(NDN) after annealing at 500 °C **d** PL spectra of ZnO films prepared from 15 % Zn(NDN) after annealing at different temperatures

quantum confinement effect of nano-crystalline ZnO phase embedded in an amorphous ZnO matrix [50]. Increasing the annealing temperature causes grains to grow larger leading to a decrease in the optical bandgap [50].

In order to further understand the degree of static disorder in the ZnO films, PL measurements were also performed by varying both the precursor concentration as well as the annealing temperature. In general, the PL spectra for a ZnO thin film constitutes of a peak at ~ 380 nm corresponding to the near band edge (NBE) emission, attributed to recombination of free-exciton [53, 54] and a deep-level (DL) emission arising from non-stoichiometric ZnO phase or oxygen vacancies [55, 56]. We observe that for ZnO films of thickness ~ 14.7 nm (Table S3) fabricated with 5% concentration, exhibit a weak NBE emission peak with respect to DL emission (Fig. 2c), indicating significant static disorder/vacancies. Upon increasing the concentration, from 5 to 25 % the intensity of the NBE emission increases. Correspondingly, FWHM of the NBE peak decreases from 38.8 nm for 5 % to 24.3 nm for 25 % concentration. Further increasing the precursor concentration to 50 %, results in a higher relative DL emission, possibly originating from inefficient packing due to large sized ZnO particles.

PL measurements were then performed on ZnO films fabricated from a solution of 15 % concentration and annealed at temperatures ranging from 400 to 700 °C (Fig. 2d). The higher DL to NBE emission ratio from films annealed at 400 °C could be attributed to the smaller sized ZnO particles and presence of grain boundary regions. Upon increasing the annealing temperature of the films, improvement in the crystallinity causes the relative emission at NBE to increase compared with the DL emission. Additionally, higher temperature assists with coalescence of smaller grains into the bigger ones, decreasing grain boundary regions as well as non-radiative defects [5, 57].

2.3 ZnO Thin Film Transistors

To obtain the optimal thickness for TFT performance, ZnO thin film devices were fabricated from different concentrations of precursors (5 % to 50 %) and annealed at 500 °C (details of the device fabrication is provided in the Experimental Section and Supplementary section S2). Variation in precursor concentration resulted in a thickness variation (as seen from Cross–section SEM images in Figure S1) from ~ 14.7 to ~ 38.5 nm as estimated by ellipsometry measurement (Table S3). TFTs fabricated from these ZnO thin films exhibit reasonable hysteresis free transfer characteristics indicating n-type transport (Fig. 3a) and near-ideal output characteristics with a distinct linear and saturation regime (Fig. 3b and Supplementary section S3a). The field effect mobility estimated from the saturation regime of transport (μ_{sat}) was obtained to be in the range of ~ 10^{-3}–10^{-2} cm^2 V^{-1} s^{-1}. The ON current increases by more than an order of magnitude when the precursor concentration is increased from 5 to 15 %. Correspondingly, the average μ_{sat} magnitude increased from 6.8×10^{-4} to 2.1×10^{-2} cm^2 V^{-1} s^{-1} (Fig. 3c). Note that for precursor

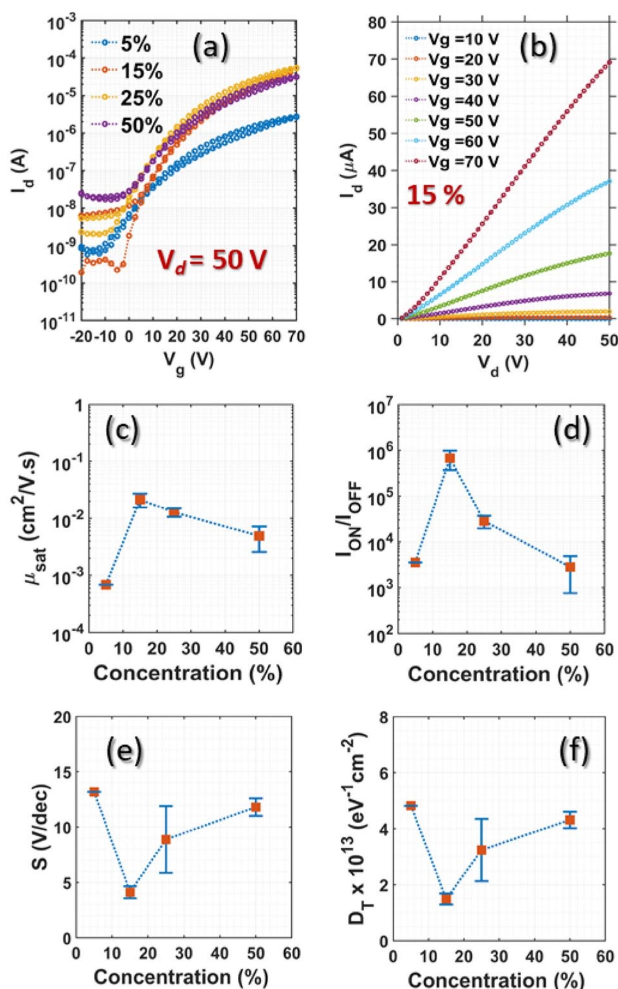

Fig. 3 **a** Transfer curves attained from ZnO TFTs prepared from different concentrations of Zn(NDN) **b** Output characteristics of ZnO TFT prepared from 15 % Zn(NDN). Variation in **c** saturation mobility **d** I_{ON}/I_{OFF} ratio **e** subthreshold swing **f** Interface trap density with Zn(NDN) concentration. Errors bars depict standard deviation over 5 devices

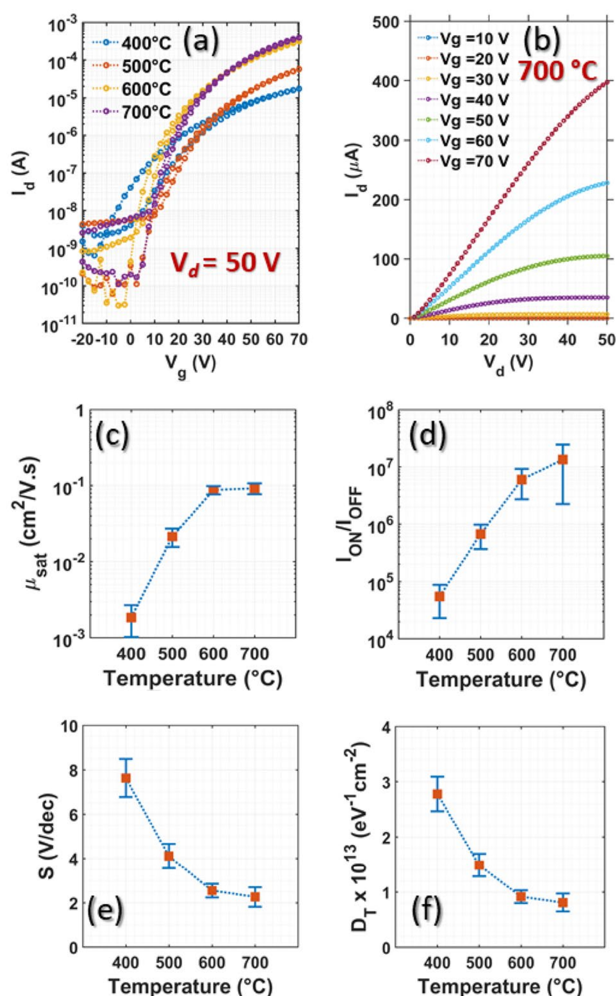

Fig. 4 **a** Transfer curves obtained from ZnO TFTs prepared from 15 % Zn(NDN) and annealed at different temperatures **b** Output characteristics of ZnO TFT annealed at 700 °C. Variation in **c** saturation mobility **d** I_{ON}/I_{OFF} ratio **e** subthreshold swing **f** Interface trap density with annealing temperature. Errors bars depict standard deviation over 5 devices

concentration above 15 % the magnitude of ON current remains fairly constant. Lower magnitude of ON current for the thin films prepared from 5 % precursor concentration can be attributed to smaller ZnO grain size (as obtained from AFM images shown in Figure S5) and insufficient percolation pathways for current flow. It should be noted that optimized TFT performance was obtained in the present case with ZnO film prepared from 15% precursor concentration with highest I_{ON}/I_{OFF} ratio (~ 10^5) as well as minimum values of subthreshold swing (4.1 V/decade) and trap concentration per unit energy (1.5×10^{13} eV^{-1} cm^{-2}). However, for ZnO films prepared from precursor concentration higher than 15 % the transport properties are observed to decrease (Fig. 3c–f) which can possibly be attributed to inefficient packing due to larger grains (Figure S5), consistent with the PL measurements shown in Fig. 2c.

As a next step we study the impact of precursor annealing temperature, on ZnO thin films prepared from 15 % precursor concentration and annealed at temperatures ranging from 400 to 700 °C for 1 h (details in the experimental section). Upon increasing the annealing temperature, following features are observed in the transistor characteristics: (a) the transfer characteristics exhibit an increase in the ON current and decrease in the hysteresis (Fig. 4a); (b) the output characteristics approach a clean saturation behavior (Fig. 4b and Supplementary section S3b); and (c) the μ_{sat} increases from 1.8×10^{-4} cm^2 V^{-1} s^{-1} for films fabricated at 400 °C to 0.1 cm^2 V^{-1} s^{-1} at 700 °C (Fig. 4c). This performance improvement can be attributed to the observed increase in

grain size of the ZnO films (Figure S6), thus reducing the grain boundary regions which act as scattering/trapping centers [33, 58, 59]. This is consistent with the increase in crystallinity of the ZnO films as observed from the XRD measurement (Fig. 1c–d) [59]. Consequentially, we also observe three orders of magnitude increment in I_{ON}/I_{OFF} (Fig. 4d), more than threefold decrease in the subthreshold swing from 7.6 V/decade at 400 °C to 2.3 V/decade at 700 °C (Fig. 4e) and a decrease in trap density (D_T) from 2.7×10^{13} eV^{-1} cm^{-2} at 400 °C to 8.1×10^{12} eV^{-1} cm^{-2} at 700 °C (Fig. 4f). Thus, the observed enhancement in the TFT characteristic can be attributed to the overall improvement in the dielectric-semiconductor interface due to the enhancement in the electronic quality of the ZnO thin films and the corresponding metal–semiconductor and semiconductor-dielectric interface. While some of the vacuum deposited ZnO thin film based transistor devices have shown subthreshold swing values down to 69 mV/dec [60–62], the best subthreshold swing values achieved in our work are comparable to the previous reports of oxide-transistors prepared from solution processing [59, 63–66].

To further understand the role of grain boundary on the TFT characteristics, TFTs were fabricated with varying channel length. We observe an increase in the TFT performance characterized by enhanced μ_{sat} (increase by a factor of ~ 3), decrease in D_T and SS upon decreasing the channel length from 50 to 5 μm (Fig. 5a and Figure S7). This trend can be attributed to the fact that the charge carriers in large channel devices encounter higher number of grain boundaries, resulting in higher degree of trapping/scattering. The channel length dependent mobility measurement brings out the limiting factor of charge transport in polycrystalline ZnO films to be grain boundary scattering rather than external factors originating from contact resistance in these devices.

Temperature dependent mobility measurements were then performed on TFTs fabricated with ZnO films obtained from annealing at 400 °C and 700 °C. Transfer curves were measured over a temperature range of 300–420 K and the mobility is fitted with an Arrhenius trend,

$$\mu = \mu_0 \exp\left(\frac{-E_a}{k_b T}\right)$$

where μ_0 is the mobility at 0 K and E_a is the activation energy as shown in Fig. 5b. Low temperature measurements were not possible with these devices because of the loss

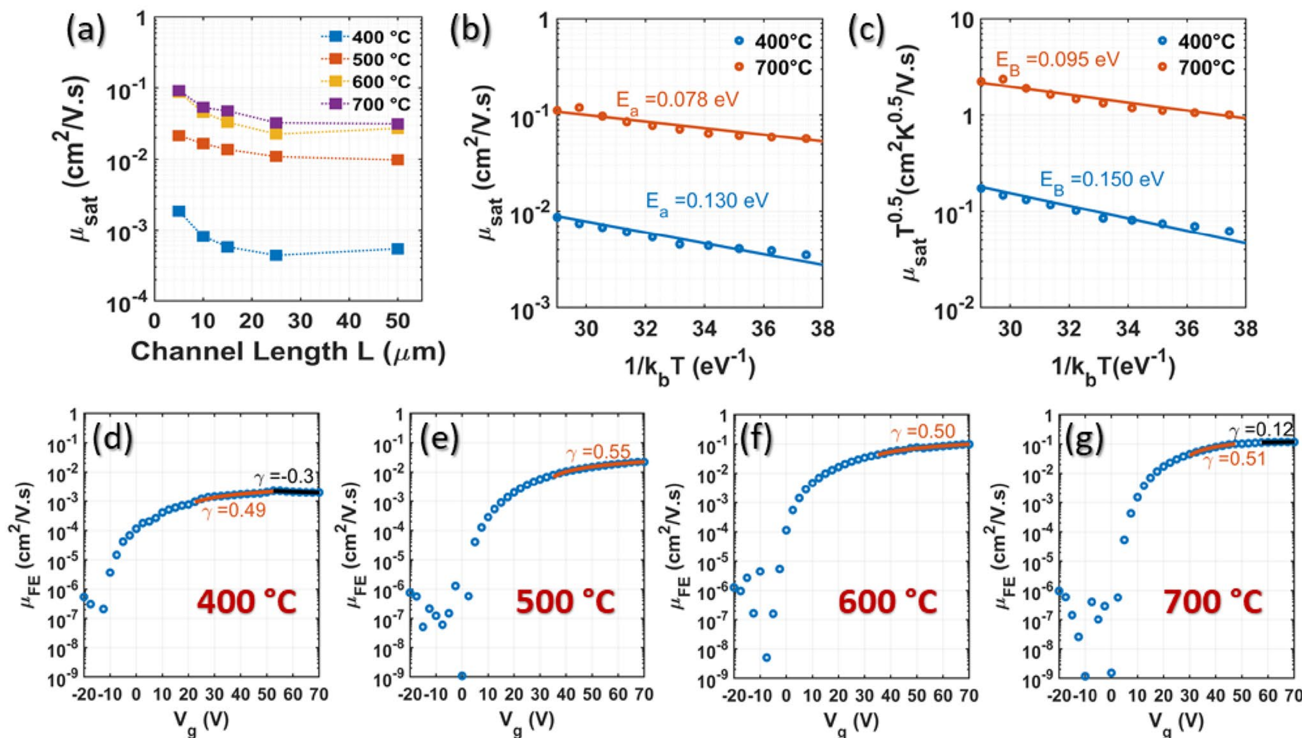

Fig. 5 **a** Evolution of transistor saturation mobility with channel length **b** Arrhenius plots of saturation mobilities extracted from ZnO thin film transistors with films annealed at 400 °C and 700 °C **c** Linear correlation plot of ln($\mu_{sat}T^{0.5}$) vs $1/_{k_bT}$ signifying grain boundary thermionic emissions limited transport **d**–**g** Mobility vs gate voltage plots of TFTs fabricated from ZnO films annealed at different temperatures. The change in γ value from 0.51 to 0.12 at 700 °C suggests deviation from trap limited transport, dominant at lower annealing temperatures

of gate modulation under vacuum, possibly due to formation of oxygen vacancies or oxygen desorption. Nevertheless, in the range of temperature measured we observe that the activation energy E_a decreases from 0.13 to 0.078 eV upon increasing the annealing temperature of the ZnO films, which is consistent with the decrease in grain boundary induced trapping/scattering mechanism. Interestingly, the value of activation energy, for the device fabricated from films annealed at 400 °C, is close to the energetic levels of zinc interstitials which was suggested by Cordaro et al. to be around 0.17 eV [67]. Removal of these deep traps as a consequence of higher annealing temperature may explain the improved performance of the devices.

The μ_{sat} versus temperature trend can be modelled as a consequence of thermionic emission across grain boundary potential barrier of polycrystalline semiconductor, using the expression,

$$\mu_{sat} = \frac{B}{T^{0.5}} e^{-\frac{E_B}{k_b T}}$$

where B represents exponential pre-factor while E_B corresponds to grain boundary potential barrier [20, 68]. As shown in Fig. 5c, a linear correlation exists between $\ln(\mu_{sat} T^{0.5})$ and $^1/_{k_b T}$ for devices fabricated at both the annealing temperatures (400 °C and 700 °C). The grain boundary potential barrier is estimated to be 0.15 eV for ZnO films annealed at 400 °C as compared to 0.095 eV in the case of 700 °C.

To further analyze the transport mechanism, we evaluated the V_g dependence of the mobility for the TFT devices fabricated with ZnO films annealed at different temperatures. The field effect mobility can be expressed as a power law behavior given by, $\mu_{FET} = K\left(V_g - V_{th}\right)^{\gamma}$; where K and γ are chosen appropriately to fit the data. The value of fitting exponent γ elucidates the type of transport mechanism assumed [69]. When γ is closer to 0.7 the transport mechanism is expected to be trap limited charge (TLC) transport and as the value approaches 0.1, effect of trapping mechanism decreases and other mechanisms of transport such as percolation dominated conduction (PC) are exhibited [66, 69]. Figure 5d–g depicts the representative plots of μ_{FET} versus V_g for TFT devices fabricated under different annealing condition along with the respective power law fits. For TFT devices fabricated with ZnO films annealed at temperatures from 400 to 600 °C the exponent γ attains values closer to 0.7, suggesting TLC dominated transport mechanism. However, two transport regimes can be identified for the devices where the films were annealed at 700 °C (Fig. 5g). At $V_{g,}$ just higher than threshold voltage, γ has value of 0.51, pointing to the transport still dominated by TLC; whereas at higher V_g regime the exponent γ drops to 0.12. This, in turn, implies that in high V_g regime, most of the traps are filled up and hence all the charges accumulated by the gate voltage thereafter can go directly to the conduction band and can add to the current flow. Nevertheless, from the analysis based on different transport models it can be proposed that grain boundary depletion region could be the major source of deep level traps in these ZnO thin films.

3 Conclusion

In conclusion, application of Zn(NDN) functional precursor was explored for fabricating ZnO TFTs. Based on detailed optical, structural, and electrical characterization it was found that films prepared with 15 % concentration of Zn(NDN) in toluene exhibit the best TFT device performance with near unity transmission suitable for transparent electronics. It was possible to observe μ_{sat} reaching up to 0.1 $cm^2 V^{-1} s^{-1}$, current modulation of ~ 10^7 and subthreshold swing as low as 2.3 V/decade when the devices are fabricated with an annealing temperature of 700 °C. Finally, the transport mechanism in the ZnO films prepared from Zn(NDN) was also investigated using different transistor mobility models. We observe a decrease in static disorder signified by lower activation energy and decrease in the depletion barrier for grain boundary thermionic emission upon increasing the annealing temperature of precursor to 700 °C. This was consistent with the deviation from trap limited behavior in the transfer characteristics for devices obtained at higher temperatures. Our study thus provides a general guideline for developing non-aqueous precursors towards oxide-based high performance transparent electronic applications.

4 Experimental Section

Precursor preparation- Zinc neodecanoate (molecular weight 407.9 g/mol; structure shown in Fig. 1a) was procured from Alfa Aesar and diluted from the commercial density 1.1 g/cc to the required concentration (v/v) using toluene as a solvent (details in Table S1). The precursor solution was subjected to ultrasonic agitation at 80 °C for 3 h to obtain a thoroughly dissolved solution. The vial was then allowed to cool down naturally. Once dissolved, the solution is stable for months.

Substrate preparation- Prime grade boron doped p^{++} Si (100) wafers with 100 nm thermally grown SiO_2 were used as substrate for the fabrication of ZnO TFTs. The 4″ wafers were diced into 12 mm x 12 mm sized substrates, cleaned by 10 min ultrasonic agitation in acetone and isopropyl alcohol and dried using compressed nitrogen flow. The samples were then placed in a freshly prepared piranha solution (1:3

volume mixture of hydrogen peroxide and sulphuric acid) for 15 min and thoroughly rinsed in HPLC grade deionized water. After blow drying with compressed nitrogen, samples were treated with oxygen plasma for 10 min and then baked on a 200 °C hotplate.

ZnO thin film synthesis- The precursor solution, filtered through 0.2 µm PTFE syringe filter, was spin coated on the precleaned Si or quartz substrates at 2000 rpm for 60 s with ramp rate of 2000 rpm/sec for device and spectroscopic studies respectively. The samples were then baked at 115 °C for 1 min to dry off the residual solvent. This was followed by loading the samples into a Carbolite tube furnace which was ramped up at 10 °C/min to obtain the final annealing temperature which in the present study ranges from 400 to 700 °C. The samples were maintained at the final annealing temperature for 1 h followed by slow cooling down back to room temperature. During the annealing step one end of the tube was connected to the exhaust line to maintain a small air flow.

XRD Measurements- For the XRD measurements ZnO thin films were synthesized from a 15% Zn(NDN) solution drop casted on a cleaned Si-SiO_2 substrates and left overnight to remove the solvent. This was followed by annealing the substrates at specific annealing temperature ranging from 400 to 700 °C for 1 h.

Optical Characterization- Transmission (300 nm to 700 nm) measurements were obtained on ZnO thin films synthesized from a 15% concentration of Zn(NDN) spin-coated on pre-cleaned quartz substrates and annealed at various temperatures ranging from 400 to 700 °C. Photoluminescence (PL) measurements were conducted on ZnO films synthesized over Si substrates, using a 266 nm Laser with an incident power of 2.2 mW power.

Transistor fabrication and characterization- The thin film transistors fabricated in this study are Bottom Gate-Top Contact devices. Once the ZnO thin films were prepared on the Si-SiO_2 substrates, the source and drain contacts were obtained using standard photo–lithography and lift–off process to obtain devices with 500 µm channel width and channel lengths varying from 5 to 50 µm. Unless otherwise stated, the transistor devices discussed here have the channel length of 5 µm. The complete processing flow is shown in Figure S2 and details of the lithography patterning is provided in the supplementary section S2. All the devices, unless stated otherwise, were characterized using SUSS-Microtec Probe station and Keithley 4200 SCS under ambient air conditions at room temperature in dark. For the transconductance measurements, $V_{ds} = 50$ V was applied, and V_g was swept from -20 V to 70 V with a step size of 2.5 V for both forward and reversed direction. During the I_d-V_d output measurements a constant V_g was applied, and V_{ds} was swept from 0 to 50 V with a 1 V step. This way, V_g was varied from 10 to 70 V with 10 V step. The mobility in the saturation regime of a transistor channel was estimated using the following expression: $\mu_{sat} = \frac{2L}{WC_o}\left(\frac{\partial\sqrt{I_d}}{\partial V_g}\right)^2$ where L and W are channel length and width respectively, C_o oxide capacitance per unit area. Oxide capacitance was estimated to be 3.5×10^{-8} F cm^{-2} based on the specifications of the oxide layer (100 nm thick SiO_2 gate oxide and relative dielectric constant (ε_r) of 3.9). Subthreshold swing was calculated using the expression: $= \frac{\partial V_g}{\partial \log I_d}$. The trap concentration per unit energy (D_T) was also calculated using the following expressions: $D_T = \frac{C_o}{e^2}\left(\frac{eS}{k_b T \ln 10} - 1\right)$ [70, 71].

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