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# Design of a Hardware/Software FPGA-Based Driver System for a Large Area High Resolution CCD Image Sensor

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**Abstract:** A hardware/software field programmable gate array (FPGA)-based driver system was proposed and demonstrated for the KAF-39000 large area high resolution charge coupled device (CCD). The requirements of the KAF-39000 driver system were analyzed. The structure of "microprocessor with application specific integrated circuit (ASIC) chips" was implemented to design the driver system. The system test results showed that dual channels of imaging analog data were obtained with a frame rate of 0.87 frame/s. The frequencies of horizontal timing and vertical timing were 22.9 MHz and 28.7 kHz, respectively, which almost reached the theoretical value of 24 MHz and 30 kHz, respectively.

**Keywords:** CCD imaging sensor, driver system, FPGA, state machine

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## 1. Introduction

The area array charge coupled device (CCD) image sensor is widely used in so many aspects such as optical real-time test, digital still-imaging, industrial measurement, and aerial photography [1, 2]. With the development of the metal-oxide-semiconductor field effect transistor (MOS-FET) array manufacture technology, CCD sensors with the larger area, more pixels, and higher resolution have gained more and more applications in the fields of the high precision remote sensing, unmanned aerial platform, and earth observation system [3, 4] and so on. Despite of advantages such as the high resolution, high sensitivity, and wide coverage, the driver system design of a lager area high resolution CCD is difficult to implement for its huge amount of imaging data and complex timing arrangement [5].

In this paper, a hardware/software field programmable gate array (FPGA)-based driver system is proposed for the KAF-39000 large area high resolution CCD. The hardware circuits were designed to supply power to the KAF 39000 circuits, while the FPGA-based hardware/software system was used to control the timing signals and imaging data streams of KAF39000. The test results showed that dual channels of imaging analog data were obtained with a frame rate of 0.87 frame/s. The frequencies of horizontal timing and vertical timing were 22.9 MHz and 28.7 kHz, respectively, which

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almost reached the theoretical value of 24 MHz and 30 kHz, respectively.

## 2. Requirements of the KAF-39000 driver system

The KAF-39000 is a dual output, high performance CCD image sensor with 7216 (horizontal)×5412 (vertical) photoactive pixels designed for a wide range of the color and monochrome imaging sensing application. In order to driver the KAF-39000 well, the requirements of the timing are first analyzed.

There are three kind of timing for KAF-39000, frame timing, line timing, and pixel timing which are shown in Figs. 1, 2, and 3, respectively. The frame timing is used to control a frame of the image outputted from the CCD sensor. The line timing controls a vertical line of pixels transferred from the imaging area to the horizontal output register under the drive of vertical clocks. The pixel timing is applied for transferring the pixels in the horizontal output register to the output amplifier under the drive of horizontal clocks. It can be seen that the generation of vertical clock signals (V1, V2), horizontal ones (H1, H2), and three timing signals are the basic requirements for driving KAF-39000. In addition, the correct power supplies are vital as well for KAF-39000, which is the basis of the whole system. Table 1 shows the requirements of bias voltages of KAF-39000.

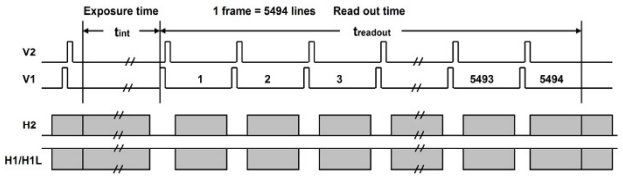


Fig. 1 Diagram of frame timing of KAF-39000.

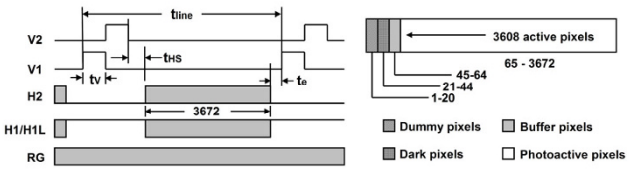


Fig. 2 Diagram of line timing of KAF-39000.

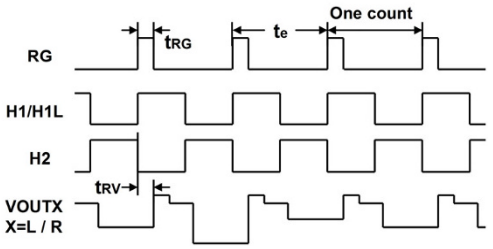


Fig. 3 Diagram of pixel timing of KAF-39000.

Table 1 Refractive index versus temperature.

| Bias voltage | Maximum (V) | Minimum (V) | Typical value |
|---|---|---|---|
| $V_{LOD}$ | 10.2 | 9.8 | 10.0 |
| $V_{DD}$ | 15.5 | 14.5 | 15.0 |
| $V_{SS}$ | 1.0 | 0.5 | 0.7 |
| $V_{RD}$ | 11.7 | 11.3 | 11.5 |
| $V_{SUB}$ | 0 | 0 | 0 |
| $V_{OG}$ | –2.8 | –3.2 | –3.0 |

## 3. Design of the KAF-39000 driver system

According to the requirements analyzed above, two sorts of driver signals, timing and power supply signals, are essential ones for the regular work of KAF-39000. Besides, after the exposure of KAF-39000, the output analog imaging signals are weak and accompanied with plenty of noises [6]. By noise filtering, voltage clamping, signal amplification, and analog-to-digital conversion, the real analog imaging signals are extracted from the noises and converted to digital ones for computational processing [7]. So two main functions are needed for the KAF-39000 driver system. The first part, which is called the basic system, is to generate two kinds of driver signals. The second one, which is called the imaging signal processing system, is used to process the output analog imaging signals of KAF-39000.

In this paper, the structure of "microprocessor + ASIC chips" is implemented for system integration and simplification. The overall system design is shown in Fig. 4. The FPGA of EPF10K30ATC144 manufactured by ALTERA Inc. was used as a microprocessor for the whole driver system. In the basic system, the chip of KSC-1000TG produced by Kodak Inc. was applied to generate the clock and timing signals. In the imaging signal processing

system, as dual output analog imaging signals, two chips of AD9845 produced by Analog Device Inc. were used to process them. The control bits were distributed to the register of selected chips (KSC-1000TG or AD9845) to control the work status of them by FPGA. The operational amplifier circuits precisely generate the bias voltages for KAF-39000 and the chips needed on board.

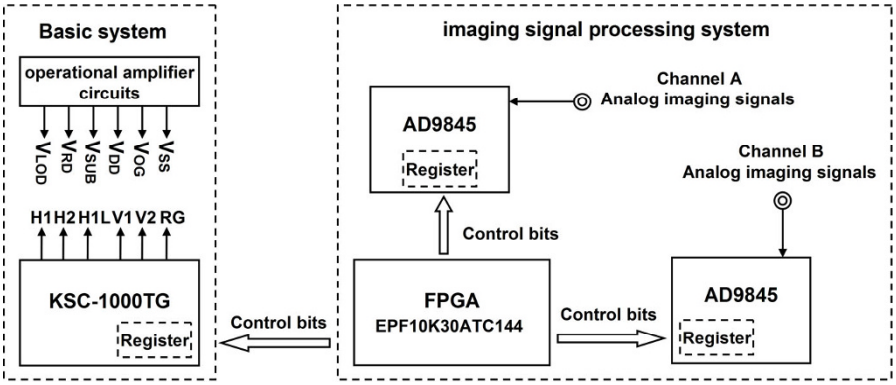


Fig. 4 Overall driver system design for KAF-39000.

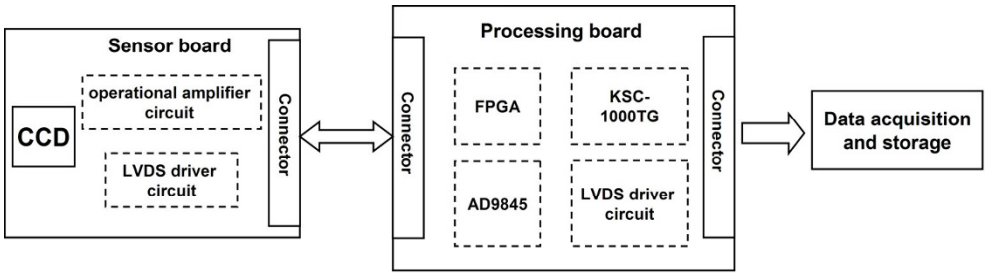


Fig. 5 Diagram of sensor board and processing board design.

In practice, in order to integrate the system, two printed circuit board (PCB) circuit boards named the sensor board and processing board were designed to realize the function described above, as shown in Fig. 5. The CCD sensor is placed on the sensor board, and the operational amplifier circuits supply the power for the sensor and ASIC chips. On the processing board, the FPGA, KSC-1000TG, and two AD9845 chips are integrated together. Two boards are connected by the low voltage differential signaling (LVDS) connectors. The power supply signals are transferred from the sensor board to the processing board, driving all chips working normally. The timing signals generated by KSC-1000TG are transferred to the CCD sensor in the contrary direction. After the exposure of the CCD sensor, two channel analog imaging signals are transferred to AD9845s for processing. Especially, LVDS connecter driver circuits are necessary to convert the transistor-transistor logic (TTL) voltages to the LVDS format.

### 3.1 Design of the sensor board

The schematic diagram of the sensor board is exhibited in Fig. 6. The external power supply ±20 V and ±5 V as the origin of the whole system. Operational amplifier circuits which consist of the inverting and non-inverting amplifiers employing OP213FSs are used to divide the external voltage to the value needed. The LVDS acceptor converts the input LVDS signals to the TTL format, and then the vertical clock driver and horizontal clock driver extract the vertical and horizontal clock signals, respectively. When exposure is triggered, the clock signals would drive the dual analog imaging signals (Vout_left and Vout_right) exported from the CCD frame by the frame. After the transportation through the protection circuit, the dual analog imaging signals are transferred to the next processing board from the connector.

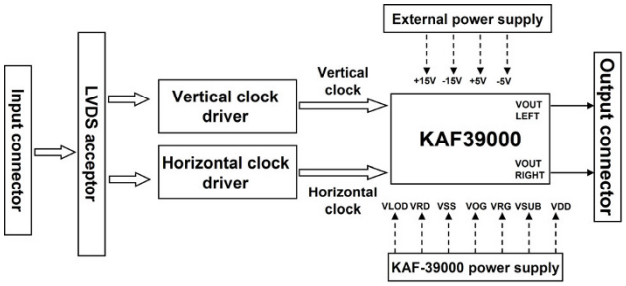


Fig. 6 Schematic diagram of the sensor board.

### 3.2 Design of the processing board

The schematic diagram of the processing board is presented in Fig. 7. The core of the processing board is the FPGA microprocessor. A hardware description language is downloaded through the JTAG downloader and decoded in the FPGA, controlling three ASIC chips by three serial control bits (SDATA, SLOAD, and SCLK). SLOAD is the enable signal; the chip is ready to work when SLOAD is on. SDATA is serial data bit stream which is inserted into the registers in three ASCI chips. SCLK is the clock signal to write the SDATA serial bit which is different for KSC-1000TG and AD9845. The vertical and horizontal timing signals generated by KSC-1000TG are decoded by the LVDS driver circuits and transferred to the sensor board. Analog imaging signals received from the sensor board are processed and converted to digital ones in two chips of AD9845. The digital imaging signals are used for the acquisition and storage for the next stage. It should be noted that a systematic crystal oscillator is provided to give the original clock signal for FPGA.

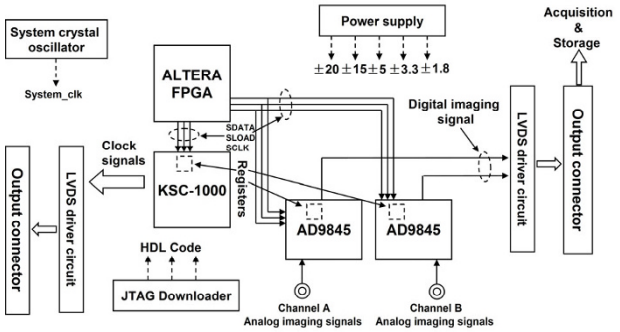


Fig. 7 Schematic diagram of the processing board.

## 4. FPGA software design

The FPGA is the key on the processing board. The function is to write "control bits" to the ASIC chips' registers to determine how the enabled chip works. The Altera hardware description language (AHDL) is used in this paper to code. Figure 8 shows the AHDL code structure which is composed of the definition section and main section. Five categories are defined in the definition section: input and output ports, register configuration constants, state machines, global variables, and local variables. The main section includes six modules analyzed as follows.

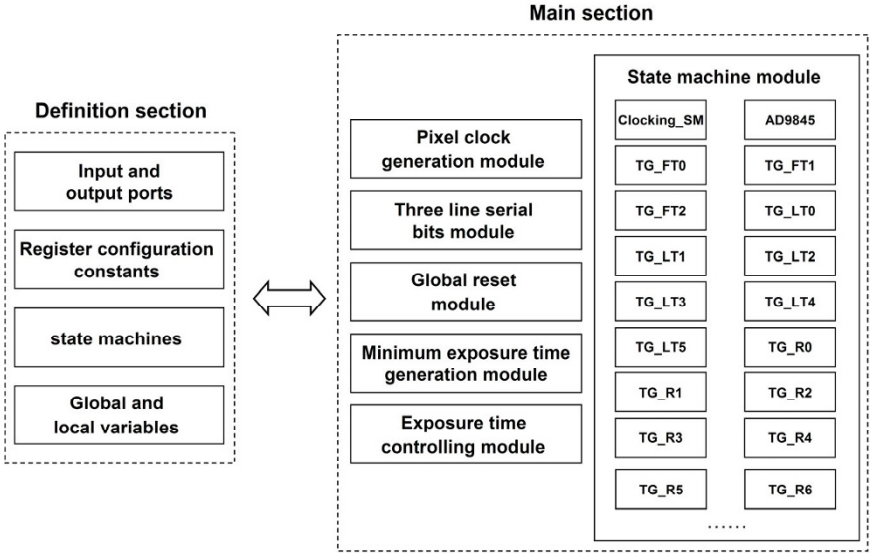


Fig. 8 AHDL code structure.

### 4.1 Pixel clock generation module

The main function of this module is to generate an internal-based fiducial pixel shifting clock and to synchronize the vertical and horizontal pixel shifting clocks. It can be achieved by frequency dividing of the system clock which is provided by the external crystal oscillator.

### 4.2 Three line serial bits module

Firstly, the input three line serial bits are decoded in the module to determine which chip is enabled. Then, three line serial bits (SLOAD, SDATA, and SCLOCK) are interpreted and inserted into the selected chip. The module working flow is shown in Fig. 9.

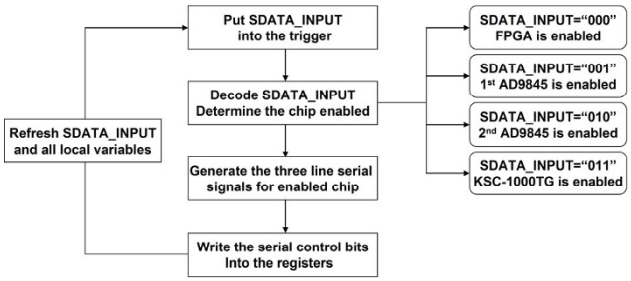


Fig. 9 Work flow of three line serial bits module.

### 4.3 Global reset module

A global reset signal is generated in this module. When it works, all of registers and flip-flops in the FPGA are shut down to the initial status. The aim is to provide a back-up reset function for the system in case of an unpredictable system crash.

### 4.4 Minimum exposure time generation module

The minimum exposure time is 1 ms in this paper, and the exposure time of the CCD sensor is a multiple of 1 ms. The minimum exposure time generation is favorable of controlling and changing the exposure time more precisely. The minimum clock is obtained by counting the pix clock.

### 4.5 Exposure time controlling module

There are two ways to control the exposure time. External input signals D[0:13] are applied to control which is not used normally. The primary method is to define a multiple of minimum exposure time and determine the exposure trigger moment. So it is easy to control the exposure time at user's will.

### 4.6 State machine module

The state machine module is vital which determines how the ASIC chips work. The function of the module is to write the "control bits" to the registers in ASIC chips by switching between state machines. There are two sorts of state machines, one is called the register state machine, and the other is named "Clocking_SM". The register state machines contain all registers in KSC-1000TG and AD9845. The register configuration constant is assigned to the global variable by the state machine switching. At last, the value of the global variable is inserted into the corresponding chip. Figure 10 displays the state machine switching procedure in AD9845.

The other Clocking_SM state machine is composed of all six states of the CCD sensor, such as clear_all, setup, trig_hold, integration, flush, and frame_transfer. The combination and switching of six states correspond to different statuses of the CCD sensor. So it is easy to control the CCD sensor by changing the state machine configuration.

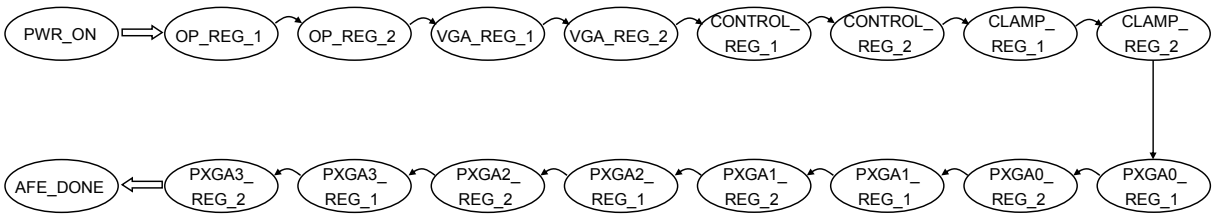


Fig. 10 State machine switching procedure in AD9845.

## 5. Experiment and test results

Based on the design of hardware and software, the sensor and processing PCB boards were drawn, printed, and tested. The test environment is shown in Fig. 11. The digital multimeter (HAITI DT9205A+), the DC stabilized power supply (LONGWEI TPR3003-2D), the digital oscilloscope (JINGCE JC1102TA), and analog oscilloscope (ATANA DK020) were used in the test. The test results are presented in Figs. 12 and 13. In Fig. 12(a), horizontal clock signals are generated at the frequency of 22.9 MHz, while the vertical clock signals exhibited in Fig. 12(b) are at the frequency of 28.7 kHz, respectively, which are almost reach the theoretical values of 24 MHz and 30 kHz, respectively. The dual analog imaging signal outputs are shown in Fig. 13, making a frame rate of 0.87 frame/s which is close to the maximum value of 0.9 frame/s.

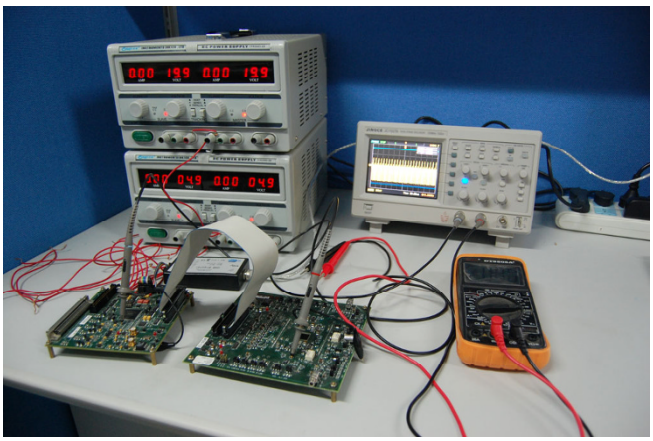

Fig. 11 Test environment for the driver system of KAF-39000.

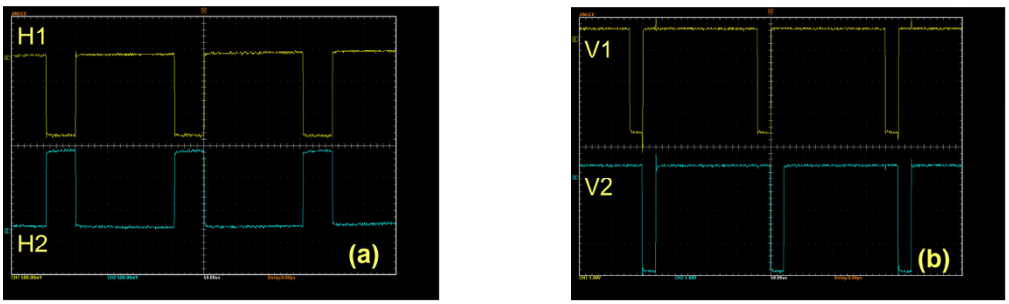


Fig. 12 Generated timing signals: (a) horizontal clock signals and (b) vertical clock signals.

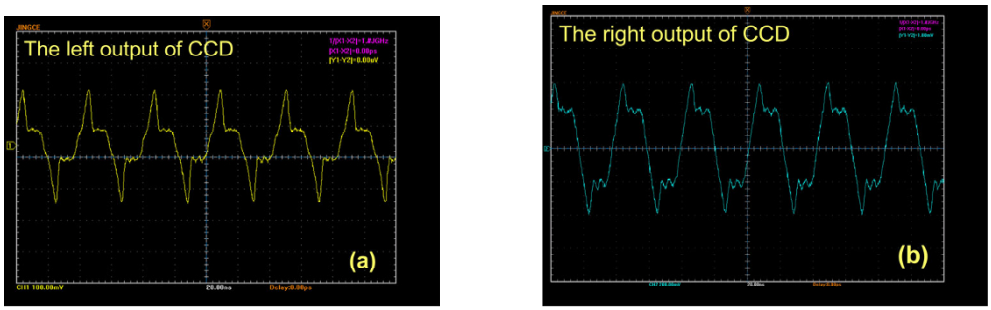


Fig. 13 Output analog imaging signals: (a) left channel and (b) right channel.

## 6. Conclusions

In summary, a hardware/software FPGA-based driver system was proposed for KAF-39000 large area high resolution CCD. The requirement of the timing and power supply for KAF-39000 was analyzed. The structure of "microprocessor + ASIC chips" was implemented for the system design. Then, the sensor and processing board were designed and manufactured subsequently. Especially as the controller of the system, the FPGA software design was described in detail. At last, the experiment and test were carried out. The results showed that dual channels of imaging analog data were obtained with a frame rate of 0.87 frame/s. The frequencies of horizontal timing and vertical timing were 22.9 MHz and 28.7 kHz, respectively, which almost reached the theoretical values of 24 MHz and 30 kHz, respectively. It could be concluded that the demands were met by the FPGA-based driver system.

## Acknowledgment

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