Silicon
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CORRECTION

Correction to: Quantization Effect in N-Channel Inversion Mode Si, In0.53Ga0.47As and Ge Based Double Gate MOSFET Using Quasi-Static Capacitance–Voltage Characteristics for Upcoming Sub 10 nm Technology Node

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Correction to: Silicon
https://doi.org/10.1007/s12633-024-02919-8

The original version of the article unfortunately contained an error.

Figure 8(a) is missing. The correct figure image is shown in the next page.

The original article can be found online at https://doi.org/10.1007/s12633-024-02919-8.

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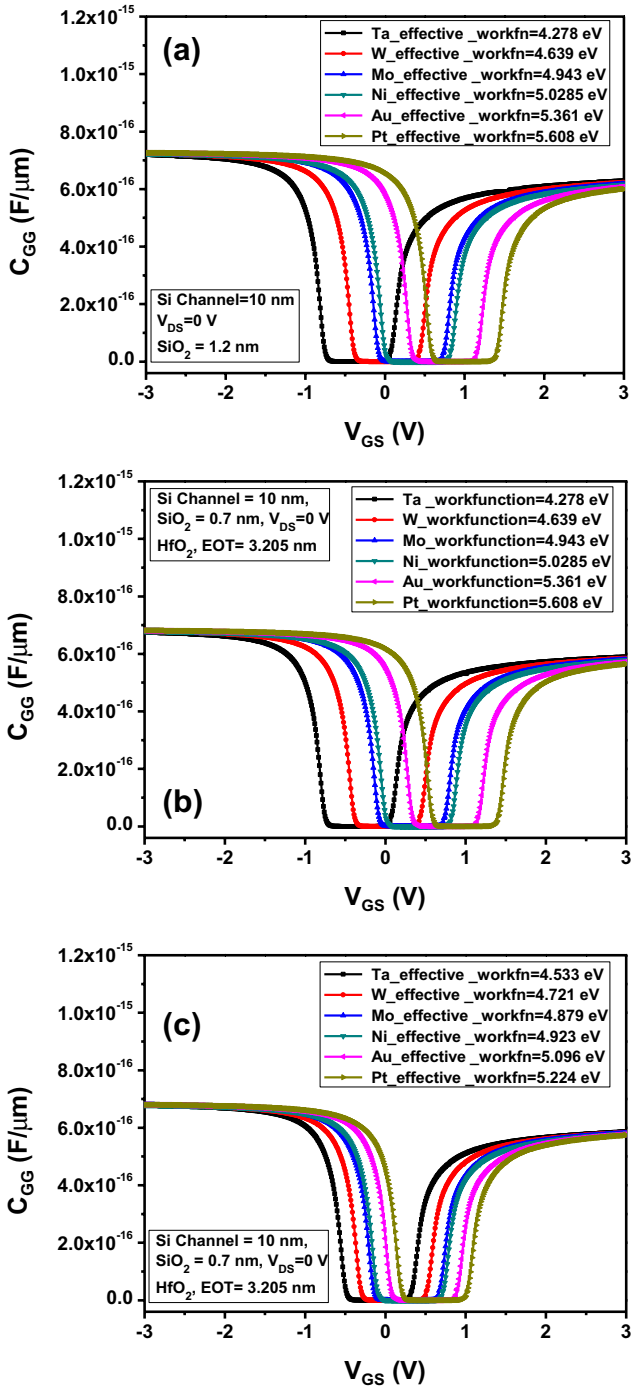

Figure 8. C_{GG} *vs* V_{GS} curves for nMOSFET with Si channel of thickness 10 nm and with different metal gates at $V_{DS} = 0V$ for (**a**) $SiO_2 = 1.2nm$ (**b**) $SiO_2 = 0.7nm, HfO2 = 3.205nm$ (**c**) $SiO_2 = 0.7nm, HfO2 = 3.205nm$

The original article has been corrected.