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ORIGINAL PAPER

# Analog/RF Performance Analysis of a-ITZO Thin Film Transistor

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**Abstract**

This work reports RF and analog performance analysis of an amorphous Indium Tin Zinc Oxide thin film transistor. The various parameters affecting the performance of a-ITZO TFT like drain current, drain conductance, output resistance, transconductance, transconductance generation factor, early voltage, intrinsic gain, capacitances, cut off frequency, maximum frequency of oscillation, transconductance frequency product, gain frequency product, gain bandwidth product and gain transconductance frequency product have been closely examined. The device is further analyzed to investigate the impact of variation in physical parameters viz. dielectric material, dielectric thickness (*Dt*) and temperature (T) on the RF/Analog performance. Use of high-*k* dielectric material in the simulated structure has resulted in low subthreshold slope (SS) of 0.62 V/decade, On voltage (*Von*) of - 0.29 V, $Ion/Ioff$ ratio of ~ $10^9$, intrinsic gain ($A_v$) of 104.5 dB and gain frequency product (GFP) of 1.86 GHz. The best results for dielectric thickness variation are obtained for $D_t$ of 150 nm with SS of 0.22 V/decade, *Von* of -0.26 V, $Ion/Ioff$ of ~ $10^{10}$, $A_v$ of 175.69 dB and GFP of 2.39 GHz. In order to investigate device thermal reliability and stability, temperature analysis has also been done. To demonstrate the circuit level implementation of the simulated structure, a resistive load inverter circuit is simulated and analyzed for different variations (high-*k*, *Dt* and T). It has also been concluded that TFT with high-*k* material or thinner dielectric at T=300 K provides best performance. This analysis confirms the potential of a-ITZO TFTs to realize high performance analog/RF circuits.

**Keywords** Analog/RF performance · a-ITZO TFTs · Dielectric material · Dielectric thickness · TCAD

## 1 Introduction

In recent years, thin film transistors have drawn a significant attention of researchers as it has become the backbone of thin film electronics industry. A CAGR of 17.34% is expected to register for TFT market during 2021-2026 [1]. TFT is used as a pixel switching element in LED or flat panel displays [2–4]. The major outlook of display industry is to produce large area and high-resolution displays. Therefore, there is an immediate need to improve the performance of TFTs. TFT is a special type of transistor which has a supporting substrate over which a layer of dielectric, semiconductor and contacts are deposited [5]. The material used as channel layer are A-Si, Poly Si, Semiconducting Metal Oxides (SMO's) etc. Use of A-Si and Poly-Si for large and high-resolution display is now becoming unacceptable because of its low mobility, high processing temperature and inferior electrical properties [6]. Considering these limitations, semiconductor oxide materials like ZnO [7], $SnO_2$ [8], GaZnO [9], IGZO [10] etc. are seen as a replacement to A-Si and Poly-Si. Among all semiconductor oxide materials, ZnO has drawn a significant attention of researchers because of its large band gap, low cost, good transparency, appreciable mobility, abundance in nature and high excitation energy [11]. However, Chung et al. [12] reported that ZnO has many grain boundaries which limit its use in large and high-resolution displays. This obstacle was resolved by doping ZnO with metals like In [13], Al [14], Tin [15], Mg [16] etc. to make amorphous oxide semiconductors (AOS) with no grain boundaries. As

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reported by Lee et al. [17], IGZO as AOS in channel layer of TFT provides high electric mobility as well as high optical transmittance. Nomura et al. [18] reported first IGZO TFT at room temperature and suggested that IGZO can be used as a potential material for future electronic devices. Yabuta et al. [19] grown IGZO as channel material for TFT with mobility ($\mu_{fe}$) of the order of ~ 10 and $I_{on}/I_{off}$ ratio of the order of ~ $10^8$. However, this high mobility and stability is still not sufficient for next generation displays which require $\mu_{fe}$ of the order of ~ 20. Wang et al. [20] proposed a-ITZO as an alternative of IGZO with high $\mu_{fe}$ (~44) and good stability. Zhong et al. [21] reported that ITZO is a potential TFT channel material as it offers high mobility of ~19 $cm^2$ $V^{-1}$ $s^{-1}$, and subthreshold swing of ~0.6 V. Based upon the past literature, it can be concluded that a-ITZO has all potential properties that makes it a potential material for TFTs.

To investigate the applicability of a-ITZO as channel layer in TFTs, a simulation study using ATLAS tool [22] from Silvaco TCAD have been reported in this work. To demonstrate the use of a-ITZO TFT in Analog/RF application, different RF/Analog parameters have been studied. To the best of our knowledge, this kind of investigations have not been reported in literature for TFTs. Furthermore, it has also been seen that high density analog and RF application are facing challenges in the attainment of higher device performance like low power and high frequency of operation. Different methods like scaling the geometric dimensions, material changes and temperature variability [23–27] can effectively make the TFTs to work at low voltages with decreased subthreshold swing. To achieve current device requirements, scaling the dimension of TFT is seen as a potential method by many researchers. Scaling also scales the dielectric thickness. Kumar et al. [28] reported that downscaling has improved electrical parameters like $I_{on}/I_{off}$, $\mu_{fe}$, SS but at the cost of increasing tunneling gate leakage current. To cop up with this, Vyas et al. [29] suggested that high-*k* dielectric material like $Al_2O_3$, $HfO_2$ etc. can improve the electrical performance of TFTs. High-*k* material is physically thick without being electrically thicker, leading to the same effect of scaling $SiO_2$ without increasing the leakage current. Many TFT applications like active-matrix liquid-crystal display (AMLCD), active-matrix organic light-emitting diode (AMOLED), bio medical devices etc. also require temperature analysis as it tells the working temperature range of the device. Considering all the above aspects, a 2D simulation of a-ITZO TFT along with its RF and analog analysis is thoroughly done by varying different physical parameters. It is seen that a-ITZO material based TFT is a promising option for future RF and analog devices.

The organization of the work is as follows: Section 2 deals with the TFT simulation approach including dimensions, materials and their properties. Section 3 deals with the simulation result, analysis and discussion about impact of different dielectric material, dielectric material thickness ($D_t$) and temperature (T) on DC, Analog and RF parameters. The application of a-ITZO TFT as resistive load inverter is discussed in Section 4.

## 2 TFT Simulation Approach

Figure 1 shows Bottom Gate Top Contact (BGTC) TFT. Device material parameter used for simulation are tabulated in Table 1 [22, 30–32]. Here, Molybdenum (Mo) is chosen as contact material because of its low work function (4.3-4.9 eV), low contact resistance (5.6-85.5 Ω-cm), high strength, high melting point and low reactivity to ambient condition like moisture, oxygen etc. [33]. The TCAD simulation have been done using ATLAS simulator on 2D grid. Newton method is employed to do the calculations. For carrier transport, drift diffusion and energy balance models have been considered. Fermi Dirac model are used for carrier distribution. The TFT uses disordered semiconductors which has defect states that can trap the charges. So, the models that define defect density are also included. To accurately model this, a continuous distribution of the sub-gap DOS (G(E)) given by Eq. 1, is extended from the valence band edge ($E_V$) to conduction band edge ($E_c$) which include four bands i.e. two tail bands and two deep energy bands and are modeled by Gaussian distribution.

$$G(E) = G_{TA}(E) + G_{TD}(E) + G_{GA}(E) + G_{GD}(E) \tag{1}$$

It is assumed that for a-ITZO, $G(E)$ consist of three bands i.e. $G_{TA}(E)$, $G_{TD}(E)$ *and* $G_{GD}(E)$ [34]. These are given by Eqs. 2, 3 and 4.

$$G_{TA}(E) = N_{TA} \exp\left[\frac{E - E_C}{W_{TA}}\right] \tag{2}$$

$$G_{TD}(E) = N_{TD} \exp\left[\frac{E_V - E}{W_{TD}}\right] \tag{3}$$

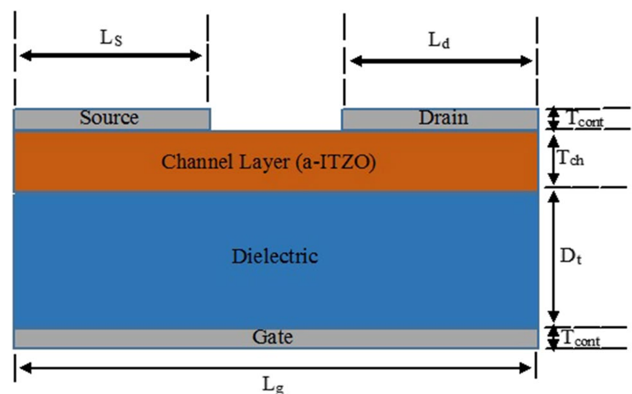



**Fig. 1** Structure of the 2D cross sectional a-ITZO TFT

**Table 1** Material and Density of State (DOS) parameter of a-ITZO

| | | |
|---|---|---|
| a-ITZO Parameters | Band Gap | 3.02 eV |
| | Dielectric Constant | 10 |
| | Affinity | 4.65 eV |
| | Electron mobility | 0.1 $cm^2 V^{-1} s^{-1}$ |
| | Hole mobility | 30 $cm^2 V^{-1} s^{-1}$ |
| | Effective density of states in the conduction band, $N_C$ | 1.59e19 $cm^{-3}$ |
| | Effective density of states in the valance band, $N_V$ | 1.21e19 $cm^{-3}$ |
| | Carrier concentration (N) | 4.62e15 $cm^{-3}$ |
| | Thickness (Tch) | 20 nm |
| Dielectric Parameters | Band Gap, $SiO_2$ | 9 eV |
| | Permittivity, $SiO_2$ | 3.9 |
| | Band Gap, $Si_3N_4$ | 5 eV |
| | Permittivity, $Si_3N_4$ | 7.5 |
| | Band Gap, $Al_2O_3$ | 8.7 eV |
| | Permittivity, $Al_2O_3$ | 9.5 |
| | Band Gap, $HfO_2$ | 5.7 eV |
| | Permittivity, $HfO_2$ | 35 |
| | Thickness (Dt) | variable (nm) (150,200,250,300) |
| a-ITZO, Density of Defects Parameters | Peak density of acceptor-like states, $N_{TA}$ | 1.22e18 $cm^{-3} eV^{-1}$ |
| | Peak density of donor-like states, $N_{TD}$ | 1.30e20 $cm^{-3} eV^{-1}$ |
| | Characteristic decay energy (acceptor-like states), $W_{TA}$ | 0.016 eV |
| | Characteristic decay energy (donor-like states), $W_{TD}$ | 0.20 eV |
| | Peak density (shallow donor Gaussian), $N_{GD}$ | 1.73e16 $cm^{-3} eV^{-1}$ |
| | Decay energy (shallow donor Gaussian), $W_{GD}$ | 0.082 eV |
| | Energy peak (shallow donor Gaussian) $E_{GD}$ | 2.9 eV |
| Source/ Drain/ Gate Parameters | Gate (Molybdenum) Length (Lg)/Width (W) /Tcont | 35 µm /10 µm /0.1 nm |
| | Molybdenum Source and Drain (Ls & Ld/W/Tcont) | 15 µm /10 µm /0.1 nm |
| | Work Function of Molybdenum (Φs) | 4.53 eV |

$$G_{GD}(E) = N_{GD} \exp\left[-\left[\frac{E - E_{GD}}{W_{GD}}\right]^2\right] \tag{4}$$

Where, E is the trap energy and the subscript T, A, G and D stands for tail, acceptor, Gaussian (Deep level) and donor states. To verify the simulation results, the simulation parameters are calibrated with the results available for TFT [34] and obtained in Fig. 2. It can be deduced that TCAD simulation results are in excellent agreement with the results obtained by taouririt et al. [34]. Further, Analog/ RF analysis of a-ITZO TFT by introducing different physical variations have been discussed.

## 3 RF/ Analog Analysis of a-ITZO TFT

This section deals with the calculation and analysis of Analog/ RF performance parameters for a-ITZO TFT using the expressions mentioned in Table 2. The primary Figure of Merits (FOM's) i.e. drain current ($I_{DS}$), $g_d$, $R_O$, $g_m$, TGF, $V_{EA}$, $A_V$, gate to source ($C_{GS}$) and gate to drain ($C_{GD}$) capacitances, $f_T$, $F_{max}$,

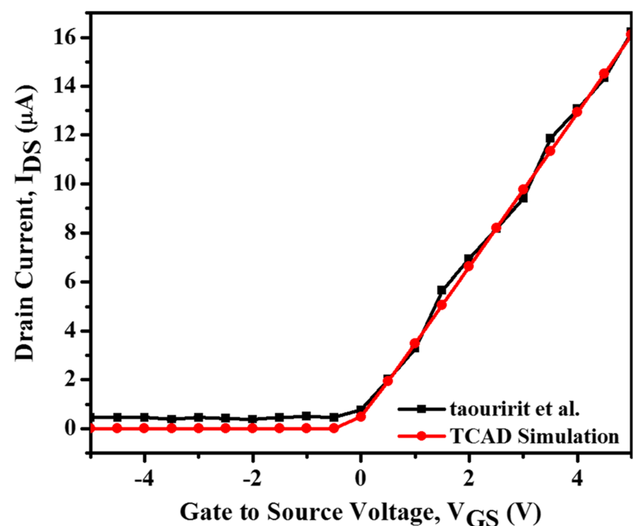



**Fig. 2** Comparison of the transfer characteristics of TFT results reported in [34] and a-ITZO TFT (TCAD simulation) for Drain-to-Source Voltage $V_{DS}$=5 V

TFP, GFP, GBP and GTFP and the impact of physical parameter i.e. dielectric material, dielectric thickness ($D_t$) and temperature (T) of a-ITZO TFT on Analog/RF performance is analyzed in the below subsections.

### 3.1 Impact of High K Dielectric Material on the DC, Analog and RF Parameters

In last few decades, $SiO_2$ was mainly used as dielectric material and have shown good electrical performance. As the technology is changing, there is a need of miniaturized devices to fulfill the requirement of future thin film electronic market. As the device dimensions are scaling down, dielectric layer thickness is also scaling, which has a positive impact on device performance. The dielectric thickness ($D_t$ ) scaling also increases (Eq. 5) capacitance per unit area ($C_{ox}$) that directly increases the drain current of the device [23].

$$C_{ox} = \frac{\varepsilon_o.k_{ox}.L.W}{T_{ox}} \tag{5}$$

Where L, W, $T_{ox}$are the length, width and thickness of dielectric, $k_{ox}$ is the dielectric constant and $\varepsilon_o$ is the absolute permittivity. To solve the thickness scaling problem, high-*k* dielectric material instead of low-*k* dielectric have been used. High-k dielectric material is recognized by Effective Oxide Thickness (EOT) which means that it is electrically thick without being physically thick which results in increased capacitances and reduced leakage current [34]. In this section, the impact of high-*k* material ($SiO_2$, $Si_3N_4$, $Al_2O_3$ and $HfO_2$) on DC, analog and RF performance of a-ITZO TFT have been studied where dielectric thickness ($D_t$) was considered as 200 nm during the simulation.

The plot of different analog/RF parameters with variation in dielectric material is shown in Fig. 3. Figure 3(a-d) shows the variation of $I_{DS}$, gd, $R_O$, $V_{EA}$, $A_V$, gm and TGF for different high-*k* materials. Drain current ($I_{DS}$) in linear and log scale w.r.t. $V_{GS}$ is shown in Fig. 3(a). The peak value of increases from 95µA to 825 µA when the dielectric material changed from $SiO_2$ to $HfO_2$. The electrical parameters are extracted from this curve and tabulated in Table 3. It is seen from Table 3 that  and $I_{on}$/ are mostly affected with this change. Also, there is an increased shift in threshold voltage ($V_{th}$) because of the reduction of surface material potential along the channel [37]. Figure 3(b) demonstrates the output characteristics and drain conduction () for a-ITZO TFT for different dielectric material at $V_{GS} = 5$ V.

The right axis (Fig. 3(b)) depicts the output characteristics and it is seen that when $V_{DS} > 5$ V, the drain current starts to saturate for all the dielectric materials, however it has higher value for $HfO_2$ based TFT. The reason for this change is increased capacitance per unit area because of decreased effective thickness (Eq. 5). The Drain conductance ($g_d$) is derived from output characteristics and is plotted on left axis of Fig. 3(b). The same rise is seen in $g_d$ as that of $I_{DS}$ for $HfO_2$ based TFT. The inverse of $g_d$ is known as output resistance ($R_O$). The inset of Fig. 3(c) shows the variation of $R_O$ with $V_{DS}$ for various dielectric materials. It is found that TFT with $HfO_2$ dielectric has low $R_O$ of 2.95 MΩ as compared to $SiO_2$ based TFT having $R_O$ of 16.86 MΩ. As a result of this, $HfO_2$ based TFT shows superior $I_{DS}$ values than $SiO_2$ based dielectric TFT (Fig. 3(a)).

**Table 2** Symbols and expressions [35, 36]

| Symbol | Quantity | Unit | Expression |
|---|---|---|---|
| $g_d$ | Drain Conductance | S | $g_d = \frac{dI_{DS}}{dV_{DS}} \mid V_{GS}$ = Const. |
| $R_O$ | Output Resistance | Ω | $R_O = \frac{1}{g_d}$ |
| $V_{EA}$ | Early Voltage | V | $V_{EA} = \frac{I_{DS}}{g_d}$ |
| $A_V$ | Intrinsic Gain | dB | $A_V = \frac{g_m}{g_d}$ |
| $g_m$ | Transconductance | S | $g_m = \frac{dI_{DS}}{dV_{GS}} \mid V_{DS}$ = Const. |
| TGF | Transconductance Generation Factor | $V^{-1}$ | TGF $= \frac{I_{DS}}{g_m}$ |
| $f_T$ | Cut-off Frequency | Hz | $f_T = \frac{g_m}{2\prod(C_{GS}+C_{GD})}$ |
| GBP | Gain Bandwidth Product | Hz | GBP $= \frac{g_m}{20\prod C_{GD}}$ |
| $F_{max}$ | Maximum frequency of operation | Hz | $F_{max} = \sqrt{\frac{f_T}{8\prod R_G C_{GD}}}$, Where, ($R_G = \frac{1}{G_{gg}}$) |
| TFP | Transconductance Frequency Product | Hz | TFP = $(\frac{g_m}{I_{DS}})^* f_T$ |
| GFP | Gain Frequency Product | Hz | GFP = $(\frac{g_m}{g_d})^* f_T$ |
| GTFP | Gain Transconductance Frequency Product | Hz | GTFP = $(\frac{g_m}{g_d})$*TFP |

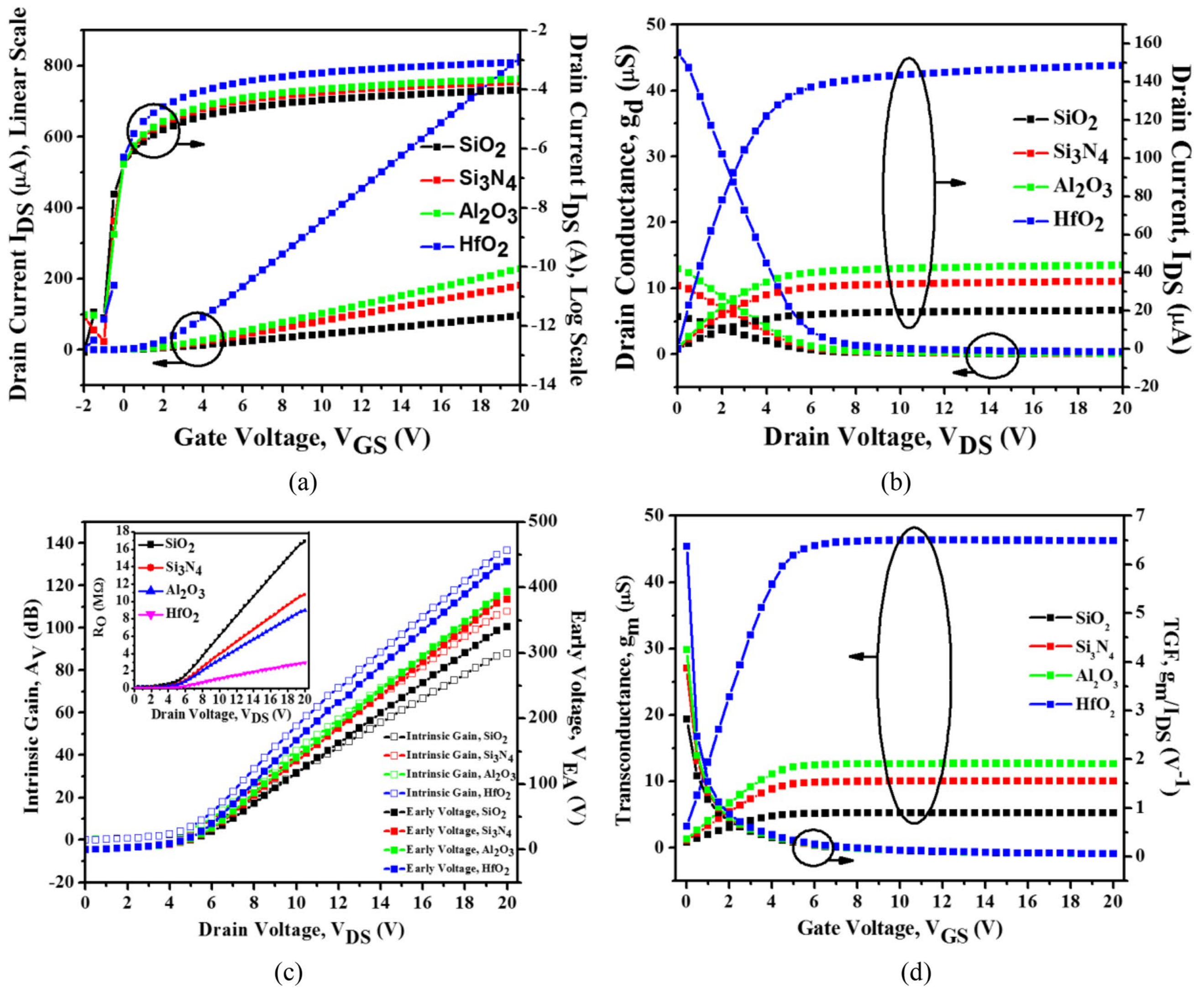



**Fig. 3** **a** $I_{DS}$ (Linear and Log) (**b**) $g_d$ & Output $I_{DS}$ (**c**) $R_O$ (Inset), $V_{EA}$ and $A_V$ (**d**) $g_m$ & TGF for different dielectric materials

**Table 3** Extracted parameters: $V_t$, $V_{on}$, SS, $I_{on}$, $I_{off}$ depending on dielectric material variation

| Dielectric | $V_t$ (V) | $V_{on}$ (V) | Sub-Threshold Swing (V/decade) | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|---|
| $SiO_2$ | 1.75 | -0.70 | 1.0775 | $9.387 \cdot 10^{-5}$ | $2.36 \cdot 10^{-12}$ | $3.97 \cdot 10^{7}$ |
| $Si_3N_4$ | 1.97 | -0.50 | 0.8492 | $1.790 \cdot 10^{-4}$ | $1.75 \cdot 10^{-12}$ | $1.01 \cdot 10^{8}$ |
| $Al_2O_3$ | 2.03 | -0.46 | 0.7945 | $2.262 \cdot 10^{-4}$ | $4.07 \cdot 10^{-13}$ | $5.55 \cdot 10^{8}$ |
| $HfO_2$ | 2.19 | -0.29 | 0.6216 | $8.232 \cdot 10^{-4}$ | $4.11 \cdot 10^{-13}$ | $1.99 \cdot 10^{9}$ |

The analog performance is further analyzed by the graph of early voltage ($V_{EA}$) and intrinsic gain ($A_V$) plotted in Fig. 3(c). The variation in $V_{EA}$ is 29% when dielectric material is changed from $SiO_2$ to $HfO_2$ for a-ITZO TFT. This higher value of $V_{EA}$ has a good sign as it tells that the simulated TFT has better control on channel length modulation and DIBL. The left axis of Fig. 3(c) shows the variation of intrinsic gain ($A_V$) with $V_{DS}$. It is defined as the ratio of transconductance ($g_m$) by drain conductance ($g_d$). An increase of nearly 55% in $A_V$ is observed for $HfO_2$ based a-ITZO TFT as compared to $SiO_2$ material based TFT. The reason for this improvement is that $HfO_2$ will provide high capacitance per unit area with large physical thickness and also provide better immunity to SCE's, that will increase the current and hence it will improve the transistor analog performance parameters $g_m$, $A_V$.

A combined plot of TGF and $g_m$ is drawn as a function of $V_{GS}$ in Fig. 3(d). The left axis of the figure shows that greater value of transconductance (~$10^{-5}$ S) is attained for a-ITZO TFT with $HfO_2$ as dielectric. The increment in $g_m$ with high-*k* material is because of increase in drain to source current of device. Effective use of current to achieve desired value of transconductance is determined by TGF. TGF is a major performance parameter for analog applications which indicates TFT's capability to amplify a signal for a certain $I_{DS}$. The value of TGF also increases with high-*k* dielectric material. This trend follows as that of maximum $g_m/I_{DS}$ is for a-ITZO TFT with $HfO_2$ dielectric followed by $Al_2O_3$, $Si_3N_4$ and $SiO_2$ for $V_{GS} < 2$ V. It is also observed that with increasing $V_{GS}$, TGF value starts to decrease for all configurations. This analysis is very beneficial for circuit designers working on analog applications.

Figure 4(a-d) represent the calculation of RF parameters i.e. $C_{GS}$ and $C_{GD}$, GBP, $f_T$, $F_{max}$, GTFP, TFP and GFP with respect to different dielectric materials. The RF analysis for the a-ITZO TFT is done from AC analysis by including frequency of 1 MHz after post processing of DC solution. The $C_{GS}$ and $C_{GD}$ values for different dielectric material TFT is plotted in Fig. 4(a). It is seen that capacitance values have incremental nature with high *k* material because of the increased fringing field density in the device [36]. The value of $C_{GS}$ and $C_{GD}$ are almost same for $SiO_2$, $Si_3N_4$ and $Al_2O_3$. The variation in $C_{GS}$ and $C_{GD}$ values for a-ITZO TFT for $HfO_2$ dielectric is from 253fF (at $V_{GS} = 0$ V) to 274fF (at

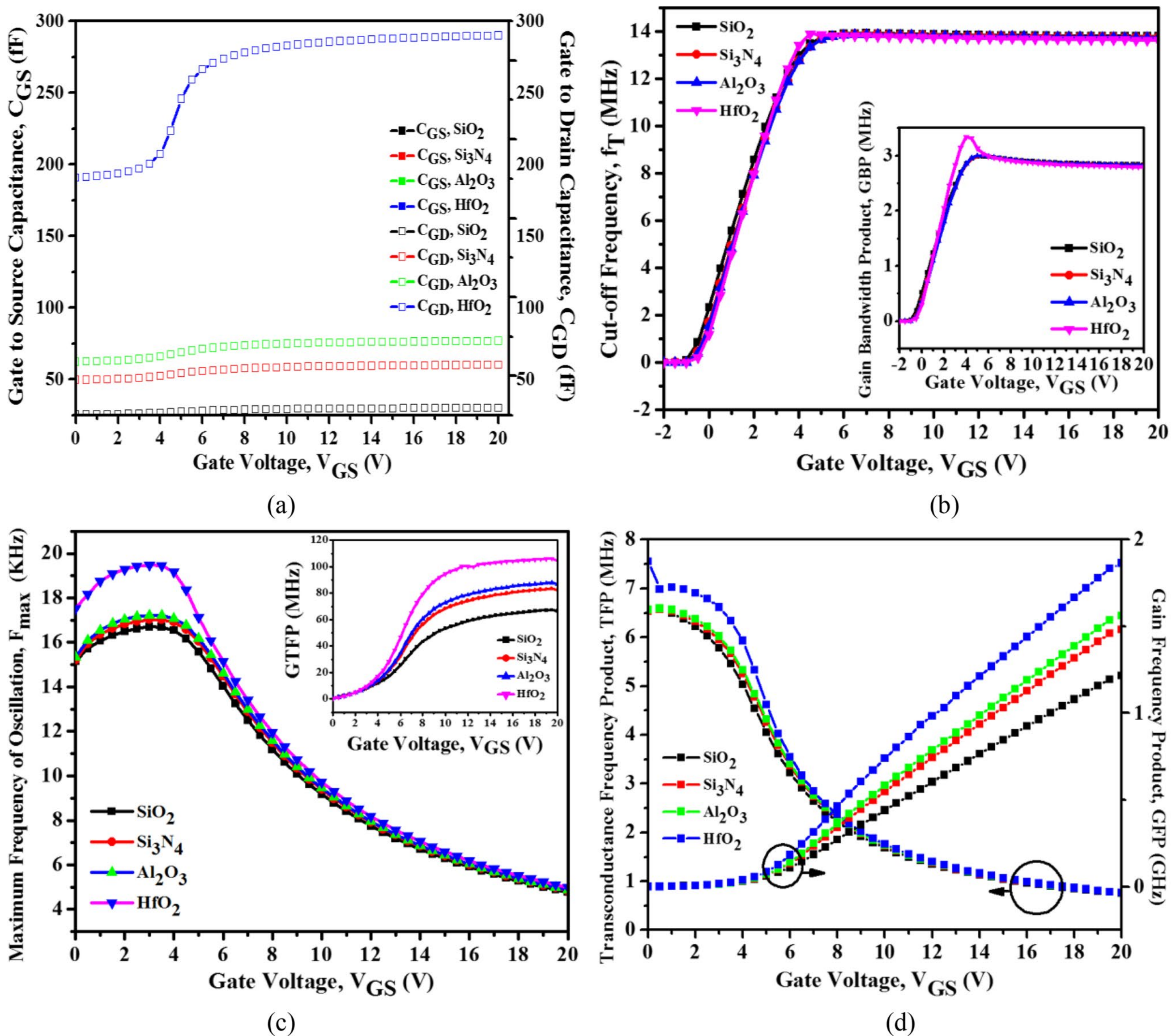



**Fig. 4** **a** $C_{GS}$ & $C_{GD}$ (**b**) $f_T$ & GBP (Inset) (**c**) $F_{max}$ & GTFP (inset) (**d**) TFP & GFP for different dielectric materials

$V_{GS}$ = 20 V) and 176fF (at $V_{GS}$ = 0 V) to 266 fF (at $V_{GS}$ = 20 V) respectively.

Unity gain cut-off Frequency ($f_T$) is another FOM for high-speed digital application. The variation of $f_T$ against $V_{GS}$ in plotted in Fig. 4(b). It is a potential characteristic for devices in defining the acceptable bandwidth range so that they can be used for RF application. As depicted from the Fig. 4(b), there is a slight variation in $f_T$ with changing dielectric material from low to high-*k*. This trend is seen because the rate of improvement in $g_m$ is higher than that of capacitances. Inset of Fig. 4(b) shows the variation of GBP with $V_{GS}$. Close analysis of the curve shows both ($f_T$ & GBP) have same nature with $V_{GS}$. At $V_{GS}$ = 4 V, the peak value of $f_T$ and GBP for a-ITZO TFT with $HfO_2$ dielectric is 13.42 Mhz and 3.34 MHz respectively.

The plot of maximum frequency of oscillation ($F_{max}$) with $V_{GS}$ is shown in Fig. 4(c). $F_{max}$ determines the transit frequency at which maximum power gain is available. $F_{max}$ value shows decreasing trend with $V_{GS}$. The a-ITZO TFT with $HfO_2$ dielectric achieve nearly 0.17 times increase in $F_{max}$ than a-ITZO TFT with $SiO_2$ dielectric. GTFP allows the circuit designers to identify the best region of operation by trading off gain, transconductance and speed. As seen from the inset of Fig. 4(c), GTFP value increases by nearly 55% when using $HfO_2$ as dielectric with a-ITZO TFT than by using $SiO_2$ because of higher value of $f_T$ and $g_m$ for the former.

Figure 4(d) represent the variation of TFP and GFP w.r.t $V_{GS}$ for different dielectric materials. TFP defines the trade-off between power and bandwidth. As seen from the curve that high TFP value is achieved for a-ITZO TFT with high-*k* dielectric at $V_{GS} < 4$ V and after that it is decreased as $V_{GS}$ is increased. GFP as seen from right axis of Fig. 4(d) shows linear rise with the $V_{GS}$. The GFP for a-ITZO TFT with $HfO_2$ dielectric has 0.5 times more GFP value than its $SiO_2$ counterpart.

### 3.2 Impact of Dielectric Thickness ($D_t$) on the DC, Analog and RF Parameters

As deduced from the last analysis, DC, analog/RF parameters are affected by dielectric material. Changing the low-*k* material to high-*k* implies low power, low leakage and high-performance electronic devices. In this section, impact of $D_t$ scaling is seen on different Analog/RF parameters. Thickness of the dielectric material is inversely proportional to capacitance. As the thickness of dielectric material reduces, it increases the capacitance which in turn induces more number of charge carriers at the same output voltage and increases the drain current. $g_m$ will also improve by variation of gate capacitance, which results in reduction of extrinsic delays in digital circuits. Figures 5 and 6 shows the calculation of different Analog/RF parameters of a-ITZO TFT with $HfO_2$ as dielectric material. The device is simulated and compared for different dielectric thickness ($D_t$) = 150 nm, 250 nm, 300 nm and 350 nm.

Figure 5(a) represent the calculation of $I_{DS}$ in linear and log scale w.r.t $V_{GS}$ at $V_{DS}$ = 5 V. The peak value of $I_{DS}$ is 1.1 mA, 824 µA, 661 µA, 552 µA for $D_t$ of 150 nm, 200 nm, 250 nm and 300 nm respectively. The increment in $I_{DS}$ is due to the increase of capacitive coupling between gate and channel with low dielectric thickness. The different parameters like $V_t$, $V_{on}$, SS, $I_{on}$, $I_{off}$ were extracted from the linear and log transfer curves and tabulated in Table 4. The $I_{off}$ state current for all the dielectric thickness is found in the range of $10^{-13}$ to $10^{-14}$. This value is above the requirement of ITRS for low power application.

The right axis of Fig. 5(b) shows output current ($I_{DS}$) w.r.t $V_{DS}$ at constant $V_{GS}$ =5 V for different dielectric thickness ($D_t$). It is evident from the curve that decrease in thickness improves the electrical characteristic and also the performance of the device because of increased dielectric capacitance per unit area [$C_i$]. It is also due to the decrease in the energy band gap of dielectric material [38]. Here, it is seen that all a-ITZO TFT shows excellent saturated characteristic at approx. $V_{DS}$ = 6 V and the thinnest TFT exhibit highest saturation current. The $g_d$ for different dielectric thickness is seen from the left axis of the Fig. 5(b). The $g_d$ for $D_t$ = 150 nm is nearly two times as that of $D_t$ = 300 nm. The increase in $g_d$ is relied to the minimization of short channel effects (SCE's). Inset of Fig. 5(c) shows the variation of output resistance ($R_O$) with $V_{DS}$ for different dielectric thickness. The value of $R_O$ is approximately same (~2.90 MΩ) for all variation of dielectric thickness.

Early voltage ($V_{EA}$) and Intrinsic Gain ($A_V$) are another FOM and their calculation with $V_{DS}$ is represented in the Fig. 5(c). $E_{VA}$ is higher for thinnest TFT i.e. nearly 80% higher than that of $D_t$ =300 nm. The value of $A_V$ is 89.3 dB, 109.2 dB, 137.1 dB and 176.2 dB for dielectric thickness of 300 nm, 250 nm, 200 nm and 150 nm respectively. Both $E_{VA}$ and $A_V$ has higher values for thinner TFT and found its use in fast memory and RF amplification application. $g_m$ as seen from the left axis of Fig. 5(d) shows inverse trend with dielectric thickness. Higher value of $g_m$ is desired to design high performance circuits. It is seen that apex value of $g_m$ increases approximately 2 times when $D_t$ reduced from 300 nm to 150 nm. Right axis of Fig. 5(d) revels that considerable improvement in TGF is seen for a-ITZO TFT with a decrease in dielectric thickness. The lower value of subthreshold swing (0.22 V/decade) exhibit higher value of TGF (6.89 $V^{-1}$) for $D_t$ = 150 nm.

Figure 6(a-d) represent the calculation of $C_{GS}$, $C_{GD}$, $f_T$, GBP, $F_{max}$, GTFP, TFP and GFP with respect to dielectric thickness ($D_t$). Figure 6(a) shows the variation of small signal capacitance $C_{GS}$ & $C_{GD}$ w.r.t $V_{GS}$. The variation in $C_{GS}$ & $C_{GD}$ values for a-ITZO TFT with dielectric thickness

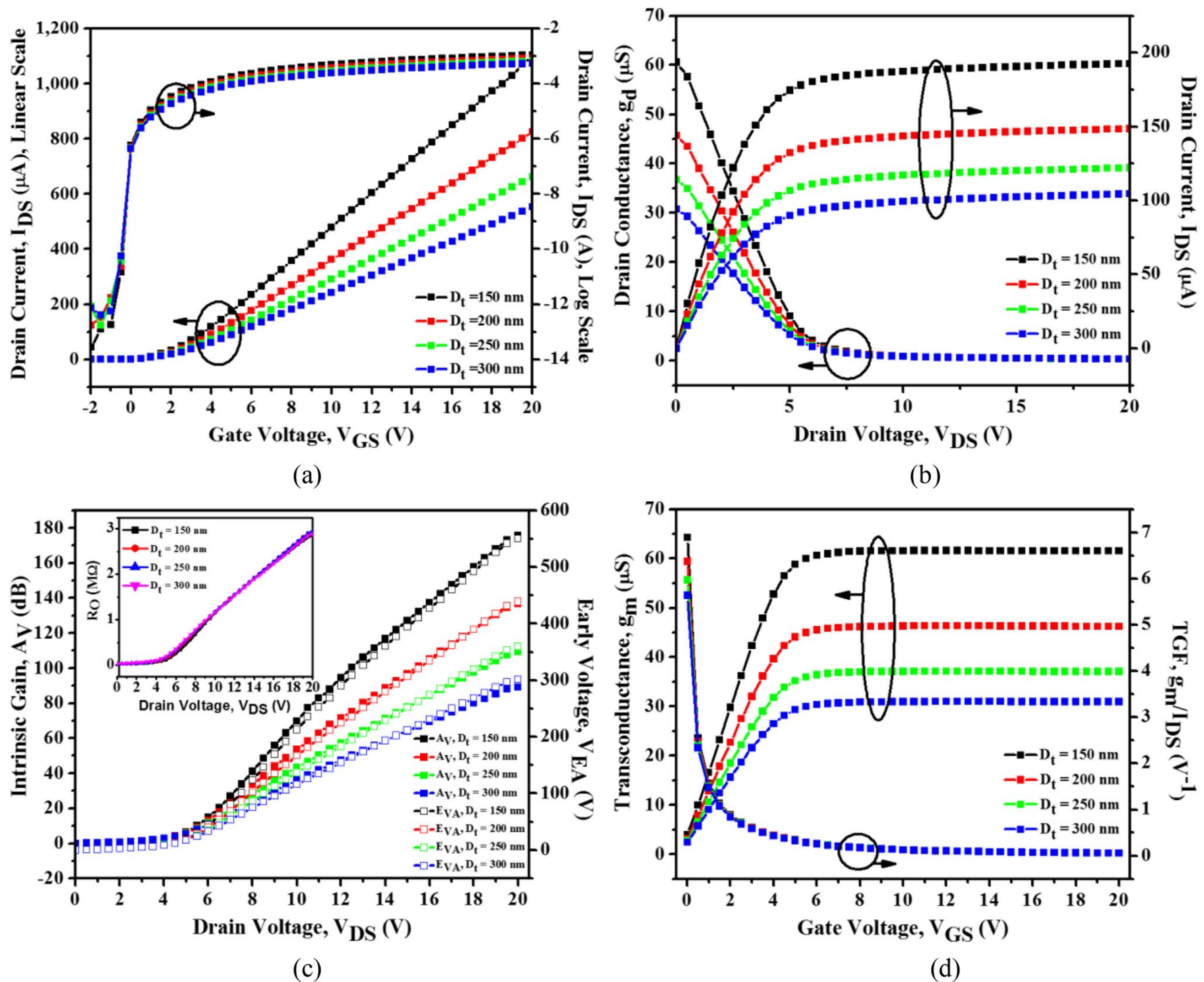



**Fig. 5** **a** $I_{DS}$ (Linear and Log) (**b**) $g_d$ & Output $I_{DS}$ (**c**) $R_O$ (Inset), $V_{EA}$ and $A_V$ (**d**) $g_m$ & TGF for different values of $D_t$

$D_t = 150$ nm is from 220 fF ($V_{GS} = 0$ V) to 365 fF ($V_{GS} = 20$ V) and 214 fF (at $V_{GS} = 0$ V) to 354 fF (at $V_{GS} = 20$ V) respectively. From circuit designer point of view these low values of capacitance are required. These intrinsic capacitances ($C_{GS}$, $C_{GD}$) are used to find cut-off frequency ($f_T$) which is shown in Fig. 6(b). From figure it is seen that a-ITZO TFT with dielectric thickness ($D_t = 150$ nm) yield a peak value of 14.3 Mhz at $V_{GS} = 4.5$ V. GBP with $V_{GS}$ is shown in the inset of Fig. 6(b). The nature of GBP and $f_T$ is similar when $C_{GS} = C_{GD}$ is approximated. a-ITZO TFT using thinner dielectric attains higher GBP. Although the variation is not so much.

The frequency at which power gain is unity is known as maximum frequency of oscillation ($F_{max}$). As evident from the Fig. 6(c), the value of $F_{max}$ decreases as we increase the $V_{GS}$. The maximum value of $F_{max}$ at $V_{GS} = 3.5$ V for dielectric thickness ($D_t$) value of 150 nm, 200 nm, 250 nm and 300 nm is 20.4 kHz, 19.5 kHz, 18.9 kHz and 18.4 kHz respectively. GTFP is defined as the product of intrinsic gain and TFP as shown in the inset of Fig. 6(c). The highest value of GTFP as obtained for $D_t = 150$ nm is nearly two times that of GTFP at $D_t = 300$ nm. Figure 6(d) shows the calculation of TFP and GFP w.r.t $V_{GS}$ for different values of $D_t$. As seen from the left axis of Fig. 6(d) that there is a slight variation in TFP with change in dielectric thickness. The value of GFP as seen from the right axis of Fig. 6(d) are 1.22 GHz, 1.49 GHz, 1.86 GHz and 2.39 GHz for decreasing dielectric thickness from 300 nm to 150 nm in steps of 50 nm respectively. The betterment of all the above RF parameters with $Dt$ is credited to the improved gate control on charge carriers i.e. enhanced electrostatic integrity with decreasing $Dt$.

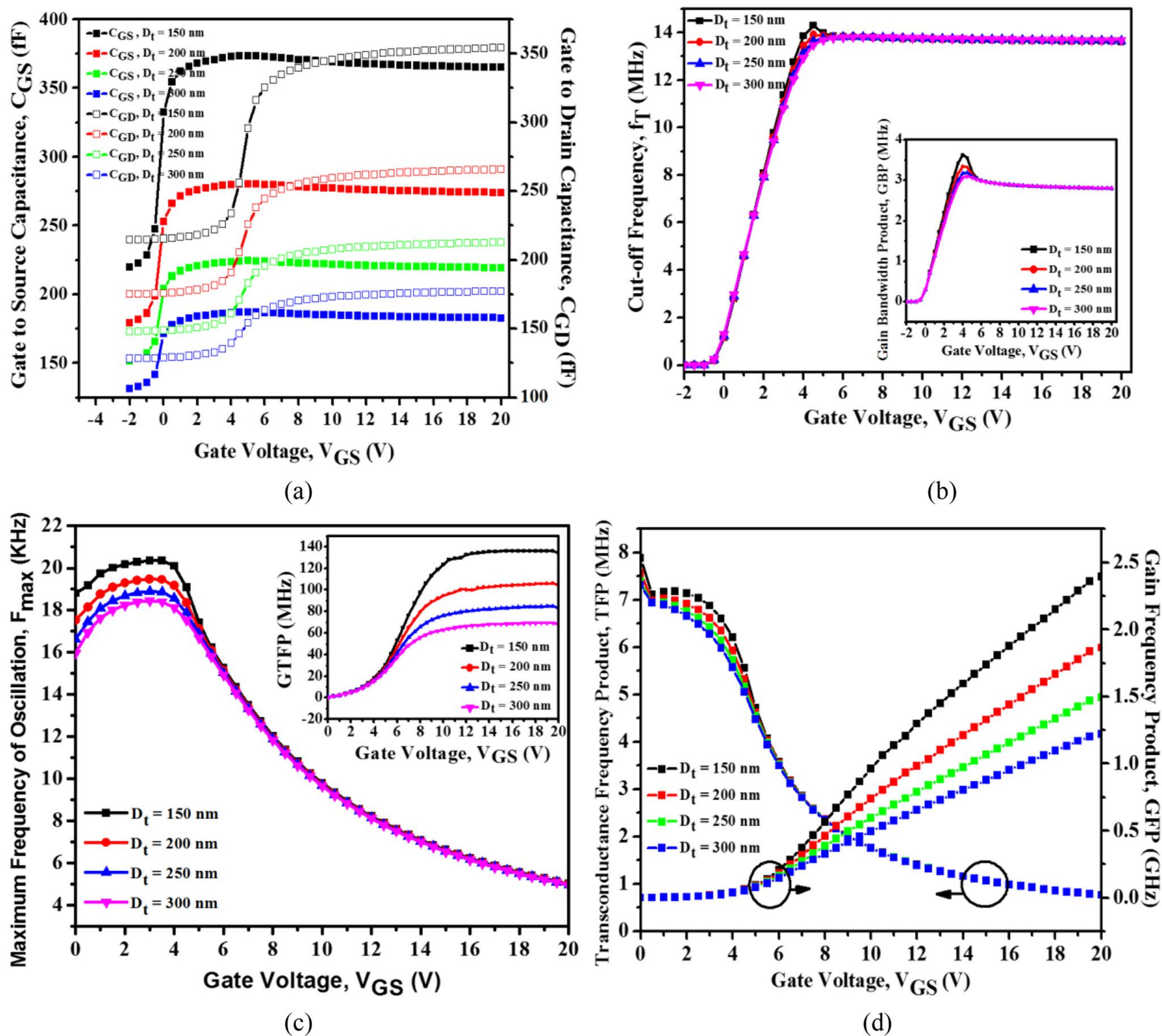



**Fig. 6** **a** $C_{GS}$ & $C_{GD}$ (**b**) $f_T$ & GBP (Inset) (**c**) $F_{max}$ & GTFP (inset) (**d**) TFP & GFP for different values of $D_t$

**Table 4** Extracted parameters: $V_t$, $V_{on}$, SS, $I_{on}$, $I_{off}$ depending on dielectric thickness variation

| Dielectric Thickness (nm) | $V_t$ (V) | $V_{on}$ (V) | Sub-Threshold Swing (V/decade) | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|---|
| 150 | 2.21 | -0.26 | 0.22 | $1.09 \cdot 10^{-3}$ | $2.74 \cdot 10^{-14}$ | $3.98 \cdot 10^{10}$ |
| 200 | 2.19 | -0.29 | 0.62 | $8.24 \cdot 10^{-4}$ | $1.72 \cdot 10^{-13}$ | $4.77 \cdot 10^{9}$ |
| 250 | 2.17 | -0.32 | 0.64 | $6.61 \cdot 10^{-4}$ | $1.75 \cdot 10^{-13}$ | $3.75 \cdot 10^{9}$ |
| 300 | 2.15 | -0.35 | 0.66 | $5.52 \cdot 10^{-4}$ | $4.03 \cdot 10^{-13}$ | $1.37 \cdot 10^{9}$ |

## 3.3 Impact of Temperature on the DC, Analog and RF Parameters

In this section, impact of temperature (T) on various DC, analog and RF parameters is analyzed. In many applications like AMOLED, medical display circuits, Amorphous Oxide Semiconductor (AOS) material plays an important role. The stability and reliability of particular circuit depend on their operating temperature like most of the medical circuits need to work in the range of 300-400 K. For these

applications, temperature stability of AOS TFT must be analyzed. Figures 7 and 8 is obtained here to see the impact of temperature changes on the different analog/RF parameters of a-ITZO TFT.

Figure 7(a) shows the variation of $I_{DS}$ with $V_{GS}$ at $V_{DS}$ = 5 V. It is seen that drain current ($I_{DS}$) in linear scale experience an increase of nearly 85% when temperature changes from 450 K to 300 K. This trend is attributed to (a) electron and hole trapping at the interface between the material, (b) oxygen vacancies and (c) donor like defect creation in ITZO channel [39]. Out of these three, electron and hole trapping at interface will lead to degradation of drain current. Huo et al. [40] also showed the same trend in drain current and they verified their result by UPS experimental analysis which tells electron structure information. Higher UPS attributes that more electrons are trapped and less free electron availability leading to decreased electrical performance with increased temperature. The different parameters used to analyze the TFT performance are extracted from linear and log curves of transfer characteristics (Fig. 7(a)) and tabulated in Table 5. The best result is observed for T = 300 K with $V_{on}$ = -0.29 V, $I_{on}/I_{off}$ = $4.77\times10^{9}$. The $I_{off}$ value is in $10^{-13}$-$10^{-14}$ range for all the temperature variation.

The right axis of Fig. 7(b) shows the output characteristic of a-ITZO TFT. As seen, after $V_{DS}$ = 7 V, the $I_{DS}$ starts to saturate. The value of $I_{DS}$ is 140 μA, 111 μA, 91.5 μA, 77.1 μA for 300 K, 350 K, 400 K, 450 K respectively. The conduction mechanism in AOS TFT is mainly hopping but here it changes to band conduction or percolation in the conduction and $I_{DS}$ reduces as temperature increases [39]. So, trapping plays an important role for analyzing AOS TFT.

The electrical properties of device can be improved based on both the carrier concentration of active layer and interface

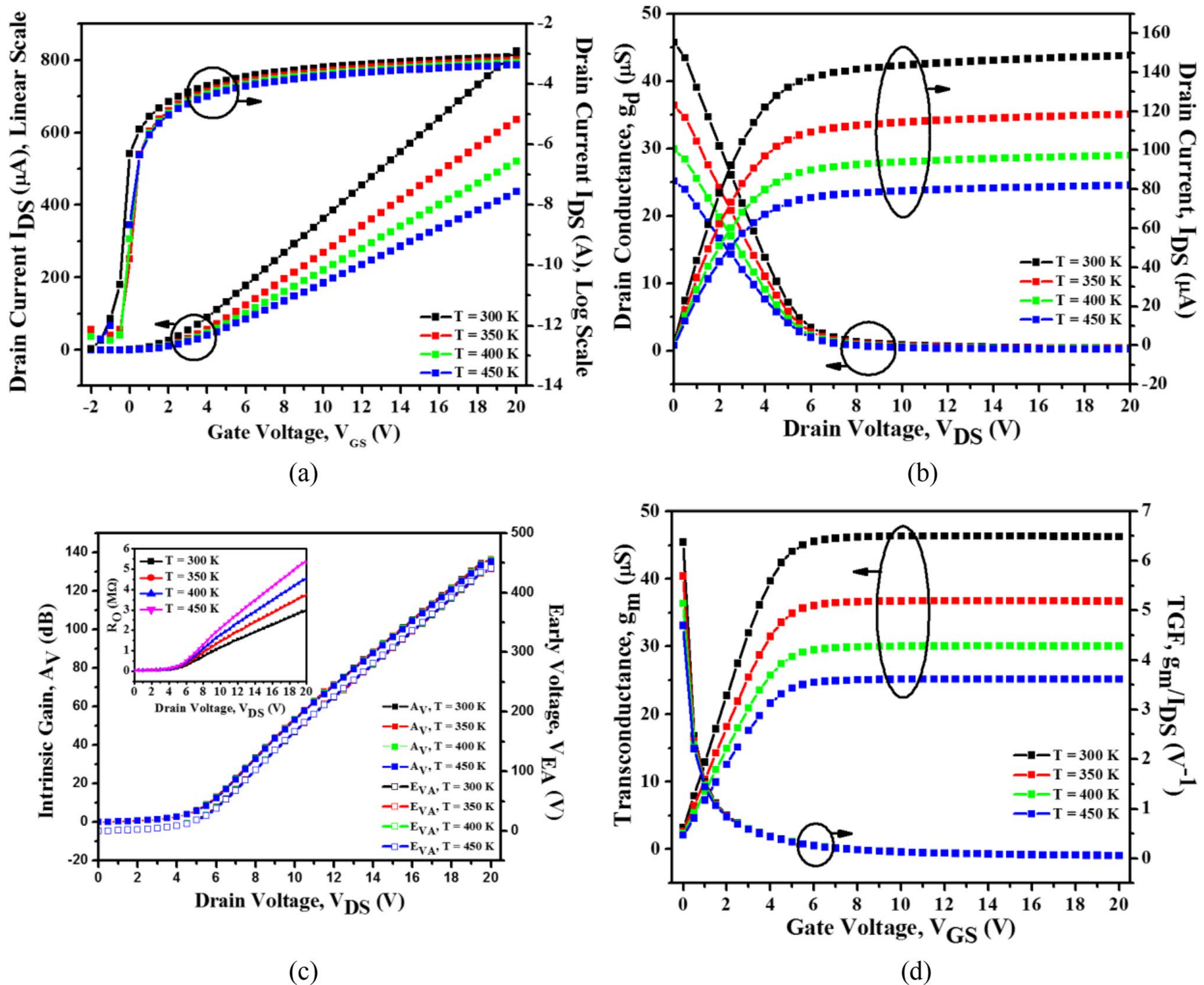



**Fig. 7** **a** $I_{DS}$ (Linear and Log) (**b**) $g_d$ & Output $I_{DS}$ (**c**) $R_O$ (Inset), $V_{EA}$ and $A_V$ (**d**) $g_m$ & TGF for different values of T

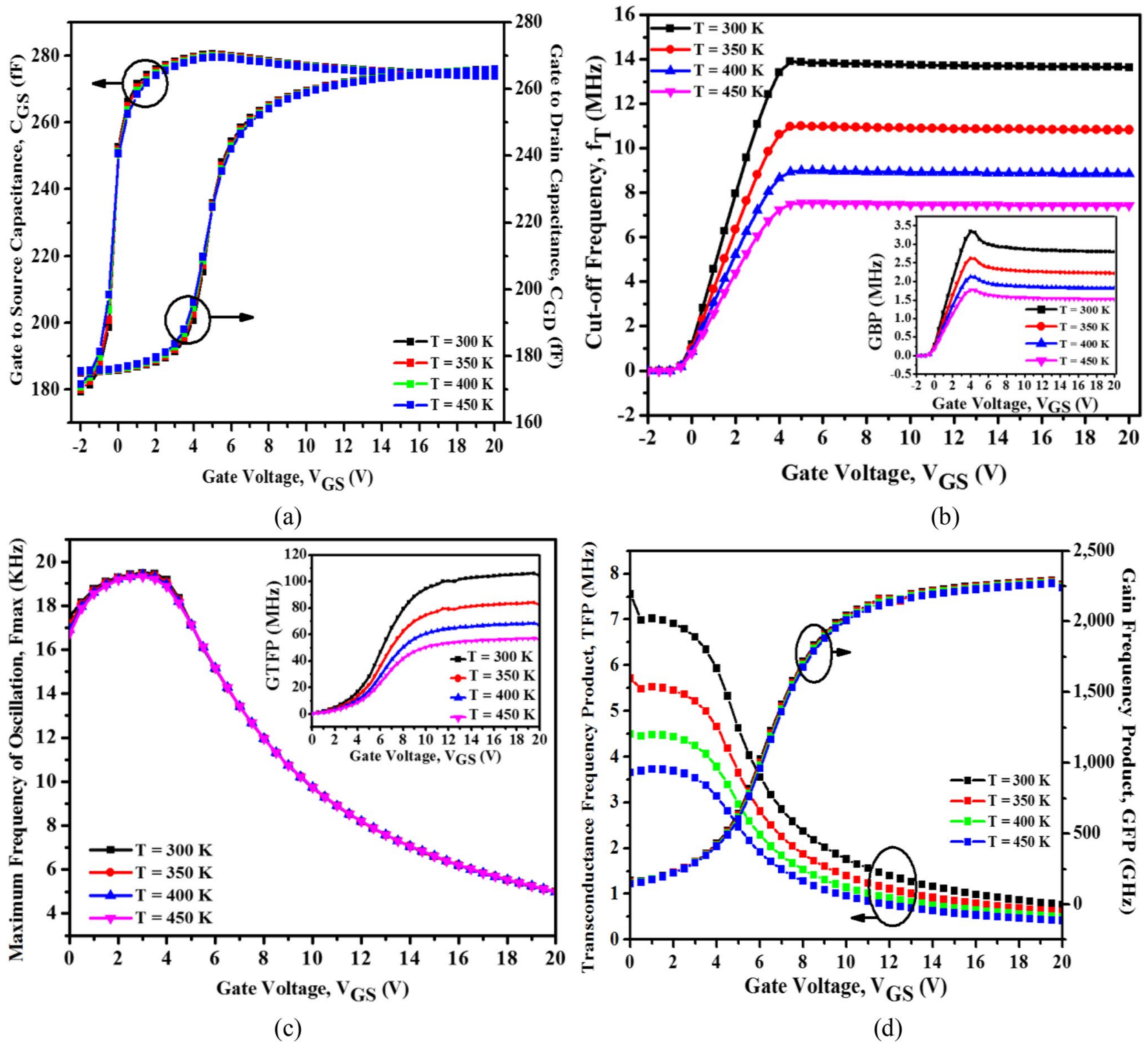



**Fig. 8** **a** $C_{GS}$ & $C_{GD}$ (**b**) $f_T$ & GBP (Inset) (**c**) $F_{max}$ & GTFP (inset) (**d**) TFP & GFP for different values of T

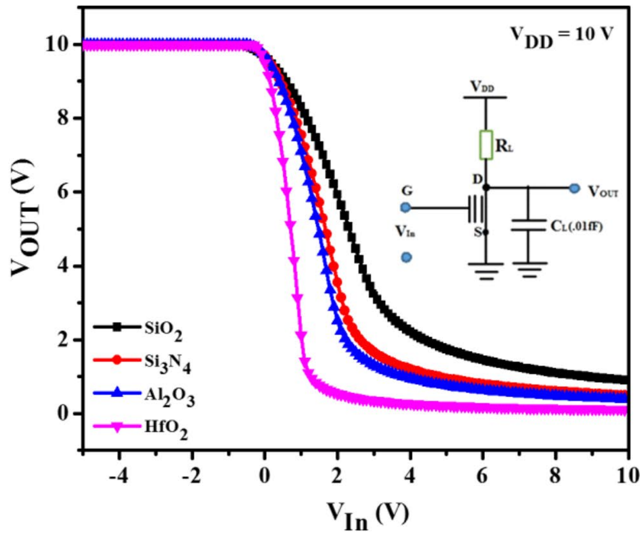
trap density. The interface trap density ($N_t$) can be extracted by subthreshold slope (SS) and is given by Eq. 6 [41]:

$$N_t = (\frac{SS}{\ln 10}\frac{q}{kT} - 1)\frac{C_{ox}}{q} \tag{6}$$

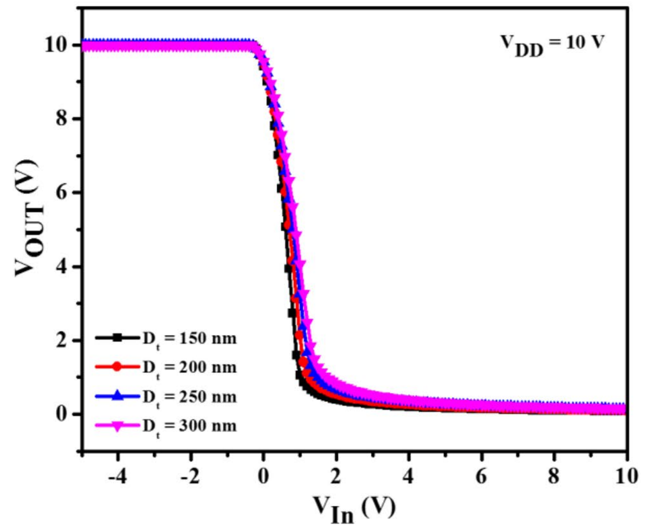
where q is electron charge, k is Boltzmann's constant, T is temperature and $C_{ox}$ is given by Eq. 5. From Table 5, it is seen that reduction in SS with decreasing temperature will lead to reduced $N_t$ and so reason of increased $I_{DS}$ at decreased temperature. The left side of the Fig. 7(b) shows

**Table 5** Extracted parameters: $V_t$, $V_{on}$, SS, $I_{on}$, $I_{off}$ depending on temperature variation

| Temperature (K) | $V_t$ (V) | $V_{on}$ (V) | Sub-Threshold Swing (V/decade) | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|---|
| 300 | 2.19 | -0.29 | 0.621 | $8.24 \cdot 10^{-4}$ | $1.72 \cdot 10^{-13}$ | $4.77 \cdot 10^{9}$ |
| 350 | 2.18 | -0.32 | 0.662 | $6.54 \cdot 10^{-4}$ | $5.30 \cdot 10^{-14}$ | $1.23 \cdot 10^{10}$ |
| 400 | 2.17 | -0.35 | 0.703 | $5.35 \cdot 10^{-4}$ | $2.03 \cdot 10^{-13}$ | $2.63 \cdot 10^{9}$ |
| 450 | 2.16 | -0.38 | 0.744 | $4.48 \cdot 10^{-4}$ | $3.56 \cdot 10^{-13}$ | $1.26 \cdot 10^{9}$ |



(a)



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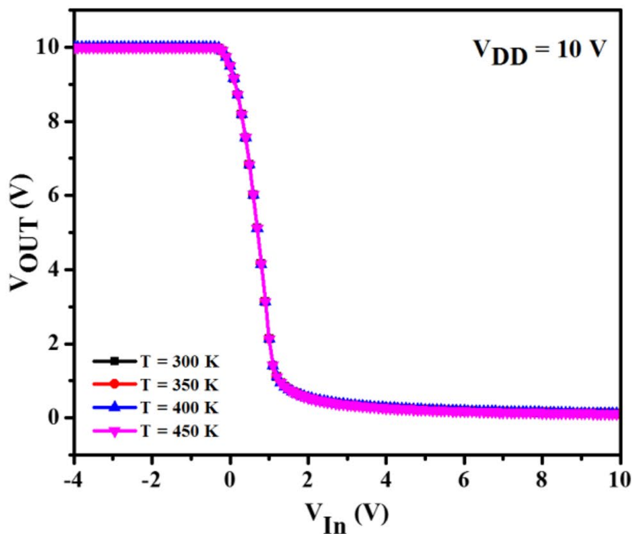
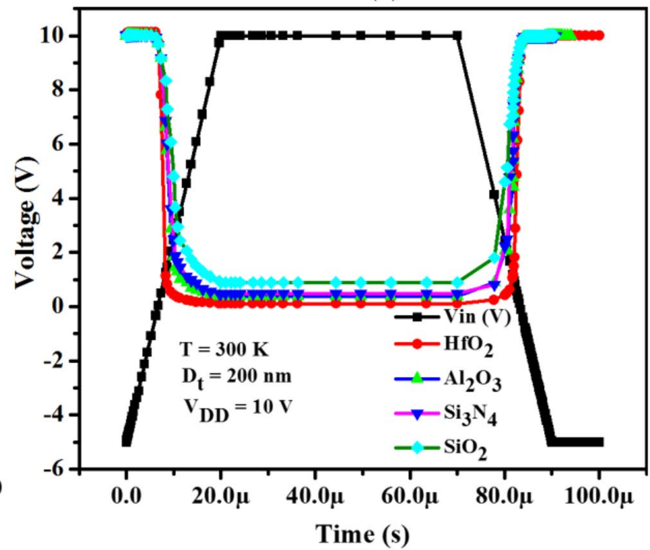
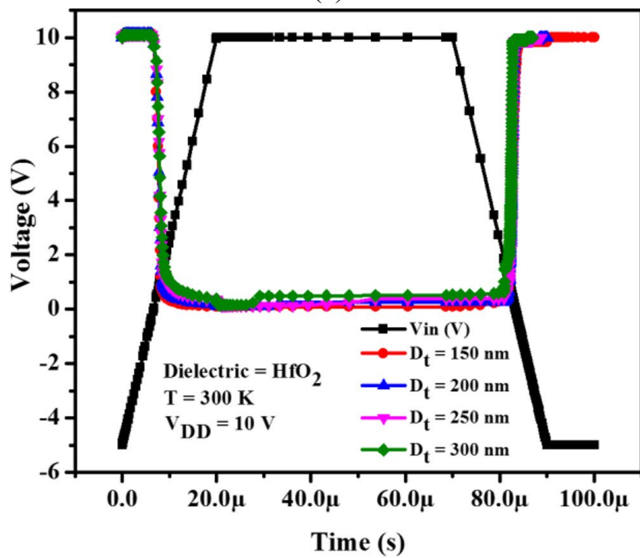


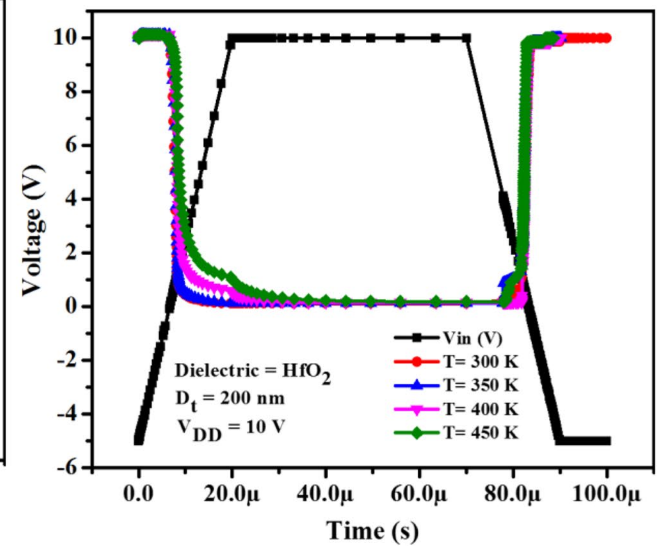
(c)



(d)



(e)



(f)

**Fig. 9** **a**, **b** and **c** VTC curve (**d**, **e** and **f**) Transient curve of the a-ITZO based resistive load inverter (inset of (**a**)) for different variations i.e. Dielectric Material, Dielectric thickness and Temperature respectively

the variation of drain conductance ($g_D$) w.r.t $V_{DS}$. It is also decreasing by nearly 2.2% wih the increasing temperature.

Inset of Fig. 7(c) shows the variation of output resistance ($R_O$) with $V_{DS}$. $R_O$ at T = 450 K is nearly 1.8 times that of T = 300 K. $V_{EA}$ and $A_V$ as seen from Fig. 7(c) shows a very little or no impact with temperature variation. From close examination we can say that analog performance is better for T = 300 K.

Figure 7(d) shows the variation of TGF and $g_m$ with $V_{GS}$. Both TGF and $g_m$ show decremented nature as we increase the temperature. The apex value of $g_m$ at $V_{GS}$ = 4 V are $4.64 \cdot 10^{-5}$ S, $3.67 \cdot 10^{-5}$ S, $3.00 \cdot 10^{-5}$ S, $2.52 \cdot 10^{-5}$ S for T= 300 K, 350 K, 400 K, 450 K respectively. TGF decreases nearly 35% when temperature is changed from 300 to 450 K. The decremented nature is ascribed to decreased mobility with increase in temperature.

Figure 8(a-d) show the variation of different RF parameter with different temperature ranges. The $C_{GS}$ & $C_{GD}$ values as seen from the Fig. 8(a) have shown same nature for all the temperature variations. It is also seen that $C_{GS}$ is greater than that of $C_{GD}$, which can be attributed to uneven distribution of charge on application of drain source bias [42]. The highest value of $C_{GS}$ & $C_{GD}$ is 280 fF and 266 fF respectively, which is very less and beneficial for circuit designing.

The variation of $f_T$ with $V_{GS}$ is seen from Fig. 8(b). Nearly 85% rise is seen in $f_T$ when temperature is decreased from 450 K to 300 K in steps of 50 K. The rise is result of degradation of carrier mobility with increasing temperature which in turn decreases *gm* [43]. GBP as seen from the inset of Fig. 8(b) has shown the same nature as that of $f_T$. GBP has attained peak value of 3.34 MHz at $V_{GS}$ = 4 V for T = 300 K. Figure 8(c) represent the calculation of $F_{max}$ with $V_{GS}$ for different temperature range. The peak $F_{max}$ for all temperature variation is nearly 19.47 kHz at $V_{GS}$ = 3.5 V. The measurement of GTFP with the $V_{GS}$ when swept from 0 to 20 V at fixed $V_{DS}$ of 5 V is seen from inset of Fig. 8(c). The peak value of GTFP at $V_{GS}$ = 20 V are 104.5 MHz, 82.7 MHz, 67.5 MHz and 56.3 MHz for T= 300 K, 350 K, 400 and 450 K respectively. Figure 8(d) is obtained to see the variation of GFP and TFP with $V_{GS}$. GFP as seen from the curve is unchanged for all temperatures. The left axis of Fig. 8(d) shows TFP at T = 300 K is nearly 2.3 times that of TFP at T = 450 K.

## 4 Application of ITZO TFT as Resistive Load Inverter

In this section, a resistive load inverter circuit to see the application of simulated TFT at device level is implemented. As seen in inset of Fig. 9(a), a-ITZO TFT is connected with 1 MΩ load resistor ($R_L$) to examine clear On/Off levels in Voltage Transfer Characteristic (VTC) curve. a-ITZO TFT can be considered as variable register depending on the $V_{GS}$ values. After verifying successful resistive operation, the transistor parameter (dielectric value (high *k*), thickness and temperature) have been varied to observe the respective variations seen in Fig. 9(a), (b) and (c). As deduced from the Fig. 9(a, b and c), the $V_{OUT}$ of VTC is consistent with the transfer characteristics shown in Figs. 3(a), 5(a) and 7(a). It is seen that there is an improvement in VTC by changing the dielectric material to high *k* ($SiO_2$ to $HfO_2$) or by decreasing the thickness of dielectric (300 nm to 150 nm). This change is attributed to increase in mobility and decrease in subthreshold swing value when changing dielectric material to high *k* or decreasing thickness. With temperature the VTC curve shows a constant behavior. The transient response of a-ITZO based inverter is also plotted in Fig. 9(d, e and f) with same parameters variation as in VTC. A ramp input of peak 10 V with 20 µs rise/ fall time is applied to the a-ITZO TFT inverter circuit, here also similar improvement trend is observed as in VTC. This investigation confirms the utility of simulated TFT structure for the designing of next generation logic circuits.

## 5 Conclusion

In this paper, RF and analog performance of an amorphous Indium Tin Zinc Oxide (a-ITZO) thin film transistor have been investigated. The impact of dielectric material, dielectric thickness ($D_t$) and temperature (T) on the DC, Analog and RF parameters of a-ITZO TFT have been studied in detail. The investigations suggest that high *k* materials have potential impact on all Analog and RF parameters. $HfO_2$ as dielectric provides best results in comparison to its low K dielectric siblings. Impact of $D_t$ on all analog and RF parameters have also been reported. Reduction of $D_t$ provides best results and this variation has same impact as that of using high *k* dielectric material. It is also seen that scaling the device dimension leads to increased leakage current. Although, all the variation shows $I_{off}$ value in range of $10^{-13}$ to $10^{-14}$ which in turn provide high $I_{on}/I_{off}$. In last, the stability and reliability of a-ITZO TFT by varying temperature is investigated and it is seen that at T = 300 K, the device provides best results. This is considered as one of the FOM's of the simulated structure as most of equipment's/ devices work on ambient temperature. It is concluded that using high *k* material which has band gap close to $SiO_2$ or thinner dielectric at T = 300 K gives the optimum results. Also, successful implementation of a-ITZO TFT as resistive load inverter indicates that the simulated TFT structure can provide further directions for researchers to design complex analog and RF logic circuits.

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**Data Availability** For this submission, no linked research data sets are there.

## Declarations

**Ethics Approval and Consent to Participate** Taken Informed consent from all authors included in the study.

**Consent for Publication** Taken Informed consent from all authors included in the study.

**Conflict of Interest** The authors declare no competing interests.

**Disclosure of Potential Conflicts of Interest** The authors declare that they have no conflict of interest.

**Research Involving Human Participants and/or Animals** Not applicable.

**Informed Consent** Not applicable.

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