International Journal on Interactive Design and Manufacturing (IJIDeM) (2021) 15:117–119
https://doi.org/10.1007/s12008-020-00736-y

SHORT ORIGINAL PAPER

An experimental-numeric approach to manufacture semiconductor wafer using thick copper front metallization

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Received: 11 March 2020 / Accepted: 6 October 2020 / Published online: 27 October 2020

Abstract
The presented work investigates about the deformation of semiconductor device induced by electrochemical deposited thick copper films. It enhances thermal and electric performances allowing to use copper interconnections without formations of intermetallic layers at the interfaces with consequent reliability improvement. Nevertheless, the induced deformation strongly affects manufacturability, criticizing the integration between different process steps. Experiment based on phase-shift Moiré principle has been performed to better understand the relation between warpage and temperature. Finite element model has been developed to reproduce the phenomenon in order to address the design and the process integration optimizing workability, electrical performances and reliability.

Keywords Power electronics · Manufacturability · Warpage · Finite element model · Process integration

1 Introduction

Thick copper electrochemical deposition (ECD) represents an attractive technology to manufacture front metallization of power semiconductor device. Compared with the nowadays common material for device front metallization, such as aluminium compounds, copper offers better electrical and thermal conductivity, which permit respectively to reduce device resistance and to improve heat dissipation providing better capabilities against electrical overload such as short-circuit. Copper metallization allows an enhanced compatibility between device fabrication (so called "Front-End" manufacturing) and final package assembly (so called "Back-End" manufacturing), improving the product process integration [2]. In fact, copper front metal enables the wire bonding of copper wire on copper device front metal (Cu–Cu), which is more reliable and more performant than Cu–Al or Au–Al systems allowing welding of homogeneous materials and avoiding intermetallic formation and growth at the interfaces [4]. The main technique to produce thick copper film on silicon substrate is the electrochemical deposition (ECD), which is a highly efficient wet process for depositing a uniform layer of metal (like copper) on wafer surface. Even if its properties make copper very attractive as device front metal, the Cu integration into the wafer manufacturing flow is a technical challenge. Deposited copper produces severe wafer warpage, which negatively affects the yield of all subsequent Front-End and Back-End processes in particular it affects the accuracy and the tolerance chain of all the photolithographic processes. The wafer warpage caused by thick Cu layer is mostly due to plastic deformation during annealing. It has been experimentally observed that warpage has no-linear trend versus temperature and that the residual wafer warpage has been generated during the mandatory annealing process. This process serves to make copper softer and to stabilize its grain size, avoiding in this way electromigration issues which can impact on interconnect reliability [3]. The scope of this work is to characterize the warpage induced by 20 μm thick Cu film on a rectangular wafer slice, according to different annealing profiles. A dedicated interferometric non-contact measurements method has been used for characterize warpage. In order to physically understand the not-linear dependency between temperature and warpage, it has been performed a differential scanning calorimetric (DSC) analysis. A finite element model (FEM) has been developed to predict the geometrically stress-curvature relation, considering material not-linearity. Numerical outcomes have been compared with the results of common analytical equations.

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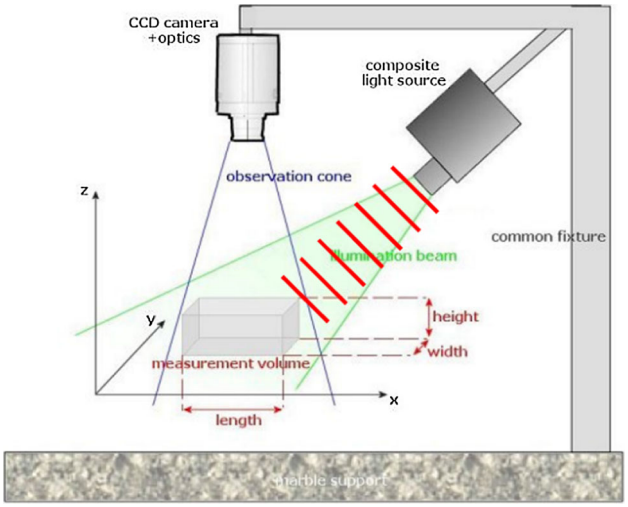

Fig. 1 Schematic of equipment dedicated for warpage measurement

2 Experimental activity

The considered test vehicles were 50 × 10 × 0.75 mm beams, made by silicon substrate 0.73 mm-thick, TiW 0.3 μm, Cu seed 0.2 μm and ECD copper 20 μm-thick. These portions have been sliced from wafer just after copper electro-deposition at room temperature, therefore copper has not been thermally treated before the deformation measurements. The measurements have been performed using an interferometric system, based on "Phase-Shift Moiré" method and described in [1]. Basically, analysed sample is illuminated by a stripped pattern, which is deformed by the sample's surface structure. The resulting image is captured by a CCD camera, that correlates the out-of-plane deformation with xy coordinates (Fig. 1). The desired temperature profiles have been reproduced during warpage measurement, heating sample by the infrared heater and cooling with compressed air. In order to evaluate the impact of heating/cooling rate and maximum temperature, beams were annealed according to different temperature profiles. Analyses show the maximum temperature is the main factor to determine the permanent warpage, whereas the increasing in warpage, during the heating phase, stops at around 150 °C. DSC highlights an irreversible transformation happened at this temperature, which adds to the copper mechanical softening enhanced by increasing temperature.

3 Numerical approach

A Finite Element Model has been developed to calculate the warpage variation, curvature and mechanical stress due to temperature variation and morphological Copper grain growth. Discretization has been performed considering silicon substrate (thickness 730 μm) and ECD copper layer (thickness 20 μm) as 3D hexaedra elements, while TiW and seed copper films have been added in the model including specific 2D shell elements because they are much thinner than other stacked materials. Due to the symmetry of considered samples, it has been modeled only a quarter (25 × 5 × 0.75 mm instead of 50 × 10 × 0.75 mm). In order to reproduce the experimental observed not-linearity, Cu softening has been modelled. Numerical outcomes have been benchmarked with literature approaches [5] and correlated with experimental results, as shown in Figs. 3 and 4.

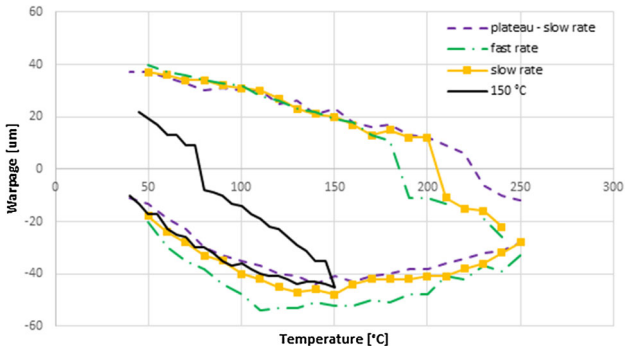

Fig. 2 Measured warpage behaviour, as function of temperature profile

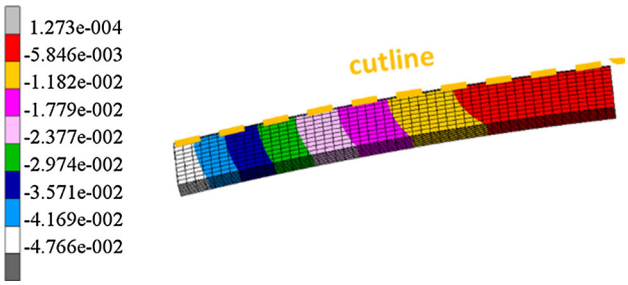

Fig. 3 Simulated warpage contour map (in mm)

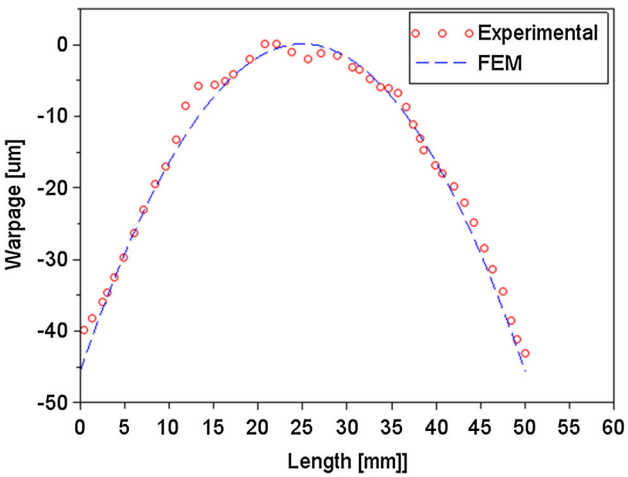

Fig. 4 Warpage along cutline, shown in Fig. 3, at 150 °C, both for FEM and for experimental results

4 Conclusion

The presented approach has been shown maximum temperature as the main factor to establish residual warpage in semiconductor device with Cu ECD films, highlighting involved not-linearities and calculating warpage with numerical approach. The non-linearity is due to Copper grain growth, highlighted by physical investigation and by thermogravimetric (DSC) measurements. Developed methodology is used at design level to minimize warpage variation, by optimizing the ECD copper pattern layout and at process decision making for the selection of the material stack. These factors play a major role to improve the wafer manufacturability and helping the integration among Front-End/Back-End Processes.

Funding Open access funding provided by Università degli Studi di Catania within the CRUI-CARE Agreement. This paper belongs to a research path funded by Università degli Studi di Catania (PIA.CE.RI. 2020-2022 Linea 2 – Progetto Interdipartimentale GOSPEL – Codice 61722102132).

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