Copper/Low-k Interconnects for Smaller and Faster Circuits

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Interconnect technology based on aluminum and SiO_2 has been almost pushed to its limits by the ever-increasing demand for higher functionality devices with higher speed and greater miniaturization. The increase in the speed and packing density of chips is achieved by reducing physical feature size, increasing the number of wiring levels, and enlarging the chip size. The attendant decrease in metal cross sections and reduced wire spacing leads to a dramatic increase in the resistance (R) and capacitance (C) of interconnect structures. For feature sizes less than 0.25 μm, the interconnect RC delay surpasses the gate delay, thereby severely limiting the speed of integrated circuits (ICs). The rise in R and C, with a decrease in interconnect size, has implications far beyond time delays, leading to a host of other problems, such as crosstalk, heat dissipation, and electromigration.[1,2] The trade-off between miniaturization, which calls for reduced metal pitch (width + spacing), and higher performance, which requires increased metal pitch, is a major stumbling block in improved chip design using conventional technology.

In order to meet roadmap projections of continuously decreasing feature sizes (e.g., a 60% reduction from 0.25 μm in 1998 to as low as 0.10 μm by 2007) as well as increasing device speeds (e.g., a 185% increase from 350 MHz in 1998 to 1,000 MHz in 2007),[3] future on-chip interconnects will have to change from the traditional aluminum (or Al-Cu alloy) and SiO_2 designs used pervasively in the electronics industry. New materials for use as metal lines and interlayer dielectrics (ILDs) as well as alternative interconnect architectures can help address these needs. Copper, with its lower resistivity (about 30% lower than that of aluminum), higher thermal conductivity (about 60% higher than that of aluminum) and high electromigration resistance, is an ideal candidate for taking the miniaturization of future on-chip interconnects to a level beyond that possible with Al(Cu)/SiO_2 technology.[1] Substitution of SiO_2 (with a dielectric constant k ~ 4 for a typical chemical-vapor-deposition SiO_2 film) with low-k dielectrics leads to a reduction in C and, in turn, will make increased speed and reduced crosstalk possible. Therefore, replacing Al/SiO_2 with copper/low-k interconnect technology is, at the moment, one of the most promising approaches for enabling further chip miniaturization with concurrent speed enhancement.

Though copper metallization reduces wiring resistance and improves reliability, it brings with it new manufacturing challenges due to four reasons. First, the high diffusivity of copper in both silicon and oxide can cause the destruction of active device regions through junction leakage and voltage drifts. This calls for barrier layers to prevent the copper from reaching the active silicon areas. Second, copper does not lend itself to conventional patterning techniques, such as plasma etching, because it does not form volatile halide by-products. New processing techniques that allow patterning without metal etch (e.g., the damascene process) involving copper deposition into preformed oxide trenches need to be used instead. The high aspect ratios associated with vias will no longer be an issue for metal etch, but will be transferred to oxide etch. Third, the replacement of aluminum with copper makes wafer fabrication more complex and relies on multiple technologies (physical or chemical vapor deposition for deposition of the conductive seed layer and barrier layers or electroplating for bulk-film deposition of copper). Fourth, fundamental differences in the properties of copper as compared to aluminum necessitate changes in processing. Also, the conductivity of copper is extremely sensitive to impurities, necessitating more stringent process control.[2,4]

Low-k dielectric materials can be incorporated into interconnect architectures either as ILDs deposited and planarized next to patterned metal lines or as ILD layers with patterned wiring channels into which metal is deposited later (damascene process). The latter option appears well suited for use with copper metallization. Several materials, such as organic and inorganic polymers, fluorinated silica glasses, and porous materials such as xerogels or aerogels, deposited by processes such as vapor deposition and spin-on coating have been or are being explored for low-k (k < 3) applications. These materials must meet strict requirements with respect to electrical, thermal, mechanical, and chemical properties for integration with either aluminum or copper. In addition to low dielectric constant, they need low water absorption, good chemical and thermal stability, high gap-fill and planarization capability, low dielectric loss, good mechanical properties, minimal CTE mismatch with metal lines, and low leakage current, among others.[5,6]

From the manufacturing point of view, copper/low-k will clearly be the most viable technology for the next step in metallic interconnects. In the upper metal layers, resistance is significant because of the longer interconnect lengths, while in the lower layers, capacitance becomes more important than the metal resistance as the transistor resistance is dominating. So, in the lower layers, the need for low-k dielectric materials takes precedence. Also, there will be reluctance in industry to use copper in the lower metal layers (because of the risk of copper diffusing into silicon) until proven and reliable low-k barrier layers become available. For these reasons, for the 0.18 μm generation, copper will most probably be incorporated only in the upper layers, while for feature sizes of 0.15 μm and below, it is expected that copper, in conjunction with low-k dielectrics, will be used for all the metal interconnects. Beyond the levels of miniaturization and performance achievable by the substitution of Al/SiO_2 with Cu/low-k, other futuristic technologies, such as three-dimensional interconnection architectures, will become necessary. In the near future, however, low-k materials and copper will be key players in making chips smaller and faster.

References

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