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Record Endurance for Single-Walled Carbon Nanotube–Based Memory Cell

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Abstract We study memory devices consisting of single-walled carbon nanotube transistors with charge storage at the SiO_2/nanotube interface. We show that this type of memory device is robust, withstanding over 10^5 operating cycles, with a current drive capability up to 10^{-6} A at 20 mV drain bias, thus competing with state-of-the-art Si-devices. We find that the device performance depends on temperature and pressure, while both endurance and data retention are improved in vacuum.

Keywords Carbon nanotube · Field-effect transistor · Memory · Hysteresis · Endurance · Data retention

Introduction

Carbon nanotube field-effect transistors (CNFETs) and their novel electronic properties have been the focus of intense research in the past few years [1, 2]. A key feature of these devices is the presence of large hysteresis in their transfer characteristics (I_{DS}–V_{GS} curves) between forward and reverse gate sweeps. The hysteresis highly depends on the experimental and the environment parameters such as the gate bias range, gate sweeping rate, and temperature [3, 4]. Despite the difficulty to control it, hysteresis can be conveniently exploited to build simple memory devices [5–13].

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In this paper, we study CNFETs where the single-walled carbon nanotube (SWCNT) has highly transparent contacts to the source and drain electrodes. We show that such transistors can work as memory devices with durability under continuous operation matching or outperforming endurance of Si-devices available on the market. The devices studied exhibit improved durability and charge retention at low temperature and low pressure. Measurements at room temperature show that such robust operation can be achieved also under ambient condition, without any passivation layer to protect the device from exposure to environment.

Experimental

Figure 1 shows the SEM image of a typical device, consisting of an individual carbon nanotube embedded in Pd/Nb (2.5 nm/50 nm) contacts. Carbon nanotubes were grown on the substrate by a catalytic chemical vapour deposition technique, yielding clean and highly crystalline SWCNTs or DWCNTs [14]. The leads were fabricated by photolithography, followed by metal sputtering and lift-off [15], and were separated by a $\sim$2 μm gap. We used a thin Pd layer in direct contact with the nanotube to achieve high transparency contacts between the nanotube and the source and drain electrodes [16]. The degenerately doped Si substrate (0.001–0.005 Ω cm) capped by 400-nm-thick thermally grown SiO_2 layer was used as back-gate.

Results and Discussion

Figure 2a shows the transfer characteristics of a device, displaying an ambipolar behaviour as a consequence of the

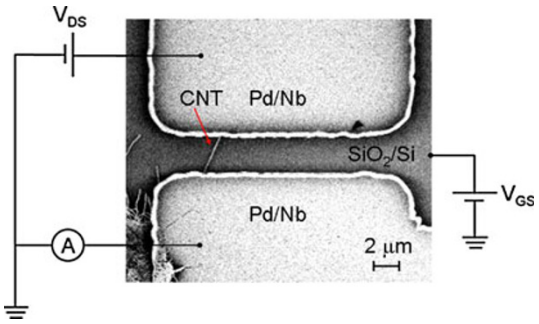

Fig. 1 Schematic of the device used in the study. The leads are made of *Pd/Nb* and the doped *Si* substrate is used as back-gate electrode

small channel bandgap. At room temperature (blue triangle), the CNFET exhibits a small ON/OFF current ratio ($\leq$10) and a low ON-state resistance ($\sim$20 kΩ) saturating at large negative voltage, confirming the high transparency of the contacts. The low ON/OFF ratio is due to the small SWCNT bandgap and can be enhanced by selecting a semiconducting SWCNT with smaller diameter and large bandgap. In our previous work [15, 17], we obtained devices with low contact resistance and large ON/OFF ratio, with the same fabrication process used for the samples discussed here. Because we use nanotubes with a small bandgap, we can test memory device properties for the *same* sample, with very different values of ON/OFF ratio, i.e. smaller ON/OFF ratio at room temperature or larger ON/OFF ratio at low temperature. Indeed, at low temperature (red circles), the ON/OFF ratio increases considerably: the current in the OFF state decreases and the current in the ON state increases. The increase in the ON-state current is due to reduced phonon scattering [18, 19]. The ON-state current of $\sim 10^{-6}$ A for a drain bias as low as 20 mV shows that the CNFET has a higher current drive capability than the present sub-micron Si-based devices [16, 20].

At a given V_{GS}, the hysteresis provides two distinct current values (ON/OFF states) that can be used as the logic levels of an easy-to-build memory device. The FET can be set to the ON state by a positive pulse at the gate (writing operation) and switched to the OFF state by a negative pulse (erasing operation). The states can be safely monitored at $V_{GS} = 0$ V (reading operation). An example of an erase-read-write-read sequence is shown in Fig. 2b.

The shortest width of the $\pm$20 V single pulses that we used for memory switching is 5 ms. Although this switching time is two or three orders of magnitude larger than that of commercial flash memory devices [21], it is similar to switching times of CNFETs with SiO_2 gate oxide reported by other groups [6, 22]. We note that the switching time depends on the characteristic times of the charge traps in the gate oxide. It has been shown that CNTFET memory devices can reach switching times as small as 100 ns, using a different gate oxide [22]. Here, we choose to focus on different properties that are important for data storage.

A memory device must have the robustness to withstand several write-read-erase cycles (endurance) and the ability to retain a certain state over time (retention). We studied these properties in our CNFETs at different temperatures and pressures. Figure 2c shows the data of the cycling test at 77 K and 10^{-5} Torr. The device exhibits remarkable endurance and maintains almost a constant programming window after undergoing $\sim 1.2 \times 10^4$ cycles. The transfer characteristic of this device does not show noticeable change after the test.

The retention times of both the ON and OFF states are tested by continuously recording the drain current in the ON (OFF) state at different temperatures and pressures. The results in Fig. 3d show that after a rapid increase in the OFF-state current during the first hour, the ON and OFF states remain well separated and the retention time exceeds 8–10 h in ambient air and under vacuum at both room temperature and 77 K. At low temperature, the current increase is slower and the separation of the ON/OFF currents is larger.

As described in [13], at least two mechanisms with very different time constants take place in neutralizing the positive charge stored at the SiO_2/SWCNT interface. The I_{DS}–t curves can be explained considering both the shallow and the deep traps at or near the SiO_2/SWCNT interface. Charges stored in the shallow traps have a higher probability of escape by thermal field emission, while charges stored in the deep traps require larger gate electric field to de-trap. Hence, the deep traps effectively help maintain the long-term separation of the two current levels. In addition to the contribution from shallow traps, the rapid change that takes place during the first hour after write (or erase) pulse can be partially due to charges attracted from the surrounding air at the SiO_2/SWCNT interface, which neutralize the stored charge. For the latter reason, low pressure favours current stability as can be seen by comparing the I_{DS}–t curves at 760 Torr and 3×10^{-4} Torr [13, 23]. This suggests that for better device performance exposure to air has to be avoided. In addition, low temperature further improves retention by increasing the ON/OFF current separation.

We also tested the endurance of our devices in air at room temperature, as shown in Fig. 3. The data in Fig. 3a are for the device that was previously tested at 77 K (see Fig. 2c). While this device undergoes $\sim 1.2 \times 10^4$ cycles at 77 K and 10^{-5} Torr by maintaining a constant programming window (Fig. 2c), a steady degradation occurred after 10^3 cycles in a successive test in air as shown in Fig. 3a. The inset in Fig. 3a shows that the window closure

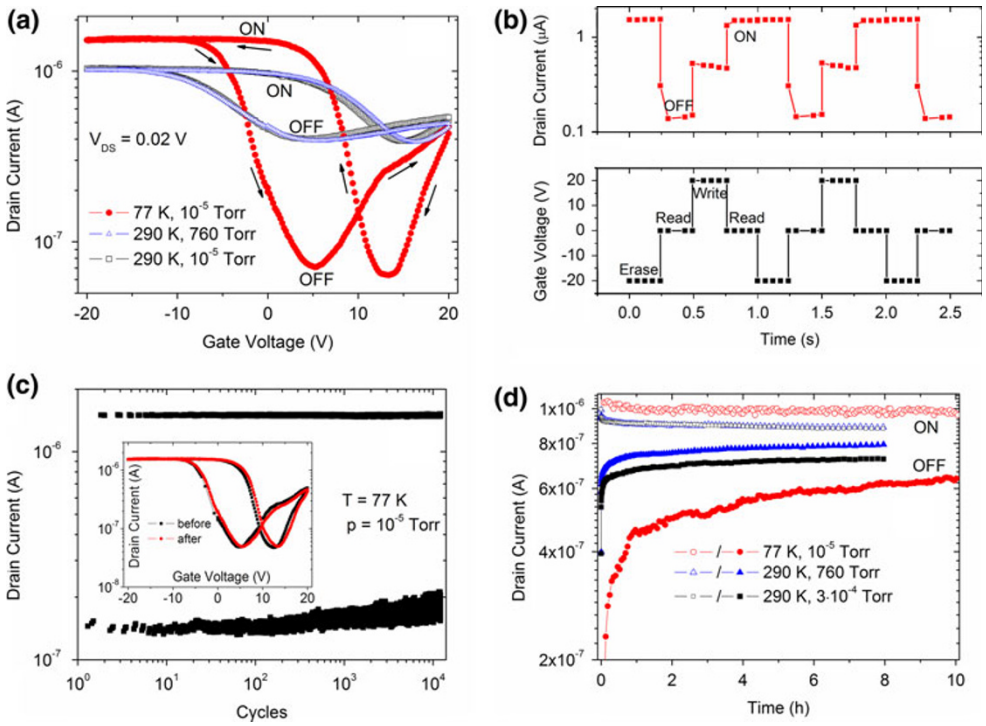

Fig. 2 **a** Effect of low temperature on the transfer characteristic of the SWCNT transistor. Low temperature greatly increases the *ON/OFF* ratio and slightly reduces the hysteresis width. **b** Erase-read-write-read cycles of the SWCNT memory device with ± 20 V and 0.25 s pulses. A negative pulse pushes the memory in the OFF state, while a positive pulse pulls it in the ON state. **c** Endurance tests performed by cycling at 77 K and in vacuum. **d** Retention of states under continuous reading in air (*blue triangle*), at low pressure (*black box*), and at low pressure and temperature (*red circle*). The same device has better retention at low pressure, and the retention is further improved at low temperature which produces a larger separation between the ON and OFF states. Current corresponding to each state was measured at 1-s intervals

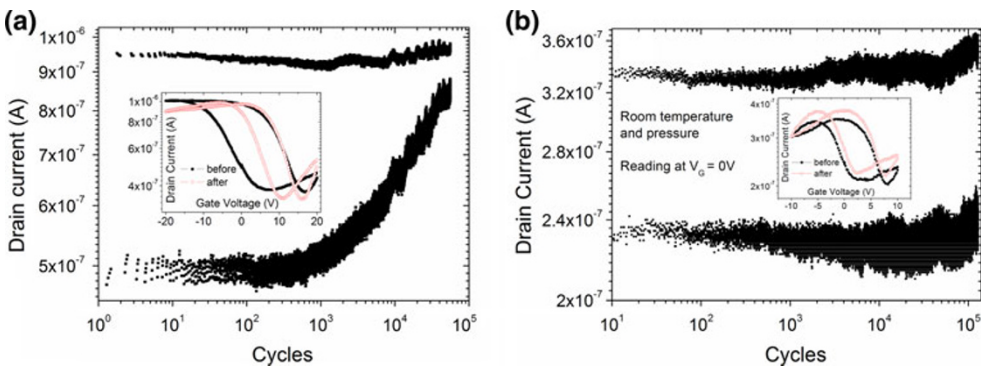

Fig. 3 **a** Endurance tests performed on the same SWCNT memory device as in Fig. 2, at 290 K in air. Switching with ± 20 V and 0.25 s pulses, reading at $V_{GS} = 0$ V. **b** Endurance test of another SWCNT memory device at room conditions with ± 20 V and 0.25-s switching pulses and reading at $V_{GS} = 0$ V

is triggered by the continuous reduction in the hysteresis width. This indicates a deterioration of the charge trapping mechanisms causing hysteresis after the stress test in air, probably due to the formation of additional defects on the oxide surface or to loss of adhesion of the SWCNT to the SiO_2. The extra defects may affect the current propagation in the nanotube and cause additional scattering, thereby decreasing the ON current at large negative gate voltage (see inset in Fig. 3a). We note that if the reading was done at a different gate voltage (for example 8–10 V), or if we monitored the threshold voltages rather than the current, we may have observed an almost constant programming window even beyond 8×10^4 cycles.

The hysteresis degradation after the stress test in air does not occur in all the samples. We cycled a second SWCNT memory from the same production batch and with comparable channel resistance, kept at room temperature and atmospheric pressure. Figure 3b shows that the device has no obvious degradation after more than $\sim 1.2 \times 10^5$ erase-read-write-read cycles, outperforming the specification of the memory devices presently on the market. Therefore, we rule out the hypothesis that the change of hysteresis after

the cycling test in air for the device in Fig. 3a is due to the ionization of air by the high electric field, as suggested in [5].

Conclusion

In summary, to our knowledge, the best endurance under continuous operation ever reported for SWCNT memory is 1.8×10^4 cycles [22] before device failure. Our devices showed remarkable endurance beyond 10^5 cycles in air, which can be considered as a breakthrough for CNT memory devices. We do not believe that the low ON/OFF ratio of our CNFET favours its endurance, since it increases the total amount of charge passed through the nanotube during the long cycling. Instead, the low contact resistance and the good quality of the SWCNT channel could prevent excessive self-heating of the SWCNT and its electric breakdown due to burning by oxidation (which usually happen above 600°C), as observed in other similar studies [22, 24].

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