Nanoscale Res Lett (2009) 4:1434–1438
DOI 10.1007/s11671-009-9416-5

NANO EXPRESS

SnO_2 Nanowire Arrays and Electrical Properties Synthesized by Fast Heating a Mixture of SnO_2 and CNTs Waste Soot

Zi-Jiong Li · Zhen Qin · Zhi-Hua Zhou · Li-Ying Zhang · Ya-Fei Zhang

Received: 3 November 2008 / Accepted: 12 August 2009 / Published online: 25 August 2009

Abstract SnO_2 nanowire arrays were synthesized by fast heating a mixture of SnO_2 and the carbon nanotubes waste soot by high-frequency induction heating. The resultant SnO_2 nanowires possess diameters from 50 to 100 nm and lengths up to tens of mircrometers. The field-effect transistors based on single SnO_2 nanowire exhibit that as-synthesized nanowires have better transistor performance in terms of transconductance and on/off ratio. This work demonstrates a simple technique to the growth of nanomaterials for application in future nanoelectronic devices.

Keywords SnO_2 nanowires · Semiconducting · Field-effect transistor

Introduction

One-dimensional semiconductor nanowires and nanotubes have stimulated increasing attention in the last few years and are expected to lead to novel device application due to their intriguing properties and potential applications in constructing nanoscaled electronic and optoelectronic devices [1–12]. Among semiconducting oxide nanostructure, SnO_2 nanowires, nanobelts, and nanowires are very important n-type semiconductors for applications as transparent conducting electrodes [12], gas sensors [13], and lithium-ion batteries [14], which utilize the unique characteristics of SnO_2 nanostructures including a wide band gap ($E_g = 3.6$ eV at 300 K) and large surface-to-volume ratios. A precondition for SnO_2 nanostructures based on the applications is an easy and lager-scale synthesis of SnO_2 nanostructures. Several methods have been reported for the synthesis of SnO_2 nanowires/nanobelts, including thermal decomposition [15], electrospinning [16, 17], solution-based crystal growth [18, 19], laser ablation, and template-based approaches [20]. However, those methods always required long time for heating and cooling, which hinder the mass production of SnO_2 nanostructures. Due to its versatility and simplicity, the synthesis method of SnO_2 nanowires is still investigated [21].

The electrical properties of SnO_2 nanowires and nanobelts are also reported [22, 23]. Field-effect transistors (FETs) based on single carbon nanotube, Si nanowire, ZnO nanowire and others are with excellent properties superior to their bulk counterparts [24, 25]. SnO_2 nanowires are one of the potential semiconducting materials for nanoelectronic devices due to their excellent electronic properties. In the present study, we report a novel method to synthesize aligned SnO_2 nanowires by using high-frequency inductive heating furnace. A mixture of SnO_2 and the carbon nanotubes (CNTs) waste soot which was a main by-product in the production of CNTs by arc-discharge. The electrical properties including application in FETs of SnO_2 nanowires were also studied.

Z.-J. Li (✉)
Department of Physics, Zhengzhou University of Light Industry, 450007 Zhengzhou, People's Republic of China
e-mail: zijiongli@hotmail.com

Z.-J. Li · Z.-H. Zhou · L.-Y. Zhang · Y.-F. Zhang
Research Institute of Micro/Nanometer Science & Technology, Shanghai Jiao Tong University, 200240 Shanghai, People's Republic of China
e-mail: yfzhang@sjtu.edu.cn

Z. Qin
College of Mathematics and Information Sciences, North China Institute of Water Conservancy and Hydroelectric Power, 450011 Zhengzhou, People's Republic of China

Experimental

The fabrication of nanowires was carried out in a high-frequency introduction furnace. The schematic diagram of the apparatus is shown in Fig. 1. The SnO_2 nanowires were synthesized on a silicon substrate by heating pure SnO_2 powders (50 wt.%) and CNTs waste soot (50 wt.%) which was a main by-product in the production of CNTs at 1,027 k in the quartz tube. An appropriate amount of source powders (about 1 g) and the silicon substrate separated by 10 cm were put in the center of the quartz tube. The silicon (100) substrate patterned with Au using conventional photolithographic method was located downstream of the source powders. The precursor was loaded in a graphite boat and located in a high-purity graphite tube. As a heating crucible, the graphite tube was placed in a horizontal quartz tube and heated in a high-frequency induction furnace. The quartz tube was first evacuated at 10^{-2} Torr by a vacuum pump. After heated up to the desired temperature (1,027 K), an Ar gas flow at a rate of 20 SCCM was introduced, and the growth was initiated and maintained for less than 3 min. When the system was cooled to room temperature, many white products were formed on the surface of the substrate.

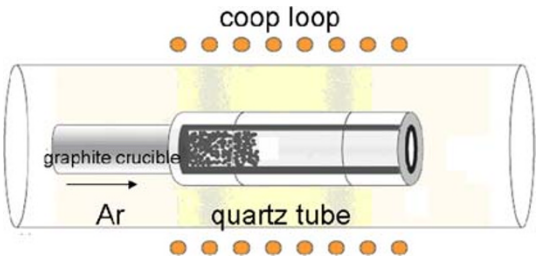

Fig. 1 Schematic diagram of the apparatus for synthesis of SnO_2 nanowires

The as-grown SnO_2 nanowires were characterized by scanning electron microscopy (SEM, FEI SIRION 200) equipped with energy-dispersive X-ray spectroscopy (EDX, INCA OXFORD) and transmission electron microscopy (TEM, JEM-2010). The electronic measurements were made using an Agilent 4156C semiconductor characterization system under an ambient condition at room temperature.

Results and Discussions

Figure 2 is the morphology of as-synthesized nanowires. Figure 2a and b show two typical SEM images of the

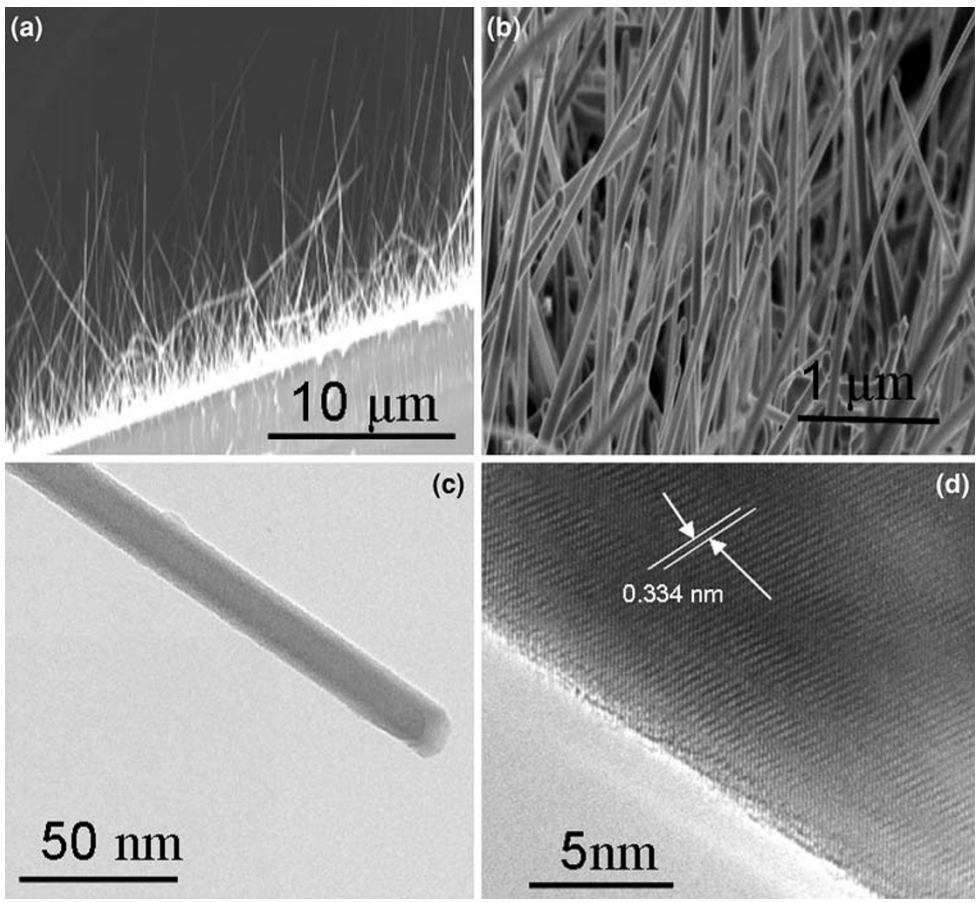

Fig. 2 **a**, **b** The typical SEM images of as-synthesized aligned SnO_2 nanowires, **c** low-magnification TEM, and **d** HRTEM image of single SnO_2 nanowire

as-grown SnO_2 ordered nanowire arrays deposited on the silicon substrate. It can be observed that large quantities of nanowires were grown vertically on the silicon substrate and formed the SnO_2 nanowire arrays with the length of tens of mircrometers, and the surfaces of the nanowires are uniform and smooth. Structural properties of the nanowires were further studied with TEM. Figure 2c shows a low-magnification TEM image of single SnO_2 nanowire with diameters ranging from $\sim$20 nm. It can be seen that the SnO_2 nanowire is very smooth, straight, and uniform, and the geometrical shape is structurally perfect. The crystallography of the nanowires was investigated by select area electron diffraction (SAED) pattern. High-resolution TEM (HRTEM) (Fig. 2d) shows that the as-synthesized SnO_2 nanowire is single crystalline. The interplanar spacing is about 0.334 nm, which is corresponding to the (110) plane of rutile crystalline SnO_2.

Figure 3 shows X-ray diffraction (XRD) patterns of SnO_2 nanowires. All the diffraction peaks can be indexed to the tetragonal rutile structure of SnO_2. The SnO_2 lattice constants obtained by refinement of XRD data are $a = 4.737$ Å, $c = 3.185$ Å, which are consistent with bulk rutile SnO_2 tetragonal structure [26]. It indicates that SnO_2 nanowires are in excellent accordance with a rutile structure. To study the composition of single as-prepared nanowire, EDS measurements (Fig. 4) have been performed on individual nanowire. All the resultant nanowires are mainly composed of Sn, O, and C (come from CNTs).

Figure 5 shows the FT-IR spectrum in the range of 1,000–4,000 cm^{-1} of as-synthesized SnO_2 nanowires. It shows dominant peaks at 1,635, 2,377, 2,925, 3,467, and 3,865 cm^{-1} which corresponds to Si–O, Sn–O, C–O, CNT, H–O–H, and C–H_x, respectively [27, 28]. The peak near 1,635 cm^{-1} can be assigned to the vibration of O–Sn–O that corresponds to the A_{2u} mode [29]. The peaks near

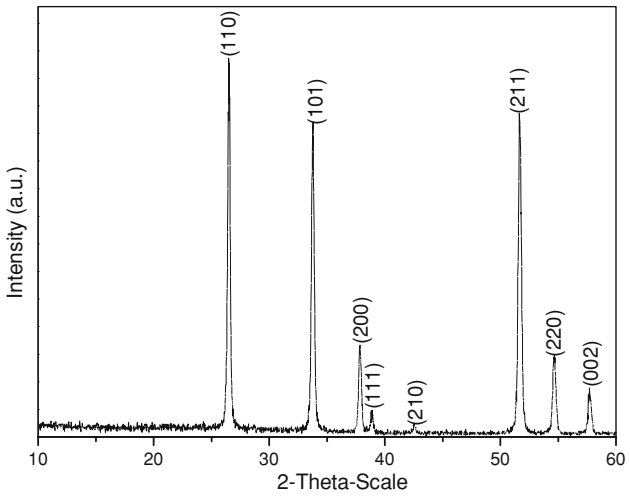

Fig. 3 X-ray diffraction patterns of as-synthesized SnO_2 nanowires

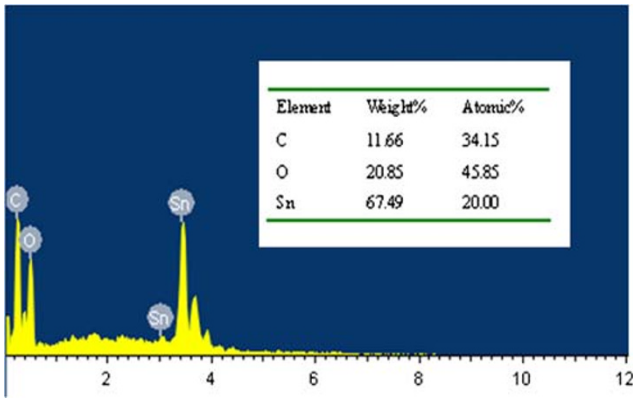

Fig. 4 EDS patterns of as-synthesized SnO_2 nanowires

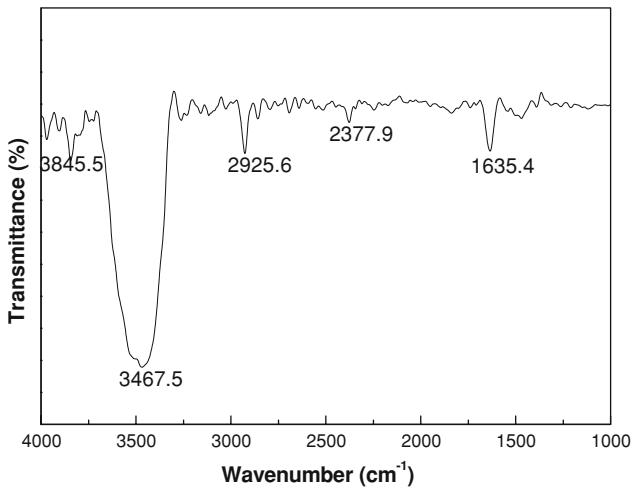

Fig. 5 FT-IR spectrum of as-synthesized SnO_2 nanowires

2,370 cm^{-1} agreed with stretching vibrations of Sn–O bonds [30].

These peaks confirm that SnO_2 nanowires possess the crystalline structure of the tetragonal rutile structure, which is corresponding to the results of XRD.

The growth mechanism of these aligned SnO_2 nanowires follows the conventional vapor–liquid–solid during the experiment. In terms of this mechanism [31], there exist three processes. First, SnO_2 powders react with CNTs waste soot powder, which results in the formation of SnO gas under high temperature. Subsequently, SnO gas will decompose to Sn and O_2 at a temperature higher than 1,027 K. Some Sn droplets reacted with the Au particles and formed Au–Sn alloyed droplets. These alloyed droplets can provide the energetically favored sites for formation of SnO_2 nanowires. Finally, aligned SnO_2 nanowires were produced by the reaction with Sn and O_2 during the process of transporting the Sn to the substrate by carrier gas. Moreover, the temperature is reached in several short seconds during high-frequency induction heating process,

which results in eliminating the dimensional growth of the Au species present on the surface, so it gives rise to the formation of SnO_2 nanowires, while other nanostructure products can not be formed. The following chemical reaction equations are proposed to explain the growth mechanism:

$$SnO_2(s) + C(s) = SnO(g) + CO_2(g) \quad (1)$$

$$2SnO(g) = 2Sn(l) + O_2(g) \quad (2)$$

$$Sn(l) + O_2(g) = SnO_2(l) \quad (3)$$

After growth, the SnO_2 nanowires were transferred from silicon substrates, and a number of FETs device structures were fabricated. Devices were fabricated by thermally growing SiO_2 film with 500 nm thickness on the top of n-type Si wafers, followed by deposition of an Au layer with sputtering and standard photolithography. Parallel Au electrode pairs, with $\sim$1 μm in length and 80 nm in thickness, were patterned. The parallel Au electrodes will be used as source and drain electrodes. An n-type silicon layer serves as the back gate. The as-prepared SnO_2 nanowires were sonicated into a suspension in ethanol, followed by solution casting the slightly dispersed SnO_2 nanowires between the drain and the source of Au electrodes to form a single SnO_2 nanowire FET (SnO_2-FET). The SnO_2-FET samples were quickly transferred to a stove to anneal in Ar at 973 K for 5 min in order to improve the quality of Au–SnO_2 contacts. The inset in Fig. 3 is the SEM image of the as-fabricated single SnO_2 nanowire with a channel width of $\sim$200 nm.

The current–voltage of drain and source (I_{ds}–V_{ds}) data of the device are shown in Fig. 6. The gate voltages were applied from 0 to 9 V and the drain voltages were from −1.0 to 1.0 V for room temperature samples. It is very clearly shown that we have demonstrated that the conductance increased with the increase of the back gate voltage, which indicates an n-type property for the SnO_2 nanowire. The possible reason is due to oxygen vacancies and extra gallium interstitial atoms in the lattice during the synthesis process [32]. An on/off current ratio (I_{on}/I_{off}) of more than 10^5 has been achieved at V_{gs} from −1 to 1 V with V_{ds} of 0.2 V. The FETs based on single SnO_2 nanowire exhibited better electrical properties, which affected both on/off current ratio and threshold voltage of the devices. Figure 6. shows a typical I_{DS}–V_{DS} characteristic of single SnO_2 nanowire FETs. The mobility can be calculated from the following formula [33–35]

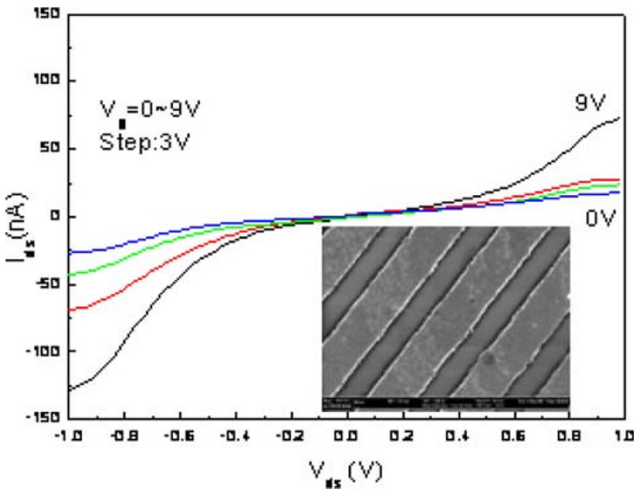

Fig. 6 Transistor characteristic of back-gated single SnO_2 nanowire FET devices on silicon substrates: I_{ds}–V_{ds} curves for gate voltages with V_{gs} = 9 V to 0 in −3 V steps from *top* to *bottom*. The *inset* is the SEM image of the as-fabricated single SnO_2 nanowire

$$\mu_e = g_m L^2 / C V_{DS} \quad (4)$$

$$g_m = \frac{dI_{DS}}{dV_g} \quad (5)$$

$$C = 2\pi\varepsilon_0\varepsilon \frac{L}{In(2h/r)} \quad (6)$$

where g_m is the transconductance, C is the capacitance and L is the channel length, ε, h, and r are the dielectric constant, the thickness, and the radius of silicon dioxide, respectively. Using $\varepsilon = 3.9$, $h = 500$ nm, $L = 1.5$ μm, and $r = 15$ nm, it can be calculated $\mu_e = 169$ cm/V s at $V_{DS} = 0.3$ V.

This value is consistent with those obtained in planar single-crystalline SnO_2 nanowire and other metal oxide nanowires. The performance of SnO_2-FET devices depends to a large extent on the source and drain contacts. In our cases, we find that it is effective to improve the quality of Au–SnO_2 contacts by annealing the SnO_2-FET devices in Ar at 973 K for 5 min. Therefore, the value of effective mobility, transconductance, and on/off ratio has also been significantly improved.

Conclusions

We present a simple, fast, and a low-cost method to synthesize SnO_2 nanowire arrays by using fast heating furnace. A ball-milled mixture of SnO_2 and CNTs waste soot was used as source materials. SEM and TEM images show nanowire diameters of 50–100 nm and lengths up to tens of mircrometers. The electrical properties of the as-synthesized single SnO_2 nanowire in FETs devices show that the n-type SnO_2 nanowires have larger on/off ratio (>10^5) and higher carrier mobility at room temperature. This method provides a promising candidate for large-scale preparation of SnO_2 nanostructures.

Acknowledgments We acknowledge that this work is supported by National Natural Science Foundation of China (No. 50730008), Shanghai Science and Technology Grant (No. 0752nm015), and National Basic Research Program of China (No. 2006CB300406).

References

1. F.L. Wang, L.Y. Wang, Y.F. Zhang, Nano. Res. Lett. **4**, 153 (2009)
2. Y. Zhang, K. Suenaga, C. Colliex, S. Lijima, Science **281**, 973 (1998)
3. H.V. Fajardo, E. Longo, L.F.D. Probst et al., Nano. Res. Lett. **3**, 194 (2008)
4. M.Y. Cheng, B.J. Hwang, Nano. Res. Lett. **2**, 28 (2007)
5. J. Mu, L. Liu, S.Z. Kang, Nano. Res. Lett. **2**, 100 (2007)
6. Y. Zhang, T. Ichihashi, E. Landree, F. Nihey, S. Lijima, Science **285**, 1719 (1999)
7. X. Peng, L. Manna, W. Yang, J. Wickham, E. Scher, A. Kadavanich, A.P. Alivisatos, Nature **404**, 59 (2000)
8. X.F. Duan, Y. Huang, Y. Cui, J.F. Wang, C.M. Lieber, Nature **409**, 66 (2001)
9. H.Y. Peng, Z.W. Pan, L. Xu, X.H. Fan, N.B. Wang, C.S. Lee, S.T. Lee, Adv. Mater. **13**, 317 (2001)
10. C.B. Murray, C.R. Cagan, M.G. Bawendi, Science **270**, 1335 (1995)
11. E.R. Leite, I.T. Weber, E. Longo, J.A. Varela, Adv. Mater. **12**, 965 (2000)
12. H.W. Ch Postma, T. Teepen, Z. Yao, M. Grifoni, C. Deckker, Science **293**, 76 (2001)
13. Z.W. Chen, J.K.L. Lai, C.H. Shek, Phys. Rev. B **70**, 165314 (2004)
14. C. Li, D.H. Zhang, S. Han, X.L. Liu, T. Tang, C.W. Zhou, Adv. Mater. **15**, 143 (2003)
15. Y. Idota, T. Kubota, A. Matsufuji, Y. Maekawa, T. Miyasaka, Science **276**, 1395 (1997)
16. Q. Dong, H. Su, D. Zhang, N. Zhu, X.Q. Guo, Acta. Mater. **13**, 3146 (2008)
17. Z. Pan, Z. Dai, Z.L. Wang, Science **291**, 1947 (2001)
18. Z.Q. Liu, D.H. Zhang, S. Han, C. Li, T. Tang, W. Jin, X.L. Liu, B. Lei, C.W. Zhou, Adv. Mater. **15**, 1754 (2003)
19. D.F. Zhang, L.D. Sun, J.L. Yin, C.H. Yan, Adv. Mater. **15**, 1022 (2003)
20. Z.R. Dai, Z.W. Pan, Z.L. Wang, Solid State Commun. **118**, 351 (2001)
21. M.H. Huang, Y. Wu, H. Feick, N. Tran, E. Weber, P. Yang, Adv. Mater. **13**, 113 (2001)
22. E.R. Leite, J.W. Gomes, M.M. Oliveira, E.J.H. Lee, E. Longo, J.A. Varela, C.A. Paskocimas, T.M. Boschi, F. Lanciotti Jr., P.S. Pizani, P.C. Soares Jr., Appl. Sci. Res. **2**, 125 (2002)
23. Z.R. Dai, J.L. Gole, J.D. Stout, Z.L.Wang, J. Phys. Chem. B **106**, 1274 (2002)
24. M. Law, H. Kind, B. Messer, F. Kim, P. Yang, Angew. Chem. **114**, 2511 (2002)
25. H.I. Liu, N.I. Maluf, R.F.W. Pease, J. Vac. Sci. Technol. B **10**, 2846 (1992)
26. T. Ono, H. Saitoh, M. Esashi, Appl. Phys. Lett. **70**, 1852 (1997)
27. F.C. Frank, Discov. Faraday **5**, 48 (1949)
28. R.S. Wagner, W.C. Ellis, Appl. Phys. Lett. **4**, 89 (1964)
29. Z.W. Chen, J.K.L. Lai, C.H. Shek, H.D. Chen, J. Mater. Res. **18**, 1289 (2003)
30. Y. Cheng, P. Xiong, L. Fields, J.P. Zheng, R.S. Yang, Z.L. Wang, Appl. Phys. Lett. **89**, 093114 (2006)
31. M.G. McDowell, R.J. Sanderson, I.G. Hill, Appl. Phys. Lett. **92**, 013502 (2008)
32. L. Luo, B.D. Sosnowchik, L.W. Lin, Appl. Phys. Lett. **90**, 093101 (2007)
33. Y.J. Chen, Q.H. Li, Y.X. Liang, T.H. Wang, Q. Zhao, D.P. Yu, Appl. Phys. Lett. **85**, 5682 (2006)
34. Q.Y. Wang, K. Yu, F. Xu, Solid State Commun. **143**, 260 (2007)
35. W.M. Zhou, F. Fang, Z.Y. Hou, L.J. Yan, Y.F. Zhang, IEEE Electron Device Lett. **27**, 463 (2006)