



Low-Resistance Room-Temperature Interconnection Technique for Bonding Fine Pitch Bumps

F. Roustaie, S. Quednau, F. Weißenborn, and O. Birlem

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In this work, we demonstrate on a new interconnection technology which can be used for bonding Flip-Chips with 5- μm -Bumps and fine pitches $< 5 \mu\text{m}$. In this technology, the bumps on both joint partners are coated with metallic nanowires (in most cases copper, in rare cases gold), through an in situ electrochemical deposition process, the so-called NanoWiring process. The diameter of the wires can be adjusted between 30 and 4000 nm, and their length is ranged from 4 to 50 μm . The process is scaled up for 12 inch wafers. The bonding process can be performed directly at wafer level or also at Flip-Chip level. The nanowires overcome the dicing step. The diced chips can be bonded by adjusting and pressing the NanoWired bumps together at room temperature, using the standard bonding devices. The required bonding forces range from 5 to 50 MPa for flip chips, LEDs and sensors. The bonding with nanowires, the so-called KlettWelding, can be explained by diffusion of the nanowires in each other under compression and weaving of the wires as well. The measured shear strength of these connections yields 15-24 MPa. The very large achieved Surface/Volume quotient of NanoWired surface causes this strength. For a better performance, a prior copper oxide reducing step for the copper NanoWires is needed. This can be done by using standard processes like forming gas plasma or formic acid vapor. By heating during the pressing process up to 230 °C, the shear strength increases to 60 MPa. The nanowired interconnections have an electrical conduction in the range of bulk metal, because of their pure metallic nature. Beside microelectronic applications, the bonding of larger metallic plates like aluminium, copper, steel and also flexible polymers, glass, silicon and ceramics are also enabled.

Keywords electronic materials, electronics, joining, nanomaterials, semiconductors

1. Introduction

With further improvements in the integrated circuits and the increment in the density of electronic packages in mobile devices, the improvements in interconnection technology are essential (Ref 1). The rapidly emerging technologies have vanished the boundaries between the semiconductors, packaging and systems (Ref 2). One major obstacle in the development of new compatible interconnections to the high dense systems and the 3D components packaging is the high temperatures for the newly innovated bonding methods. Other than that, the new techniques consist of multiple layers with toxic alloys. Recycling of such electronic devices is an environmental challenge today. The heat-free or low-temperature processes are also limited in their application and performance. The KlettWelding solution, introduced in this

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F. Roustaie, S. Quednau, F. Weißenborn, and O. Birlem, NanoWired GmbH, Emanuel-Merck-Str. 99, 64579 Gernsheim, Germany. Contact e-mail: Farough.roustaie@nanowired.de.

paper, is a high-performance interconnection technology with electrical resistance in the range of bulk copper material. The thermal resistance of the connections is near zero. This technology enables bonding ultrahigh dense pads with 3- μm -edge length and 5- μm -pitches at wafer level chip scale packaging (WL-CSP) or Fan-out packaging on panel level (FOPLP) or flip-chip level. This technology is a room temperature or low-temperature technology. Thus, the mismatch of the thermal expansions between the BGA and substrates by rapid temperature changes (Ref 3) vanishes.

2. The NanoWiring and KlettWelding Process

The basic of the NanoWiring process is a standard electrochemical deposition for microstructures. For this process, an electrically conductive seed layer is needed. For non-metallic substrates like glass, silicon, polymers or ceramics, this layer in combination with an adhesion layer is sputtered, or laminated on the surface. The connection pads or bumps are defined in a lithographical step. This process is described in detail in (Ref 4). The pad sizes are limited to the exposure limit of the mask aligner. NanoWiring process can be performed on pads down to 3 μm . At the next step, the pads are covered with a porous template membrane. The metal deposition takes place in the pores of the template. To fix the template on the pads, the deposition takes place in a specially developed NanoWiring machine. As the last step, the template membrane is removed in a wet chemical stripping step or a standard plasma ashing process. The sputtered seed layer at unwanted areas can be removed in a short-time etching step, and the nanowires overcome this step. The NanoWiring steps are illustrated in

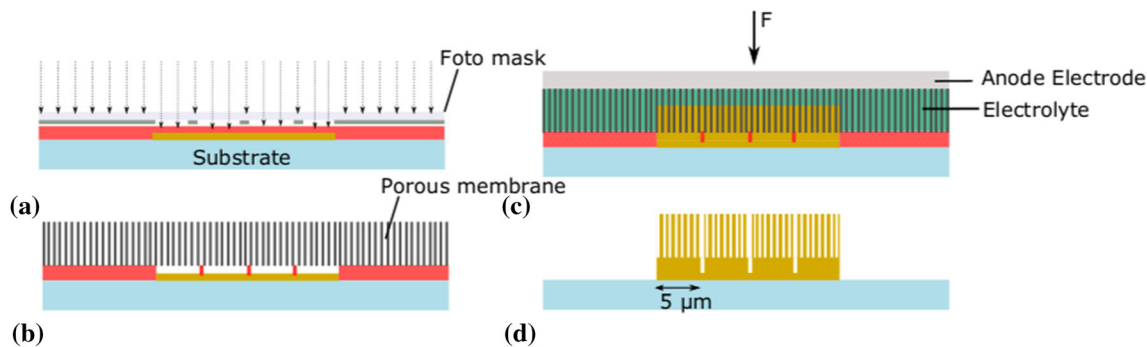


Fig. 1 (a) The substrate is passive with a 1 to 2 μm thin layer of positive photo resist. The pads or bumps are defined in a lithographical step. (b) A porous membrane is fixed on the top of the pads. (c) The nanowires grow in an electrochemical deposition process while the porous membrane is fixed by the applied force on the anode electrode, and (d) the porous membrane is removed in a wet chemical stripping step

Fig. 1. In this process, the porous template geometry defines the density, thickness and length of the nanowires. The wires diameter ranges between 30 and 4000 nm, and their length can be adjusted between 4 and 50 μm , and the standard deviation in the wire length is less than 10% of the maximum wire length. The fill factor of the surface with wires ranges between 10 and 40% depending on the wire's diameter. The maximum allowed local surface roughness for the NanoWiring seed layer is 20% of the maximum wire length or $\pm 10 \mu\text{m}$ for 50 μm long wires. Nevertheless, the KlettWelding process works on mesa structures and bumps with a height or depth even larger than 50% of the maximum wire length. The synthesis of the wires takes place in a standalone NanoWiring machine with automatically controlled parameters. The process is scaled up to 12-inch wafers or $300 \times 400 \text{ mm}^2$ panels. Active NanoWiring surface ranges between $9 \mu\text{m}^2$ and 1200 cm^2 . In this machine, NanoWiring with different metals like copper, gold, silver, nickel, and platinum is possible. The copper deposition can be done at temperatures below 35 $^\circ\text{C}$, and in cases like gold or platinum a temperature of about 65 $^\circ\text{C}$ is needed. The NanoWiring process on flat and curved surfaces is described in detail in (Ref 4-8). In Fig. 2, different surfaces covered with NanoWires are shown. The bonding process of the pads or bumps can be done just by pressing two surfaces with NanoWiring together at room temperature, so-called KlettWelding. This can be done either at wafer or panel level or flip-chip level, needing no inert gas or underfill. The physical explanation behind the KlettWelding process is the simultaneous entanglement of the wires in each other and the diffusion of the NanoWires into each other by the migration of the atoms from the crystal lattice of one wire to the other one. The connection achieves 70% of the maximum mechanical strength in $< 60 \text{ ms}$, and in 12 h, it reaches its maximum strength. By applying additional thermal energy, the motion process increases. Thus, the maximum strength reaches in 10-120 s, depending on the surface geometry and substrate material. For a better diffusion, a prior copper oxide reducing step for the copper Nanowires is needed. This can be done by using standard processes like forming-gas plasma or formic acid vapor (Ref 9).

For different applications or different types of material, the bonding process can be performed in different NanoWiring combinations (Ref 9). For example, covering just one of the samples with the NanoWires and pressing them at a temperature between 170 and 270 $^\circ\text{C}$, the so-called KlettSintering or combining the nanowires with a proper glue, the so-called

KlettGlueing. These different techniques, their properties and achieved shear strength are listed in Table 1 (Ref 9). KlettWelding-Tape is a copper foil, covered with NanoWires on both sides. This tape is shown in Fig. 3. It enables bonding two surfaces without NanoWiring, the so-called KlettSintering+. In this method, the KlettWelding-Tape is sandwiched between two surfaces, and they are bonded at a temperature of about 170 and 270 $^\circ\text{C}$ and bonding pressures of about 10 MPa for chips to 60 MPa for laser cut bus-bars with a burr along the bar. The achieved shear strength is about 15-115 MPa for different techniques. The cross-section images of such contacts are shown in Fig. 3.

3. Electrical Resistance of NanoWired Interconnections

The NanoWired interconnections are pure metallic connections from copper, gold or silver. Thus, the electrical resistance of these joints is in the range of bulk metal. For measuring the electrical resistance and mechanical shear strength of the connections, a connection between 2 metallic copper bars with 6 mm and 4-mm-width and 2-mm-thickness is considered (see Fig. 4). The interconnections have an area of $4 \times 5 \text{ mm}^2$. The samples have NanoWiring with a nanowire diameter of 1 μm and a mean length of 45 μm on the surface. For each experiment in a time interval, 8 connections are considered. The electrical resistance of all the connections is measured with a HIOKI RM3545 resistance meter in a 4-terminal measurement setup using a Z3003 multiplex unit at controlled ambient conditions of 21 $^\circ\text{C}$ and 55%Rh. Each connection is measured 10 times at 1A current flow, and the result for each connection is calculated as the mean value of the measurements. The result of this measurement on all samples for each bonding method is shown as a box-diagram in Fig. 5. As it can be seen the results are in the range of a bulk oxygen-free copper (Cu-OF) specimen with the same dimensions and measured in the same device.

At the next step the aging of the connections is conducted as per (Ref 10). In this test, the gap corrosion of the contacts under humidity and thermal stress of 85%Rh and 85 $^\circ\text{C}$ for 500 and 1000 h is tested. At each step, the electrical conductivity of the samples is measured. The tests run in a WK 111-600 climates simulation chambers of the company Weiss Technik. The results for the KlettWelding+, KlettSintering and KlettSinter-

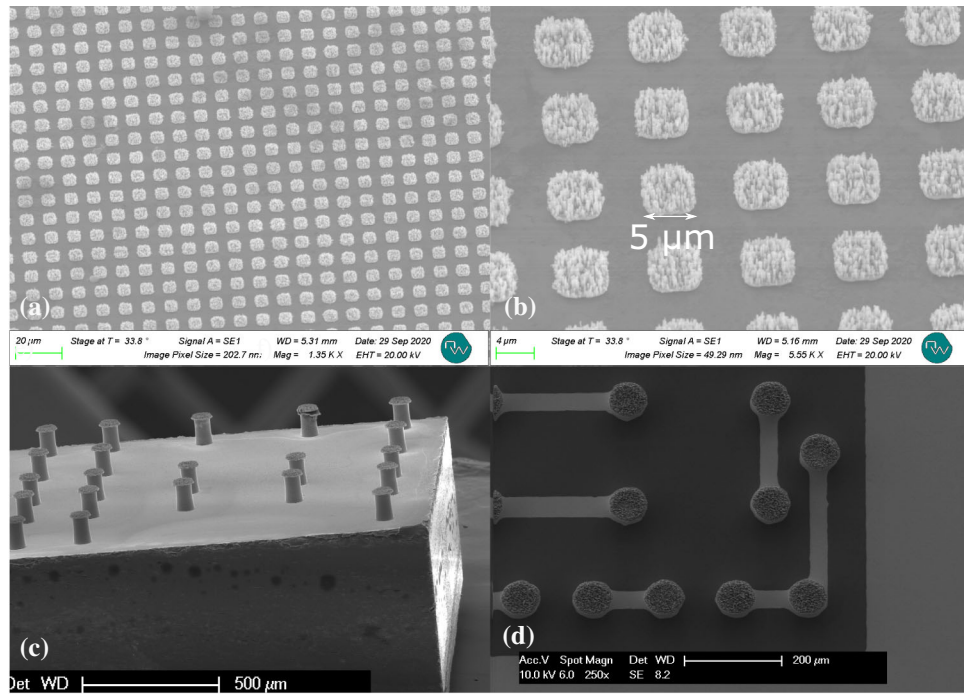


Fig. 2 (a) and (b) SEM images of micro pads with 5- μm -edge length and 5- μm -pitch on a 8-inch wafer. The wires have 200-nm-diameter and 4- μm -length that means an aspect ratio of 20. (c) and (d) Micro bumps with 60- μm -diameter on a chip covered selectively with NanoWires. The NanoWires overcome the dicing process

Table 1. Properties of different methods for bonding with NanoWired surfaces

Method	Bonding pressure, MPa	Bonding temperature, °C	NanoWiring	Shear strength, MPa
KlettWelding	15–60	21	Both sides	18
KlettSintering	10–60	170–270	One side	37
KlettGlueing	1–10	140	One side	15
KlettWelding+	15–150	170–270	Both sides	40–115
KlettSintering+	10–60	170–270	–	40

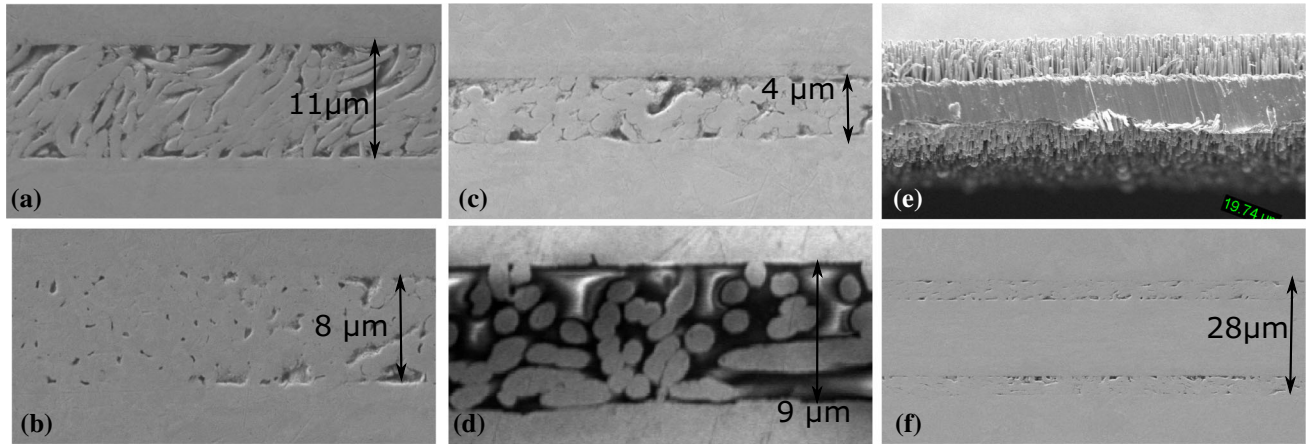


Fig. 3 Cross-section images of the NanoWired contacts (a) KlettWelding at room temperature with bond line of 11 μm , (b) KlettWelding+ at 230 $^{\circ}\text{C}$ and 50 MPa with 8 μm bond-line, (c) KlettSintering with one sided NanoWiring and 230 $^{\circ}\text{C}$ with bond line of 4 μm , (d) KlettGlueing at 140 $^{\circ}\text{C}$ and 10 MPa bonding pressure with a bond line of 9 μm , (e) Cross section of KlettWelding-Tape with 1 $\mu\text{m}/25 \mu\text{m}$ copper nanowires at both sides and (f) KlettSintering+ with KlettWelding Tape with a bond line of 28 μm including the Tape thickness of 20 μm

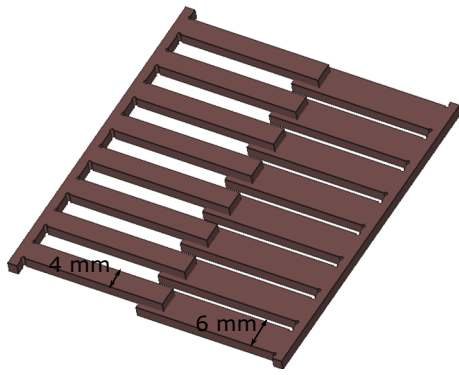


Fig. 4 Copper bar specimen for resistance and shear strength measurement. To perform the measurement, the supporting frame is cut

ing+ samples are shown in Fig. 6. For all three methods, the measured electrical resistances are still in the range of the accuracy of the measurement system, and no significant changes are observed. The samples are tested for the changes in their shear strength, and no changes were obvious as well after 1000 h. The images of the contact areas are demonstrated in Fig. 7. As can be seen, no corrosion is optically detected on the contact surface, while the nanowires in the neighbor area are oxidized. Also, an EDX measurement detects no copper oxide or copper hydroxide in the contact area (see Fig. 7). Some color changes detected on the surface are the backlog of sintered copper nanowires on the surface.

Also performed thermal shock tests (1000 cycles of the $-40\text{ }^{\circ}\text{C}/150\text{ }^{\circ}\text{C}$) did not show a significant drop in electrical conductance or mechanical shear strength.

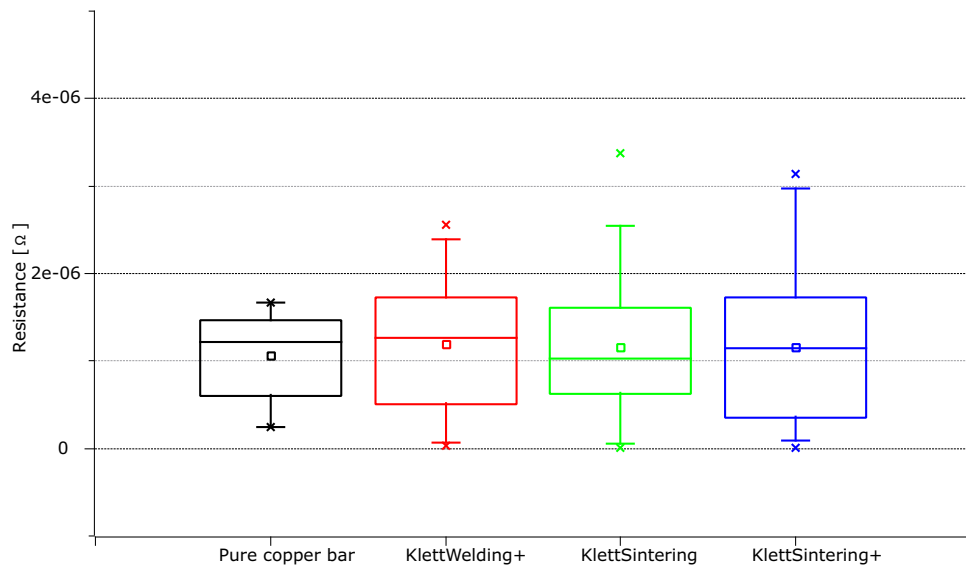


Fig. 5 Measured electrical resistance of interconnection with three bonding methods. All three methods show a mean value about in the range of system accuracy and near the measured pure bulk copper resistance

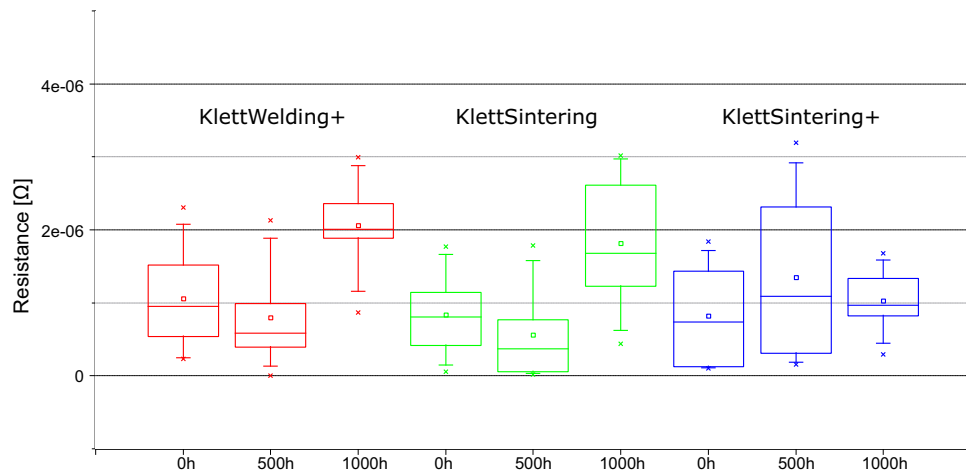


Fig. 6 Aging the interconnections at $85\text{ }^{\circ}\text{C}$ and $85\%\text{Rh}$ for 500 h and 1000 h. The resistance measurements show no increase after 1000 h aging

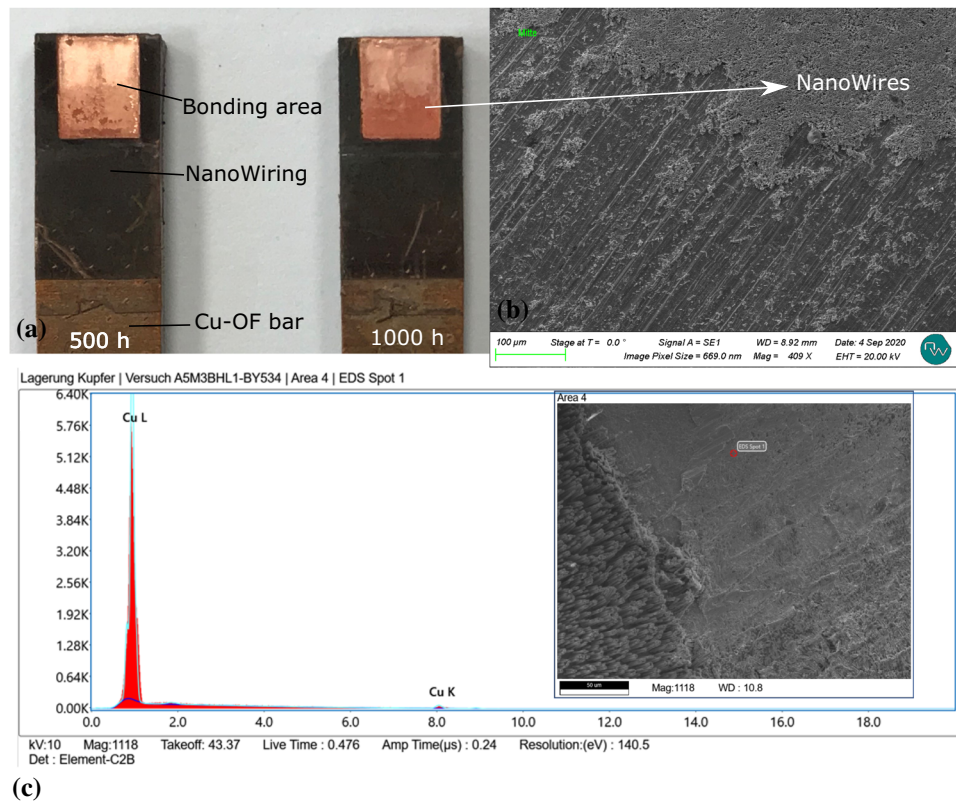


Fig. 7 (a) Contact areas after 500 h and 1000 h show no optical sign of corrosion like the neighbor NanoWiring areas. (b) The color changes under SEM show the NanoWiring residues on the surface, and (c) an EDX measurement did not detect any oxygen in the contact area

4. Conclusion and Outlook

The result achieved in this experiment agrees with a previously performed helium gas sealing test that shows a leakage rate of 9.5×10^{-9} mbar \times l/s for KlettSintering connections and 1.0×10^{-8} mbar \times l/s for KlettWelding+ structures. With the method introduced in this paper, the NanoWiring of almost all kinds of substrates like Polymers, Silicon, Glass, Ceramics, Aluminum, Steel, Copper is possible. It is also possible to bond different material combinations like Aluminum-Ceramics or Glass-Metal bonding without any thermal stress in the joints and an electrical conductance near zero. The first tests show a contact thermal conductivity of about 350 W/mK. An investigation on higher number of samples is ongoing on.

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