



Microcracking in On-Chip Interconnect Stacks: FEM Simulation and Concept for Fatigue Test

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Abstract

The semiconductor industry is continuing the scaling down of both device and on-chip interconnect features, for performance and economic reasons. This trend has implications for the design of guard ring structures, i.e. metallic non-functional structures in the back-end-of-line (BEoL) stack designed to be efficient to stop microcracks. In this work, we present a sample design for an in situ experiment to study mechanical degradation and failure mechanisms of crack stop structures in the BEoL stack, to ensure the mechanical robustness of microchips for future technology nodes. Additional finite element method (FEM) simulations provide supplementary understanding of the crack kinetics. To examine the effects of mechanical loading on crack stop elements of the BEoL stack, a novel sample geometry for an in situ fatigue experiment using x-ray microscopy was developed. The x-ray microscope (ZEISS Xradia 800 Ultra) enables high-resolution imaging of the 3D-patterned sample structures and defects such as microcracks. The tailored sample geometry allows the application of a tensile load to a BEoL specimen by a lever mechanism. The feasibility of the sample design is shown by mode-I loading of a pure interconnect sample. Post-mortem analysis by scanning electron microscopy (SEM), confirming planar microcrack propagation from the notch through the dielectric layer with small deflections of the crack path near cone shaped copper vias. FEM simulations focusing on the stress-strain fields around a crack tip indicate the beginning of copper plasticity as major mechanism starting the redirection of cracks due to resulting material compression in front of the obstacle.

Keywords Microelectronics · micromechanical test · fracture mechanics · x-ray microscopy · high-resolution 3D imaging

Introduction

The semiconductor industry is continuing the downsizing of copper (Cu) and organosilicate glass (low-k material) on-chip interconnect stack dimensions, while the reliability demands of microelectronic products for critical applications are significantly increasing. Mechanical robustness of microchips, mainly caused by low Young's modulus and fracture toughness of dense and porous low-k material, is a serious reliability concern.¹ Microcracks initiated at the rim of the die during the wafer dicing process are risks for failure when

propagating into the back-end-of-line (BEoL) stack of the die. Manufacturers try to mitigate this risk by implementing a specially designed metallic non-functional structure, known as a guard ring, with the goal to stop microcrack propagation.² In addition, residual stress introduced during fabrication and thermal expansion coefficient mismatches between involved materials are additional driving forces for crack propagation.

To ensure the requested robustness of microchips, it is essential for semiconductor companies to design efficient guard ring structures. To assess the influence of the guard ring design on the microcrack propagation in the Cu/low-k stacks, it is essential to study this protective structure under controlled loading conditions. Existing 2D tests, including four-point bending³ and modified cross-sectional nanoindentation (MSCN)⁴ studies, provide valuable insights into the location of microcrack paths but lack the visualization of intermediate cracking states and 3D microcrack evolution. The latest reported in situ micro double-cantilever

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beam (μ DCB) test allows continuous 3D imaging of crack propagation; it relies on the stepwise opening of an existing microcrack at several mixed fracture mode loading conditions.⁵ Pure mode-I (tensile opening) loading generally governs crack initiation and propagation and hence is mandatory during testing in order to gain an understanding of the crack mechanisms. Moreover, cyclic thermomechanical loads are an essential root cause for the growth of microcracks, which have to be realized for mimicking lifelike loading scenarios. Therefore, both pure mode-I loading as well as fatigue loading must be realized to gain further understanding of the crack steering mechanisms of protective structures.

In this study, a test specimen design for fatigue testing of on-chip Cu/low-k interconnect stack structures was developed that allows a pure mode-I loading experiment. Its design is tailored towards in situ x-ray microscopy

experiments enabling microcrack initiation and propagation inside the BEoL with simultaneous high-resolution visualization of the cracking states in 3D throughout the entire experiment. The applicability of the new sample design to induce cracking into a specimen that includes the BEoL of a microchip to test guard ring structures is shown in this paper by pure tensile loading. In the future, fatigue tests of on-chip Cu/low-k interconnect stack structures can be carried out by cyclically loading of the test geometry. This sample design allows us to study mode-I and fatigue fracture mechanics of on-chip interconnect structures, and to evaluate the performance of guard ring structures. An existing micromechanical test rig (MMR-tester, Fig. 1⁶) is used for actuation of the sample generating a tensile load in a specific region of the on-chip interconnect structure; see Fig. 2. In order to discuss crack deflection mechanisms, the experimentally observed cracking behavior was analyzed applying finite element modeling (FEM) with a specific focus on the influence of copper plasticity on the acting stress close to the crack tip.

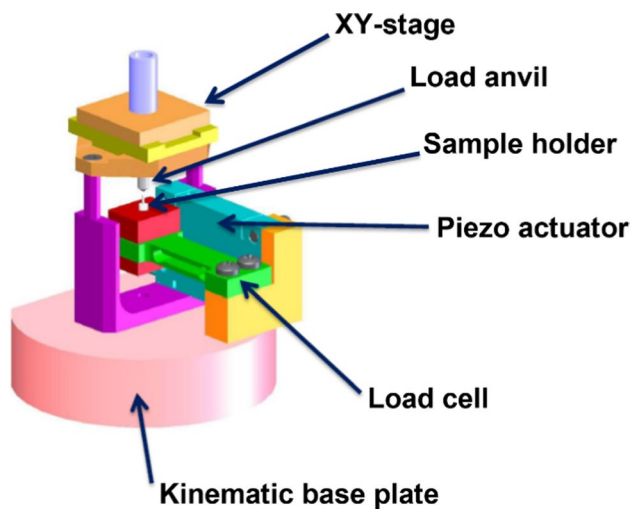


Fig. 1 MMR-tester design for in situ testing using x-ray microscopy. Figure adapted and modified with permission from Ref. 6.

Methodology

The fracture behavior of on-chip interconnect stack structures can be studied by integrating a micromechanical test setup into an x-ray microscope, a unique nondestructive high-resolution imaging technique for the in situ visualization of BEoL structures with sub-100-nm resolution. This technique allows the gradual imaging of crack propagation in 3D nanostructures. The acquired 3D data provide information about the crack path, as well as local values such as critical energy release rate for crack propagation.⁷

Visualizing opaque materials is usually unfeasible using light and electron microscopy due to the insufficient penetration depth of photons and electrons into the materials. However, x-ray microscopy allows high sample penetration

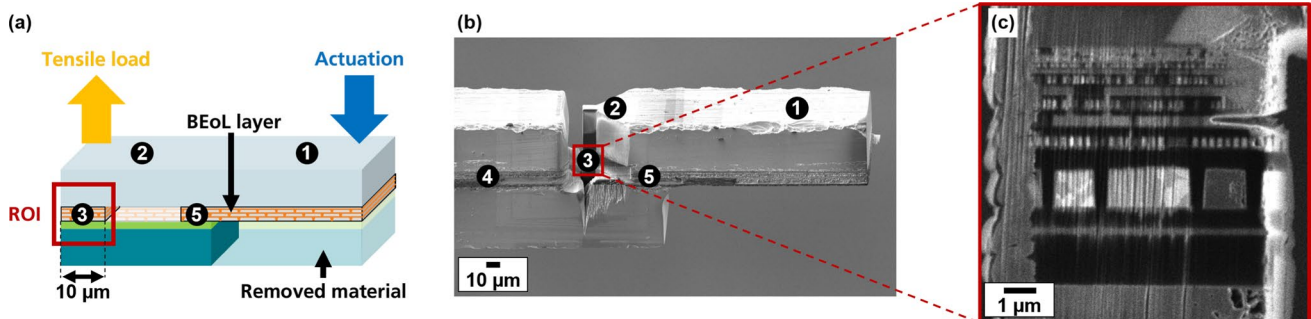


Fig. 2 (a) Schematic representation of the sample blank with faintly marked FIB trenches and its working principle. The outermost layers are silicon, which enclose the structured body, the BEoL, and the adhesive layer. The scale of the ROI is indicated, the remaining dimensions are not to scale. (b) SEM image of the final sample design

after FIB preparation. (c) Magnified SEM image of the ROI illustrating the copper structures (bright), the dielectrics (dark), the redeposition (left hand side), the notch (right hand side), the adhesive (bottom), and silicon (top).

in combination with high spatial resolution by utilizing higher-energy photons. Thus, an x-ray microscope (ZEISS Xradia 800 Ultra, Cu-K α radiation) was used for in situ imaging of the 3D nanostructure. The photon energy of 8.05 keV requires the preparation of samples with a thickness of < 100 μm to ensure sufficient x-ray transmission and to enable the visualization of the 3D Cu/low-k interconnect stack with sufficient contrast. During tomography, 801 images were acquired for an angular range of 180°. The field of view was 65 μm \times 65 μm .

For micromechanical testing, a customized test rig (MMR-tester) was utilized (Fig. 1). The MMR-tester is equipped with a piezo actuator enabling stepwise motion of the sample holder in the vertical direction. A Berkovich indenter tip is mounted above the sample holder in a load anvil to operate the loading. Horizontal alignment of the indenter and sample is obtained on an XY-linear stage to align the indenter relative to the sample. Vertical positioning is received by vertically positioning of the load anvil. A load cell connected between the actuator and sample holder allows us to measure the applied load during actuation.

Sample Selection and Preparation

On-chip interconnect stacks are composed of multiple materials with size-dependent material properties. The three major materials are silicon (Si), Cu, and dielectrics (silicon dioxide (SiO₂) or low-k material). Dense and porous organosilicate glass has a reduced dielectric permittivity (k value) compared to SiO₂; however, it also has a significantly reduced Young's modulus, and consequently lower fracture toughness.⁸ This means that the resistance to microcrack propagation is reduced, which results in a higher risk of failure.

The growth of microcracks initiated during the wafer dicing process at the rim of the microchip is a significant reliability concern. During microchip manufacturing and in operation, cyclic thermomechanical loads occur, which drive existing cracks to further propagate and thus accelerate failure mechanisms. The understanding of pure fracture mode-I loading is a first step towards understanding the fatigue failure behavior of a microchip, and in particular its BEoL stack.

For designing a special sample design for mode-I loading of BEoL structures, the following facts must be considered:

- Cracking is supposed to originate and propagate in the BEoL structure.
- Failures at other regions of the sample must not occur; in particular, total failure caused by fracture must be excluded.
- Stable specimen construction is required with space for solid mounting of the sample.

- Pure mode-I load is applied on the BEoL structure to assess resistance to tensile load fracture.
- The sample dimensions must ensure good contrast during x-ray imaging using Cu-K α radiation.

Considering these requirements, sample blanks are produced from a microchip with a BEoL consisting of 12 metalization layers, as described by Kutukova.⁹ The microchip and a piece of plain Si are bonded together by an adhesive (EPO-TEK® 353ND) in such a way that the BEoL layer stack is embedded by two Si layers. The maximum sample thickness for imaging using a photon energy of 8.05 keV is about 70 μm , calculated considering the attenuation lengths (l_{att}) of the materials [Si ($l_{\text{att}} = 71 \mu\text{m}^{10}$), SiO₂ ($l_{\text{att}} = 130 \mu\text{m}^{10}$), epoxy ($l_{\text{att}} = 1287 \mu\text{m}^{11}$), and Cu ($l_{\text{att}} = 22 \mu\text{m}^{10}$)]. A sample cross section of 50 $\mu\text{m}^2 \times 70 \mu\text{m}^2$ was selected to ensure that the whole BEoL stack fit into the field of view of the microscope. A total sample length of 1500 μm was chosen, with a length of 500 μm for the implementation of a mechanical sample structure and 1000 μm to facilitate mounting of the sample to the sample holder.

A customized lever design was developed (see scheme in Fig. 2a), with the goal to generate a mode-I load on the BEoL as a counteracting force caused by the stepwise actuation of a freestanding lever. The sample consists of a freestanding lever (⊙) which is actuated by a microindenter. Deflecting the freestanding lever, a second lever (⊗) on the opposing end of the sample is pulled upwards. Since the second lever is attached to the base structure, tensile load concentrates in the connecting piece where the BEoL is located, from now on this region is referred to as the region of interest (ROI) (⊚). A notch (2 $\mu\text{m}^2 \times 0.3 \mu\text{m}^2$) is applied in the layered BEoL structure of the ROI serving as crack initiator during tensile loading of the structure. Note that the sample structure of Fig. 2a represents only the end of the 1500- μm -long sample blank. A vertical notch is separating the second lever from the remaining unprocessed section of the sample (⊘), as seen in Fig. 2b. The unprocessed section is used for mounting the sample with an adhesive to a sample holder for sample handling.

For sample preparation according to the geometry described above, some material is milled away by focused ion beam (FIB) milling (Thermo Fisher, Helios 5 PFIB Cxe). The 150- μm -long freestanding lever is obtained by milling away the material underneath the BEoL stack at the very end of the sample blank. On the adjacent unmodified side of the stack, a 20- μm -long via structure (⊙) is retained for load transmission during actuation while maintaining the stability of the overall sample. For load concentrations at the end of the second lever where the ROI is located, a trench of 10 $\mu\text{m}^2 \times 25 \mu\text{m}^2$ is milled in the BEoL layer; for the removed material see Fig. 2a. The 10- μm -wide unprocessed part of the BEoL at the end of the second lever represents the ROI

where the counteracting tensile load is concentrated during actuation of the freestanding lever. The second lever is separated from the remaining part of the sample blank by an adjacent $15\ \mu\text{m}^2 \times 40\ \mu\text{m}^2$ notch. To reduce the risk of breakage at the sharp edges introduced by the FIB, the edges at the separating notch as well as at the edge at the first lever are not completely milled but rounded. To further increase the tensile load in the connecting piece with the BEoL structure, the second notch is tapered towards the end. The width of the lever shrinks gradually from $50\ \mu\text{m}$ to $10\ \mu\text{m}$ at the target structure; see the scanning electron microscopy (SEM) image in Fig. 2b. For maintaining stability of the overall sample structure, the tapering is introduced only in the top structure including the original microchip and the epoxy layer, at the bottom the plain silicon layer remains. Since it was not possible to generate a plane step at the desired depth due to FIB milling of an inhomogeneous material, “canyons” of different depth are visible on the prepared specimen; see Fig. 2b. The nature of the milling process causes removed material that is partly redeposited elsewhere. This layer of redeposition is visible at the outer face of the ROI; see Fig. 2c. Thus, the ROI consists of the BEoL stack and a layer of redeposited material which could influence the fracture behavior of the BEoL and may give misleading results of the kinetic cracking process.

Cantilever Push Tensile Test Experiment

During the micromechanical test, radiographs are taken to track the 2D microcrack initiation and propagation in the ROI, where microcracks can be detected from a dimension of about $100\ \text{nm}$. In addition to visual crack detection, abrupt drops of the loading curve during the gradual actuation process also indicate the formation of cracks in the structure. Figure 3a shows the ROI before the experiment, and Fig. 3b the ROI after the first load drop from $23\ \text{mN}$

to $10\ \text{mN}$ (see Fig. 4), representing a total failure of the structure. The cracking initiated at the notch tip and propagated horizontally through the entire sample which led to total failure of the ROI. These pure mode-I results are proof that the design of the sample geometry can be applied for the study of microcrack propagation due to mode-I fatigue loading in the BEoL.

The post-mortem 3D visualization of the sample in Fig. 3c shows the two fragments of the fractured BEoL stack and the implemented notch for microcrack initiation on the lower fragment. The crack surfaces indicate a planar fracture of the interconnect stack starting at the notch tip and propagating between two metallization layers. The clear distinction of the notch in the 3D dataset confirms the ability of x-ray microscopy to visualize the microcrack path, including the geometry of the crack surfaces, and reveal deflections of the cracking path.

To gain further insights into the fracture mechanics, the broken interface is visualized by SEM giving 2D information of the cracks visible on surfaces. In this way, the external cracking path can be visualized in 2D at higher resolution, revealing crack progression in more detail while lacking information about internal fracture mechanisms and 3D information of the cracking path. Post-mortem SEM imaging of the experimental sample reveals that the crack

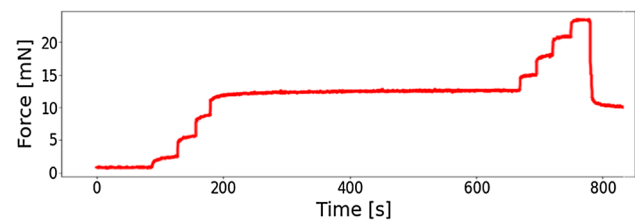


Fig. 4 Loading curve of the microindenter actuating the lever during tensile testing of the sample.

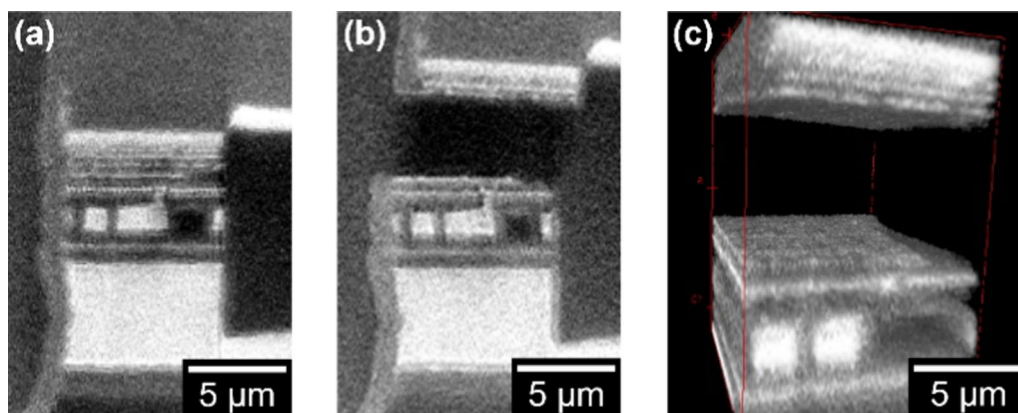


Fig. 3 2D cross-section of the ROI reconstructed after tomography (a) prior to and (b) after the stress test. (c) 3D reconstruction of the fractured ROI.

developed through the dielectric layer; see Fig. 5c. The crack path appears to be deflected by the trapezoidal copper vias before the crack comes into contact with the via. Therefore, the question arises which effects cause the deflection of the crack path.

Compared to other micromechanical experiments, the main advantage of the cantilever push tensile test is the creation of a pure mode-I loading scenario of BEoL structures while enabling the visualization of 3D microcrack evolution providing information about crack steering mechanisms and the fundamental mode-I fracture behavior. The future application of fatigue load also allows the investigation of the fracture behavior due to fatigue loading.

FEM Model

To understand the stress-strain field around the crack tip vicinity and, thus, further crack growth, when the crack is facing an obstacle, quasi-static FEM simulations are established using ANSYS. This can provide an understanding of

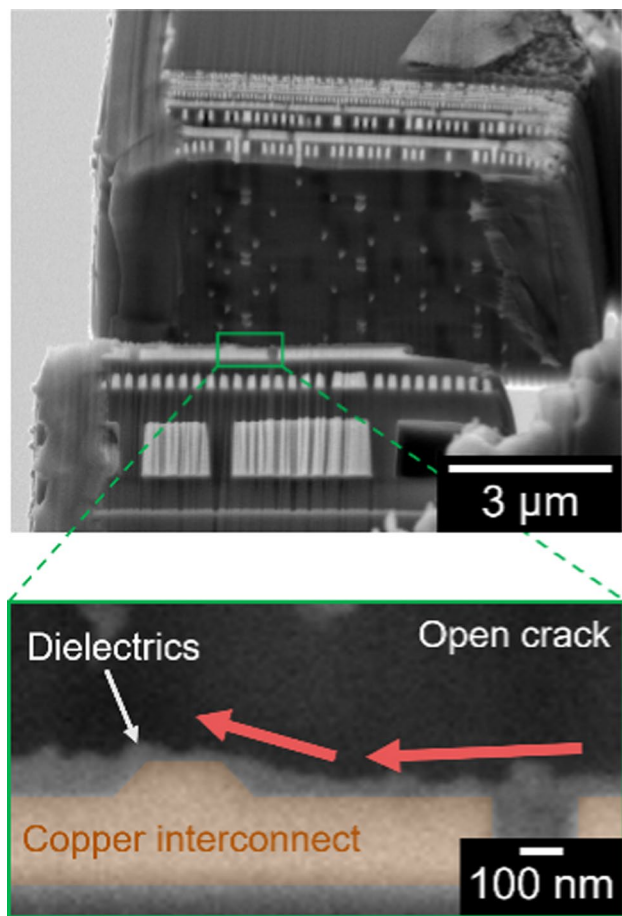


Fig. 5 SEM image of the fractured ROI of the specimen and a magnification of the cracked interface below, showing the deflection of the crack path near a copper interconnect structure.

the observed crack deflection at Cu vias, where the cracks are redirected before arriving at the vias and are steered to a region more prone to cracking of the interconnect stack. An initial simplified simulation is used to gain basic insight into the acting stress-strain fields around a crack tip when facing a rectangular Cu obstacle. Subsequently, a simulation tailored to the experimental sample model including the trapezoid-shaped copper via of the previous section is examined and compared to the experimental results.

For the simplified simulation, a rectangular base ($19 \mu\text{m}^3 \times 5 \mu\text{m}^3 \times 3 \mu\text{m}^3$) with the material parameters of the SiO_2 dielectric is modeled containing a Cu block ($2 \mu\text{m}^3 \times 3 \mu\text{m}^3 \times 3 \mu\text{m}^3$) which serves as an obstacle for crack propagation at a distance of $1 \mu\text{m}$ from a central crack ($7 \mu\text{m}^3 \times 0.1 \mu\text{m}^3 \times 3 \mu\text{m}^3$); see Fig. 6a. The stress-strain behaviors of the materials are simplified by using a bilinear isotropic hardening model including the implementation of Young's modulus (E), yield stress (σ_Y), and tangent modulus (E_T). The latter is defined as

$$E_T = \frac{\sigma_F - \sigma_Y}{\epsilon_F - \sigma_Y/E}. \quad (1)$$

The used material parameters of SiO_2 and polycrystalline copper are specified in Table 1. The goal is to examine the effects of the obstacle on an approaching crack during loading. To model the stress-strain fields around the crack tip which ultimately govern the further crack propagation towards the obstacle, a mechanical load is applied by pulling the upper lever gradually apart while the lower one remains fixed. The final displacement of $0.7 \mu\text{m}$ is divided into 40 equal load steps. The copper obstacle is observed to be plastically deformed from load step 7 onwards ($\epsilon > \sigma_Y/E$). After the plastic deformation of the copper has started, noticeable trends for the normal stresses in the Y -direction and the total equivalent stresses (von Mises) appear; see Fig. 6b and c. In the case of the Y -normal stress, an area of compression forms in front of the obstacle after plasticity develops; see Fig. 6b2. A crack principally follows the path of least resistance against crack propagation and the highest local crack opening stresses. Given a uniform material behavior, tension stress inside the material lowers the resistance against cracking at the respective region, so a crack would run through the region exposed to the greatest tensile stress. Accordingly, a propagating crack would avoid the region under compression and moves towards a region under tension. Thus, the observation of the compression area in front of the Cu obstacle suggests a crack deflection away from this obstacle. Moreover, the total equivalent stress shows a horizontal stress field bending away from the obstacle as the copper plasticity emerges; see Fig. 6c2. Therefore, the stress field indicates a crack path being deflected around the Cu obstacle. An equal simulation of the model with removed plasticity effects (Cu

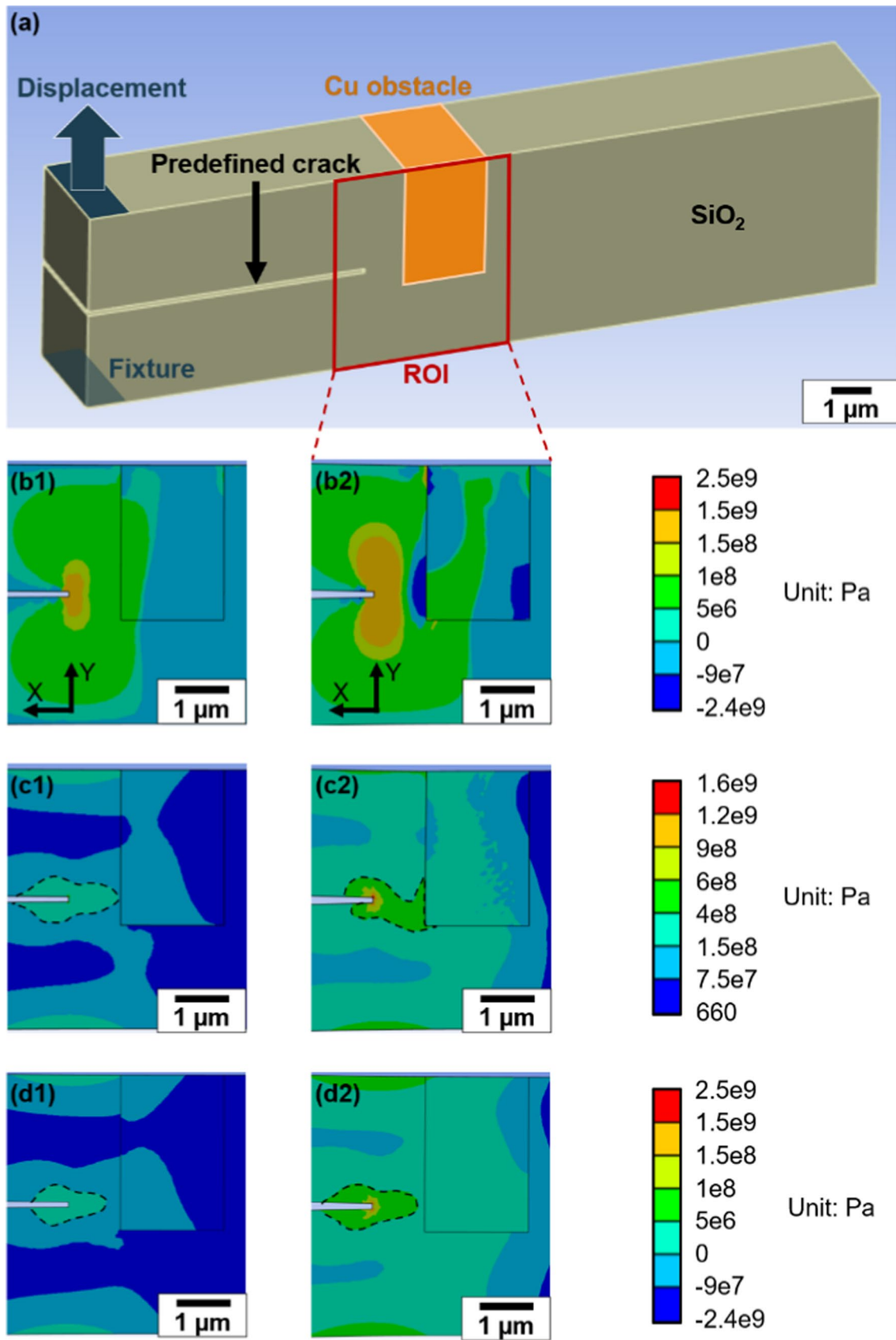


Fig. 6 (a) ANSYS model of a simplified cracking scenario inside SiO₂ where a crack propagates towards a Cu obstacle. (b) Results of the *Y*-normal stress field inside the geometry at (b1) load step 7 and (b2) load step 20. Outcome of the total equivalent stress (von Mises) field inside the geometry at (c1) load step 7 and (c2) load step 20. Results of the total equivalent stress (von Mises) for the same simulation model but removed material plasticity, at (d1) load step 7 (begin of plastic deformation) and (d2) load step 20 (fully developed plastic deformation). The cutting plane located in the center is shown in (b), (c), and (d).

has been modeled as a purely elastic material; see Fig. 6d1 and d2) strengthens the argument that copper plasticity is the reason for the crack deflection. The stress fields at the same time point show no emerging compression area in the model of the *Y*-normal stress and also show a straight line towards the developing Cu stress field for the total equivalent stress, thus indicating that plasticity is a dominating root cause in building stress fields that steer a crack around an obstacle.

To gain a further understanding of the observed crack steering in the proof-of-concept experiment, a simulation geometry ($1 \mu\text{m}^3 \times 0.3 \mu\text{m}^3 \times 0.1 \mu\text{m}^3$) is created to mimic the cracked sample interface (magnification of Fig. 5) of the tensile test; see Fig. 7a. The analysis focuses on the stress-strain fields around the tip of a predefined crack ($0.05 \mu\text{m}^3 \times 0.1 \mu\text{m}^3 \times 0.1 \mu\text{m}^3$) in the SiO₂ dielectric. A central copper via, characterized by trapezoidal base dimensions (0.3 μm lower base, 0.1 μm upper base, 0.1 μm height), obstructs the crack propagation. The crack is positioned at the center height in front of the copper trapezoid. Stress is applied by gradually displacing the upper lever by 70 nm while keeping the lower lever fixed. Consistent with the previous simulation, the onset of copper plastic deformation marks the emergence of a compressed region in front of the obstacle, as observed in the *Y*-normal stress field; see Fig. 7b. The tensile stress field indicates potential for crack propagation in both upward and downward directions from its defined origin. Due to the stress maxima at the bottom edge of the predefined crack, the *Y*-normal stress suggests the start of the crack propagation at the bottom edge. Examination of the total equivalent stress (see Fig. 7c) reveals the highest stresses being below the predefined crack, also suggesting crack initiation at the bottom edge with possible propagation towards the

top or bottom due to the overall stress field. Notably, the visualization of the total equivalent stress unveiled a broad stress field below the crack, unaccounted for by the *Y*-normal stress and thus must be attributed to the *X*-normal stress. The depiction of the *X*-normal stress, in Fig. 7d, shows the mentioned wide stress field beneath the crack and illustrates the development of a compressed area below the crack at the lower model boundary. The propagating crack would navigate away from this compressed region and follow the upwards orientated tensile stress field, favoring its advancement. With consistent indication of an upward crack propagation across all three stress models, it is likely that the crack will circumvent the trapezoid and move upward before approaching at the copper via.

In summary, FEM simulations are used to gain understanding of the observed crack deflection near copper vias in the tensile test. In the simulations, the formation of copper plasticity generates a compressed area in front of the obstacle, which is the reason for the deflection of the advancing crack. When facing an obstructing via, stress-strain fields indicate crack propagation towards the thinner part of the via, aligning well with the observed cracking trajectory in the proof-of-concept experiment.

The FEM simulation of the stress-strain fields around the crack tip gives valuable insights about the fundamental stress acting on the crack tip during its propagation. They give a deeper idea about the key mechanisms which control the direction of crack propagation when facing an obstacle. Implementing exact replication of the crack stop into the sample structure of the FEM model, aids visualizing the local stress and contributes towards understanding the observed fracture behavior. With the help of the FEM model, experimental data can be quantified by determining the cracking parameters in the simulation which constitutes an essential supplement in specifying the performance of crack stop structures.

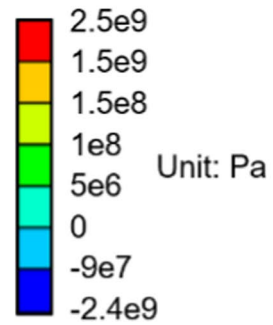
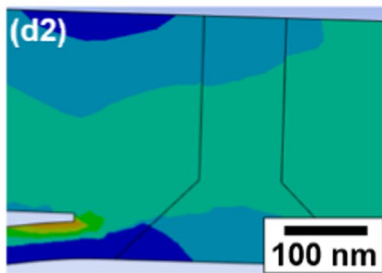
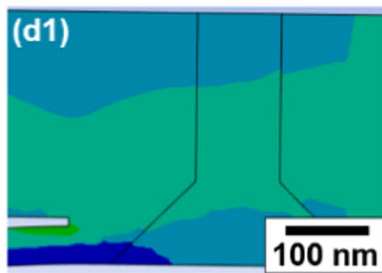
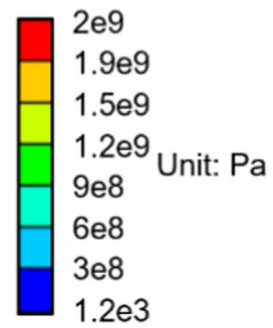
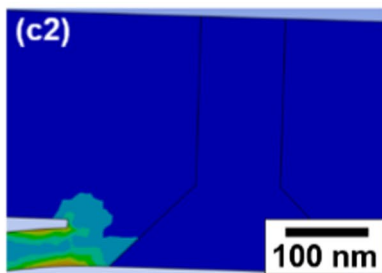
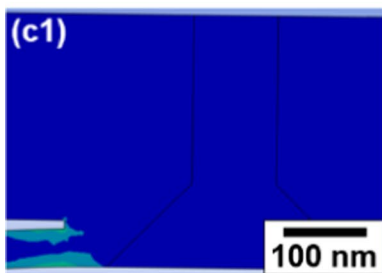
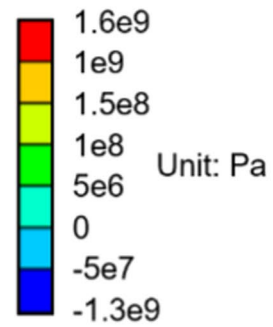
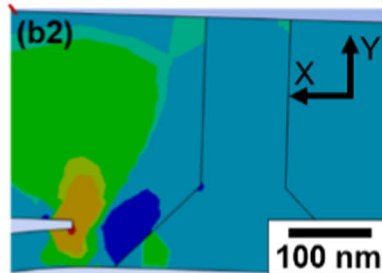
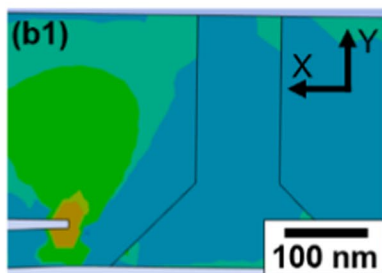
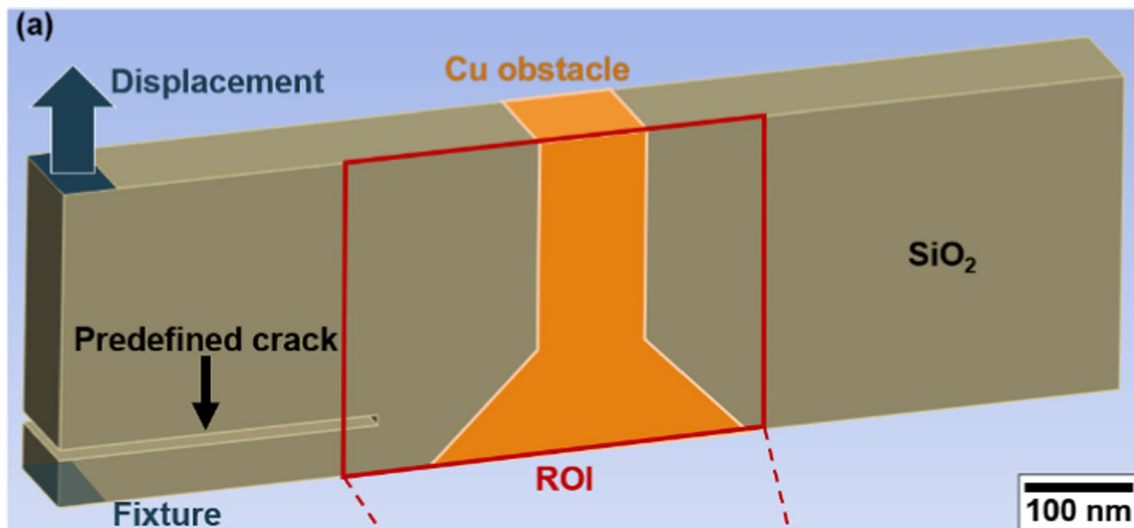
Conclusions

Microcracks generated at the rim of the microchip during the wafer dicing process are a risk for failure when propagating into the BEoL. Crack stop structures are integrated between the rim and BEoL of a microchip to prevent cracks from propagating into the on-chip interconnect stack structure and eventually to prevent mechanical failure of the chip. During operation, the growth of existing cracks is dominated by occurring cyclic thermomechanical loads. To access the influence of the protective structure on fatigue microcrack propagation and to gain understanding of the crack steering mechanisms, controlled micromechanical tests with cyclic loading of the BEoL structure are required. By pure mode-I testing, understanding of the major crack initiation and propagation mechanisms can be obtained.

In this study, a test specimen design for microcracking of on-chip interconnect stack structures was presented which enables

Table 1 Material properties of SiO₂ and polycrystalline copper (Cu_{poly}) applied in the FEM simulation, along with the corresponding references (Ref.) and indication of suitable assumptions (asm)

	SiO ₂	Cu _{poly}	Reference	
Young's modulus E [GPa]	60	128	[12]	[13]
Tangent modulus E_T [GPa]	6	0.45	asm	–
Elastic limit σ_Y [GPa]	2	0.15	asm	[14]
Fracture stress σ_F [GPa]	364	240	[12]	[14]
Fracture strain ϵ_F	0.025	0.20	[15]	[14]
Poisson's ratio	0.17	0.35	[16]	[17]



◀**Fig. 7** (a) ANSYS model of the cracked interface of the experiment geometry in Fig. 5 where a crack propagates towards a Cu obstacle in SiO₂ bulk material. (b) Results of the *Y*-normal stress field inside the geometry at (b1) load step 7 and (b2) load step 20. Outcome of the total equivalent stress (von Mises) field inside the geometry at (c1) load step 7 and (c2) load step 20. Results of the total equivalent stress (von Mises) for the same simulation model but removed material plasticity, at (d1) load step 7 (begin of plastic deformation) and (d2) load step 20 (fully developed plastic deformation). The cutting plane located in the center is shown in (b), (c), and (d).

pure mode-I loading as well as fatigue loading of BEoL structures to examine its failure mechanisms. In situ testing using x-ray microscopy facilitates the initiation and propagation of microcracks in the nanostructured BEoL with simultaneous high-resolution visualization of the crack states in 3D. The feasibility of the new cantilever specimen design for the generation and propagation of cracks in the BEoL is demonstrated in a proof-of-concept experiment where the pure interconnect specimen broke planar through one dielectric layer of the BEoL.

The proof-of-concept experiment demonstrated that the propagation of microcracks in 3D nanostructured systems can be imaged non-destructively using x-ray microscopy, opening the possibility of exploring the fatigue behavior of a broad field of materials. The ability to visualize the entire kinetic process of crack propagation in materials will provide an essential contribution to the understanding of fracture mechanics in small dimensions.

Post-mortem SEM analysis of the fractured interface revealed crack propagation through a dielectric layer with early deflections of crack propagation near intersecting copper vias. Deliberate simulations of a predefined microcrack encountering an obstacle reveal the prevailing stress-strain fields acting on a crack tip and facilitate the understanding of microcrack kinetics in on-chip interconnect stack structures. The FEM model indicated the emergence of copper plasticity as the reason for the formation of a compressive stress zone in front of the obstacle which is the potential cause for the redirection of the crack path.

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References

1. H. Li and M. Kuhn, Controlled fracture and mode-mixity dependence of nanoscale interconnects. *IEEE Trans. Device Mater. Reliab. A* 17, 636 (2017).
2. M. Rabie, N. A. Polomoff, M. K. Hassan, V. L. Calero-DdelC, D. Degraw, M. Hecker, M. Thiele, E. M. Bazizi, in 2018 IEEE 68th Electronic Components and Technology Conference (ECTC) (2018) pp. 460–466.
3. T. Shaw, E. Liniger, G. Bonilla, J. Doyle, B. Herbst, X. H. Liu, M. Lane, in International Interconnect Technology Conference (2007) pp. 114–116.
4. J. Molina-Aldareguia, I. Ocana, D. Gonzalez, M. Elizalde, J. Sanchez, J. Martinez-Esnaola, J. Gil-Sevillano, T. Scherban, D. Pantuso, B. Sun, G. Xu, B. Miner, J. He, and J. Maiz, Adhesion studies in integrated circuit interconnect structures. *Eng. Fail. Anal.* 14, 349 (2007).
5. K. Kutukova, S. Niese, C. Sander, Y. Standke, J. Gluch, M. Gall, and E. Zschech, A laboratory x-ray microscopy study of cracks in on-chip interconnect stacks of integrated circuits. *Appl. Phys. Lett.* A113, 091901 (2018).
6. E. Zschech, M. Löffler, P. Krüger, J. Gluch, K. Kutukova, I. Zglobicka, J. Silomon, R. Rosenkranz, Y. Standke, and E. Topal, Laboratory computed x-ray tomography – a nondestructive technique for 3d microstructure analysis of materials. *Pract. Metallogr. A* 55, 539 (2018).
7. K. Kutukova, J. Gluch, M. Kraatz, A. Clausner, and E. Zschech, In-situ x-ray tomographic imaging and controlled steering of microcracks in 3d nanopatterned structures. *Mater. Des.* A 221, 110946 (2022).
8. K. Vanstreels and H. Li, J.J. Vlassak, *Mechanical Reliability of Low-k Dielectrics*. ed. M.R. Baklanov, P.S. Ho, and E. Zschech (Chichester: John Wiley & Sons Ltd, 2012), pp. 339–367.
9. K. Kutukova, In-situ study of crack propagation in patterned structures of microchips using x-ray microscopy, doctoral thesis, BTU Cottbus - Senftenberg (2023).
10. E. Gullikson, x-ray Attenuation Length. (CXRO The Center for x-ray Optics, 2023), https://henke.lbl.gov/optical_constants/atten2.html. Accessed 13 September 2023.
11. S. Niese, Lab-based in-situ x-ray microscopy - methodical developments and applications in materials science and microelectronics, doctoral thesis, BTU Cottbus - Senftenberg (2015).
12. W.N. Sharpe, J. Pulskamp, J. Gianola, C. Eberl, G. Polcawich, and R.J. Thompson, Strain measurement of silicon dioxide microspecimens by digital image processing. *Exp. Mech.* A 47, 649 (2007).
13. A. Buch, *Pure Metals Properties: A Scientific-Technical Handbook* (Novelty: ASM International, 1999).
14. M. Smolka, Temperaturabhängige mechanische Eigenschaften miniaturisierter Kupferstrukturen aus der Leistungshalbleiterelektronik, doctoral thesis, Montanuniversität Leoben (2011).
15. T. Yoshioka, T. Ando, M. Shikida, and K. Sato, Tensile testing of SiO₂ and Si₃N₄ films carried out on a silicon chip. *Sens. Actuators A*. 82, 291 (2000).
16. Eigenschaften von Quarzglas. (Heraeus Holding, 2023), https://www.heraeus.com/de/hca/fused_silica_quartz_knowledge_base_1/properties_1/properties_hca.html#tabs-608478-6. Accessed 12 April 2023.
17. M. Ashby, Material Property Definitions – a summary. (Ansys Inc, 2021), <https://www.ansys.com/content/dam/amp/2021/august/webpage-requests/education-resources-dam-upload-batch-2/properly-definitions-BOKMPDFEN21.pdf>. Accessed 15 April 2023.

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