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ORIGINAL RESEARCH ARTICLE

Electronic Structure and Quantum Transport Properties of 2D SiP: A First-Principles Study

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Abstract

With the rapid evolution of microelectronics, the field of integrated circuits is facing unprecedented challenges. Traditional silicon-based transistors cannot maintain the advantages of high performance during the process of further ultra-scaling due to severe short-channel effects. Two-dimensional (2D) materials are potential channel materials that can replace silicon. Herein, 2D SiP is predicted to have a band gap of 1.49 eV with anisotropic electronic properties by means of first-principles calculations, which is suitable as a channel candidate of transistors. Hence, we investigate the ballistic transport properties of 2D SiP double-gate metal oxide semiconductor field-effect transistors (MOSFETs) by using ab initio quantum transport simulations. Despite anisotropic electronic properties of 2D SiP, the performances of monolayer SiP MOSFETs have weak directional dependence due to high valley degeneracy. The *n*-MOSFETs with 10-nm gate length can fulfill the high-performance requirements of the International Roadmap for Devices and Systems 2020 Edition (IRDS 2020). However, the *p*-MOSFETs cannot fulfill the demands of IRDS 2020 because of heavy hole effective masses. Considering the appropriate on-current of 1292 µA/µm for SiP *n*-MOSFETs, 2D SiP could be utilized as a potential channel material in the next-generation FETs.

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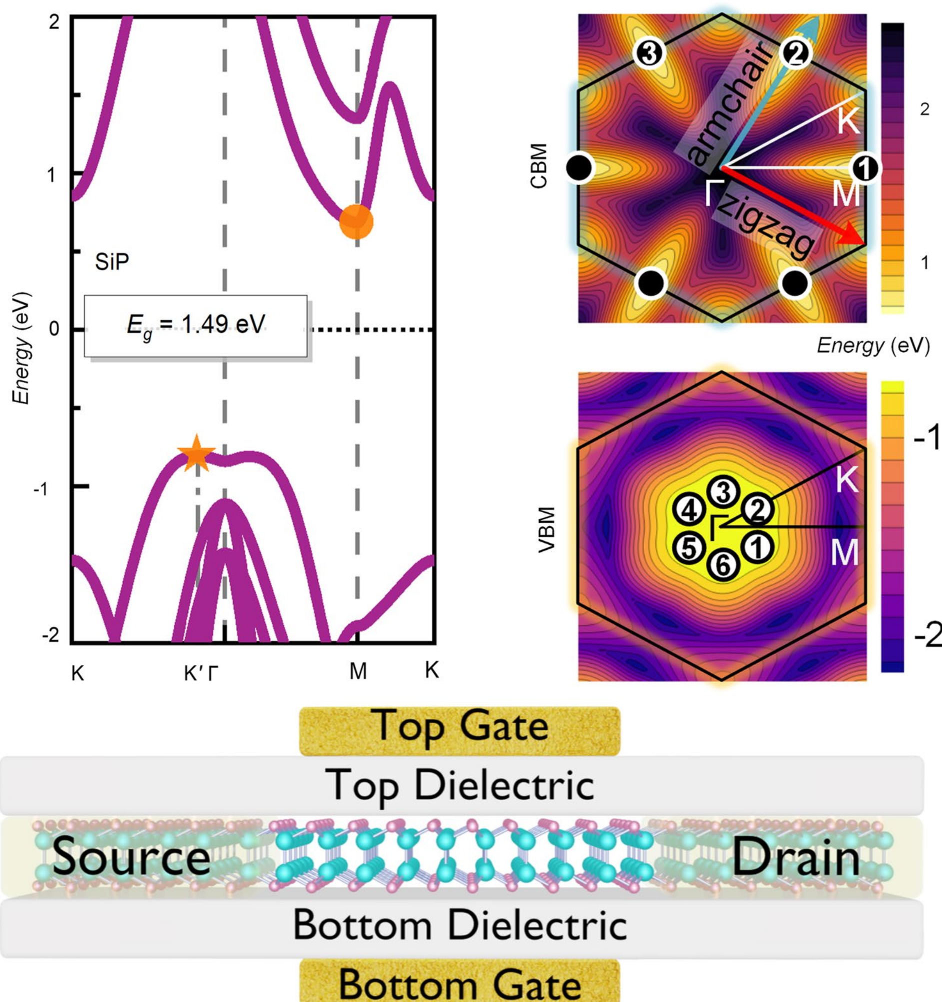
Graphic abstract



Keywords 2D materials · SiP · electronic structure · transport properties · first-principles calculations

Introduction

The electronics industry has compelling demands for electronic products with excellent performance.[1–4] However, traditional silicon field-effect transistors (FETs) have approached their physical limit so that they cannot maintain the advantages of high performance (HP). Because of the short-channel effect, increased leakage current, and excessive power consumption, it is difficult for silicon FETs to scale down to 10-nm gate length with satisfactory performance.[4–6] To address these issues, two-dimensional (2D) materials are proposed as the next-generation potential channel candidates to replace traditional bulk silicon.[1,7–9] 2D materials show characteristics of atomic thickness, no dangling bonds, and smooth surface, resulting in the integrity of electrostatic and fewer traps on the interface of the semiconductor-dielectric, which are suitable for ultra-scale channel materials.[10–16]

The most intensively concerned 2D semiconductors for FETs are MoS_2, black phosphorene (black P), and InSe.[17–19] 2D MoS_2 FETs with sub-10-nm channel length have been fabricated, which show a high on/off ratio of 10^7.[20] However, the MoS_2 FETs suffer from low on-state current ($I_{on} < 250$ μA/μm) and thus low switching speed.[2,21] 2D black P and InSe have high I_{on}, but their device performance degrades in the air due to ambient instability.[19,22–26] Therefore, identifying novelty 2D materials with proper band gaps is critical for HP applications.

Recently, 2D silicon phosphide (SiP) has drawn increasing attention among 2D materials.[27] According to the calculations of density functional theory, 2D SiP with the space group $P\bar{6}m2$ is highly stable, and it has higher

cohesive energy than silicene and phosphorene.[28,29] 2D SiP has an appropriate band gap of ~1.5 eV, which is expected to facilitate photocatalytic water splitting because its band gap straddles the redox potentials of water.[30] The monolayer SiP has potential for application in optoelectronic devices due to the high absorption in the visible light wavelength region.[30] Additionally, 2D SiP exhibits the ZT value of 0.98 for *n*-type and *p*-type doping at room temperature, which makes it a promising candidate for efficient thermoelectric devices.[27] However, research on the transport properties of 2D SiP is lacking. For the 2D SiP with a tunable band gap,[31] it is urgent to explore its transport properties and potential performance of FETs.

Here, electronic properties of 2D SiP, including band structure, projected density of states, and effective masses, are obtained by means of density functional theory. We find that it has anisotropic electronic properties with obvious direction-dependent effective masses. Then, we explore the device performance of 2D SiP double-gate metal oxide semiconductor FETs (MOSFETs) along two transport directions using ab initio quantum transport simulations. The on-state current, subthreshold swing, delay time, and power-delay product of 2D SiP *n*-MOSFETs can fulfill the HP requirements of the International Roadmap for Devices and Systems 2020 Edition (IRDS 2020).[32] Hence, 2D SiP has great potential as the channel material for integrated circuits application.

Methods

Structure relaxation and electronic properties of 2D SiP and device characteristics of MOSFETs are calculated by the Quantum Atomistix ToolKit 2020 package coupled nonequilibrium Green's function (NEGF) formalism.[33,34] The Perdew-Burke-Ernzerhof (PBE) exchange-correlation function is used in the generalized gradient approximation (GGA).[35] Numerical LCAO basis sets containing FHI pseudopotential with double-zeta-polarized (DZP) basis function have been used. In order to shield layered interactions, the vacuum space is chosen as 40 Å. The cutoff energy of 75 Hatree and 24 × 24 × 1 Monkhorst-Pack *k*-points are adopted. For accuracy, force tolerance is 1×10^{-2} eV/Å and stress-error tolerance is 0.05 GPa.

MOSFET models including dielectric layer with dielectric constant $\varepsilon = 4.0$ and double metal gates are used to estimate device performance. 50 × 1 × 100 *k*-mesh is sampled. The Poisson equation is self-consistently solved to treat the electrostatics, and the periodic, Neuman, and Dirichlet bounary conditions are used along the transverse direction, the direction normal to SiP surface, and transport direction, respectively. The Landauer-Bűttiker formula[36] gives the drain current $I_{\rm d}$

$$I_d(V_{\rm ds}, V_g) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E, V_{\rm ds}, V_g) \times [f_S(E-\mu_S) - f_D(E-\mu_D)]\}{\rm d}E, \quad (1)$$

where e is the elementary charge and h is the Planck constant. At a given bias voltage $V_{\rm ds}$ and gate voltage $V_{\rm g}$,$T(E, V_{\rm ds}, V_g)$ is the transmission coefficients. For a given Fermi level of the source μ_S and drain μ_D, $f_{\rm S}$ and $f_{\rm D}$ are the Fermi–Dirac distribution function of corresponding electrode. The transmission coefficient $T(E)$ is the average of k-dependent transmission coefficients $T_{k_\parallel}(E)$ over the Brillouin zone.

At energy E, the k-dependent transmission coefficient $T_{k_\parallel}(E)$[34] is

$$T_{k_\parallel}(E) = Tr[\Gamma^S_{k_\parallel}(E) G_{k_\parallel}(E) \Gamma^D_{k_\parallel}(E) G^\dagger_{k_\parallel}(E)], \quad (2)$$

where $k_\parallel$ is the reciprocal lattice vector parallel to the surface in the irreducible Brillouin region. In the formula, $G_{k_\parallel}(E)$ and $G^\dagger_{k_\parallel}(E)$ are the retarded and advanced Green's function, correspondingly. $\Gamma^S_{k_\parallel}(E) = i(\Sigma_S - \Sigma^\dagger_S)$ and $\Gamma^D_{k_\parallel}(E) = i(\Sigma_D - \Sigma^\dagger_D)$ are the level broadening originating from the source and drain in the form of self-energy Σ_S and Σ_D, respectively.

Results and Discussion

Firstly, we optimize the monolayer SiP structure and analyze its bonding properties. Figure 1a shows that monolayer SiP possesses a honeycomb lattice with $P\bar{6}m2$ space group. The lattice parameters of the monolayer SiP are marked as $a = b = 3.52$ Å. As is illustrated in Fig. 1b, the Si atoms in the inner two sublayers and the P atoms in the outer two sublayers are arranged in unequivalent positions in the order of P–Si–Si–P. The Si–Si and Si–P bond lengths are $d_1 = 2.36$

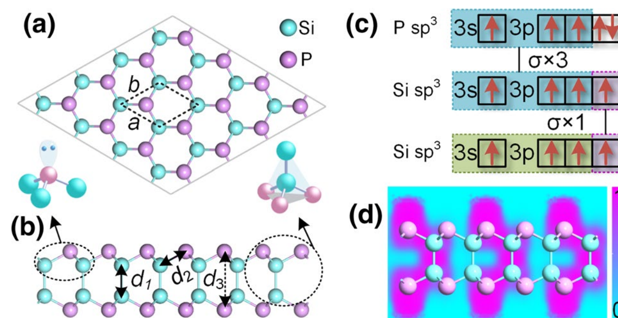


Fig. 1. **a** Top and **b** side view of hexagonal monolayer SiP structure and atomic orbital hybridization. **c** The valence-bond model of the monolayer SiP using valence electrons distributed in sp^3 hybridization for Si atoms and P atoms. **d** The electron localization function of the monolayer SiP.

Å and $d_2 = 2.28$ Å, respectively, and the whole layer thickness is $d_3 = 4.42$ Å.

Figure 1c illustrates that P atom has five valence electrons, which are hybridized into sp^3 orbital to form three strong σ bonds with neighboring Si atoms and lone pair electrons. The four valence electrons of the Si atom are hybridized into sp^3 orbital to form four strong σ bonds with three P atoms and one Si atom.

To further confirm the bonding characteristic of 2D SiP, we calculate the electron localization function of SiP (1 1 0) cross section, as shown in Fig. 1d. Strong electron localization emerges in the middle of Si–Si and Si–P bonds, indicating strong covalent bonds. In addition, strong electron localization also appears at the outer layer of P atoms, indicating an electron pair.

Electronic properties of monolayer SiP are further calculated based on the optimized stable structure, which is primary for device performance. As illustrated in Fig. 2a, monolayer SiP has an indirect band gap of 1.49 eV.[27,29] The valence-band maximum (VBM) is located at the K' point between Γ and K, and the conduction-band minimum (CBM) is located at the M point. Notably, the band dispersion near CBM shows obvious anisotropy along the two directions (M–Γ and M–K). The band dispersion near VBM presents a Mexican hat, corresponding to the sharp van Hove singularity in the density of states (Fig. 2b), indicating an ultrahigh density of state. Orbital-projected density of states of 2D SiP show that VBM is mainly contributed by P–*p* and partly contributed by Si–*p* and P–*s*. The CBM is mainly contributed by hybridized 3*p* orbitals of Si and P atoms.

Furthermore, we comprehensively understand the anisotropy through below band contours and anisotropic effective masses. The CBM is threefold degenerate, and the VBM is sixfold degenerate, which is one of the reasons why VBM has a higher density of state than CBM. The energy variations of every valley (marked with numbers) along the armchair and zigzag direction show strong anisotropy in Fig. 2c. Therefore, the electron effective masses are sensitive to transport directions. As is illustrated in Table I, for valley1 and valley3, the electron effective mass along the armchair direction is 0.17 m_0 and that along the zigzag direction is 0.41 m_0. For valley2, the effective mass along the armchair direction is 1.54 m_0, which is 12 times higher than that along the zigzag direction (0.13 m_0). However, hole effective masses along two directions are similar to each other and are much larger than electron effective masses.

Table I Effective masses of carriers along varied transport directions ($|m_0|$)

Carrier type	Valley index	Armchair	Zigzag
Electron	Valley1	0.17	0.41
	Valley2	1.54	0.13
	Valley3	0.17	0.41
Hole	Valley1	4.80	3.32
	Valley2	3.59	4.32
	Valley3	3.59	4.32
	Valley4	4.80	3.32
	Valley5	3.59	4.32
	Valley6	3.59	4.32

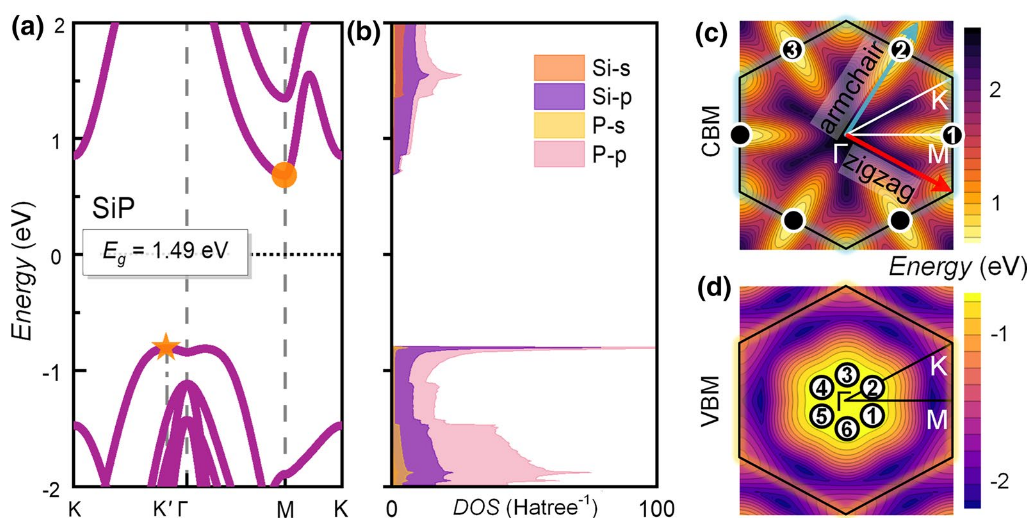


Fig. 2. **a** Electronic band structure of the monolayer SiP. The valence-band maximum (VBM) and conduction-band minimum (CBM) are marked by the orange pentagram star and the orange circle, respectively. **b** Projected density of states of the monolayer SiP. **c** Conduction and **d** valence band contours. The hexagon is the first Brillouin zone. The red and blue arrows demonstrate the zigzag and the armchair directions, respectively.

Motivated by the anisotropic electronic properties, we then studied the 2D SiP MOSFET device performance along two directions. The device structures of MOSFETs in the armchair and zigzag direction are presented in Fig. 3. The MOSFETs have *n*-type or *p*-type doped SiP as source and drain. The doping concentration of source and drain is 5.0×10^{13} cm^{-2}. The gate length is set to 10 nm without considering the underlap. The equivalent oxide thicknesses (EOT) and the supply voltage (V_{dd}) are set to 0.50 nm and 0.64 V, respectively. Detailed parameters are listed in Table II.

In a transistor, I_{on} is a key parameter to reflect device performance and a higher one means faster operating speed in HP servers. I_{on} is defined as the current of the transfer characteristic at a gate voltage V_g (on) = V_g (off) + V_{dd}, where V_{dd} is the supply voltage between source and drain, and V_g (off) is the gate voltage corresponding to the off state. I_{off} (0.01 μA/μm) is the current at the off state decided by IRDS requirements.

The curves in Fig. 3 show that *n*-type 2D SiP MOSFET along the armchair direction has the high I_{on} (1292 μA/μm) and on/off ratio (1.3×10^5), which satisfy IRDS 2020 requirements for HP applications for the year 2028. Additionally, the *n*-type device along zigzag direction (I_{on} = 1110 μA/μm) also successfully meets the HP requirements. Hence, there is a small difference in the *n*-type device performance between the two directions. Nevertheless, the *p*-type devices has lower I_{on} (15 μA/μm) than those of the *n*-type because the large effective mass of the *p*-type causes lower mobility of holes than electrons. The performance of *p*-type devices is almost the same in both directions.

Even though 2D SiP has anisotropic effective masses, the anisotropy of I_{on} is weak because of the compensation effect of high valley degeneracy.[37] High valley degeneracy

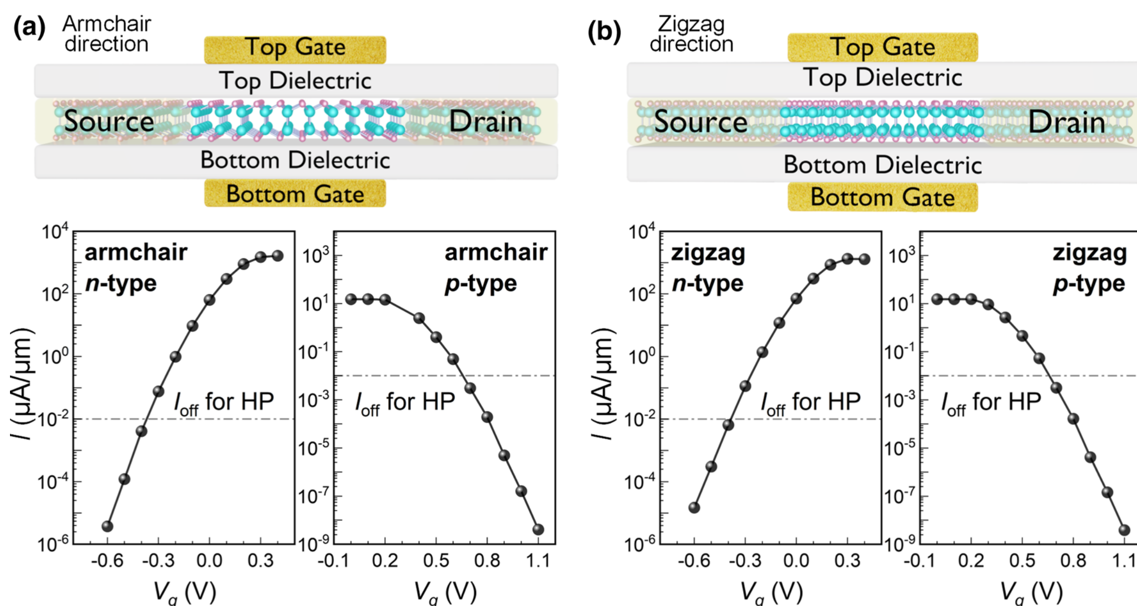


Fig. 3. Device structures without underlap and transfer characteristics of 10-nm gate length (L_g) monolayer SiP MOSFETs along the **a** armchair and **b** zigzag directions for HP applications. The doping concentration of source and drain is 5.0×10^{13} cm^{-2}.

Table II Device parameters in HP IRDS 2020 road map for the year 2028 and ours

Device parameters	IRDS2020 for 2028	Armchair *n*-type	Zigzag *n*-type	Armchair *p*-type	Zigzag *p*-type
L_g (nm)	12	10	10	10	10
V_{dd} (V)	0.65	0.64	0.64	0.64	0.64
EOT (nm)	\	0.50	0.50	0.50	0.50
I_{off} (μA/μm)	0.01	0.01	0.01	0.01	0.01
I_{on} (μA/μm)	924	1292	1110	15	15
SS (mV/dec)	75	65	75	63	69
τ (ps)	0.78	0.134	0.150	11.361	11.083
PDP (fJ/μm)	0.47	0.131	0.129	0.098	0.095

means that there are multiple valleys in the first Brillouin zone. In the 2D SiP, a valley along the light effective mass direction is always accompanied by the heavy effective mass direction of other valleys. Hence, the current increase (decrease) due to the low (high) effective mass of one valley is compensated by the current decrease (increase) due to the high (low) effective mass in the other valleys, leading to the inapparent change of the total current.

Subthreshold swing (SS) is a key figure of merit to describe the gate control ability of devices in the subthreshold region. From the transfer characteristics, the definition of SS is the gate voltage required to change the drain current by one order of magnitude. SS is described as $SS = \partial V_g / \partial \lg(I_{ds})$. A smaller SS presents a better gate control ability, and the limiting value of SS at room temperature is 60 mV/dec for MOSFETs. As shown in Table II, the SS of *n*-type SiP MOSEFTs are 65 and 75 mV/dec along the armchair and the zigzag directions, respectively. As for *p*-type devices, the SS along the armchair and the zigzag directions decrease to 63 mV/dec and 69 mV/dec, respectively.

To expose the gate modulation mechanism and current change, the position-resolved local device density of states and spectrum current of the 10-nm L_g MOSFET along armchair direction at different gate voltages (V_g) are shown in Fig. 4. Generally, total current consists of thermionic current (I_{therm}) and tunneling current (I_{tunnel}), separated by the effective barrier height (Φ_B). This effective barrier is able to suppress the transport of electrons from the drain to the source, and holes from the source to the drain.

For *n*-type, the device achieves I_{on} of 1292 μA/μm at $V_g = 0.27$ V, and the corresponding Φ_B is zero in Fig. 4a. Thermionic emission dominates the electron transport. To reduce the current to 0.01 μA/μm, V_g needs to be decreased to −0.37 V and the corresponding Φ_B increases to 0.24 eV in Fig. 4b. The transport by thermionic emission is greatly suppressed at off state. For *p*-type, the changes from on state to off state are similar to that of *n*-type. However, the total

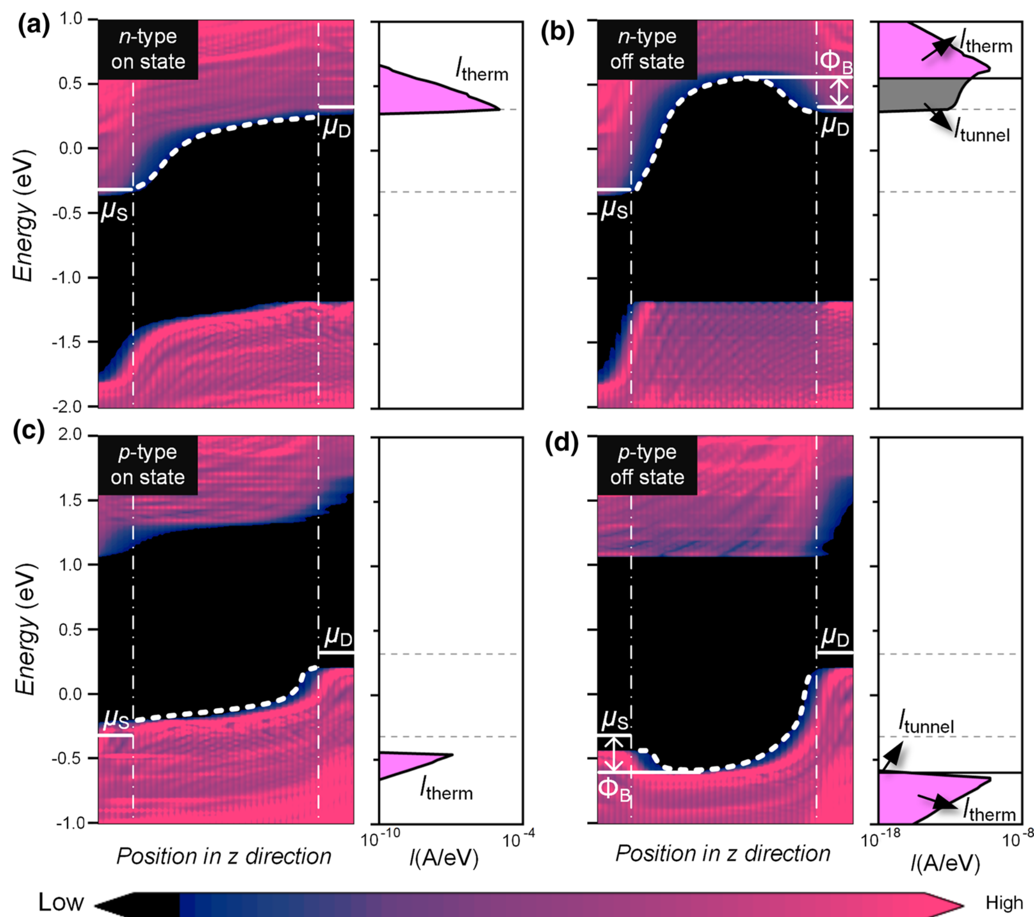


Fig. 4. Local device density of states and spectrum current plotted in log scales for 10-nm L_g monolayer SiP MOSFETs along the armchair direction under $V_{dd} = 0.64$ V. **a** *n*-type and on state. **b** *n*-type and off state. **c** *p*-type and on state. **d** *p*-type and off state. μ_S and μ_D represent the Fermi level at the source and drain, respectively. Φ_B is the effective barrier height. The dash dot lines are the boundaries between the channel region and the electrode.

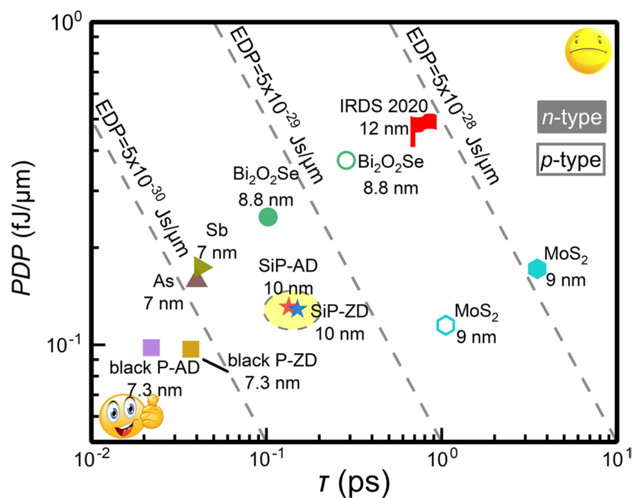


Fig. 5. Power-delay product (PDP) versus intrinsic delay time (τ) of SiP MOSFETs with 10 nm L_g for HP applications compared to other 2D materials. Gray dashed lines represent specific energy-delay product (EDP). The meaning of "SiP-AD 10 nm" is the SiP MOSFETs of 10 nm L_g along the armchair direction. The label "black P" represents the black phosphorene. Solid symbols represent *n*-type devices, and hollow symbols represent *p*-type devices.

current and I_{tunnel} of *n*-type device are higher than those of *p*-type device due to the light electron effective masses of 2D SiP.

In addition to the I_{on} and SS, we check the intrinsic delay time (τ), which is an important factor of evaluating the switching speed, and the lower one means the faster switching speed. τ is defined by the formula: $\tau = (Q_{on} - Q_{off})/I_{on}$,[14] where Q_{on} and Q_{off} are the total charge of the central region at the on state and off state, respectively. For monolayer SiP *n*-MOSFETs, τ are 0.134 ps and 0.150 ps along the armchair and the zigzag directions, which are obviously lower than those of *p*-MOSFETs according to Table II.

The PDP is another significant figure in a switching system, indicating the switching energy of MOSFETs. The PDP is represented as PDP = $(Q_{on} - Q_{off})V_{dd}/W$,[14] where W is the channel width. As presented in Table II, PDP of SiP *n*-MOSFETs and *p*-MOSFETs meet the IRDS 2020 requirements for HP applications, ranging from 0.095 to 0.131 fJ/μm.

It is important to obtain small τ and PDP for low power consumption and fast switching speed. To evaluate ultra-fast energy-efficient FETs more intuitively, the energy-delay product (EDP = PDP × τ) is extracted.[16] Figure 5 demonstrates PDP versus τ of SiP MOSFETs with 10 nm L_g for HP applications compared to other 2D materials, such as MoS_2,[38] black P,[23] arsenene,[39] antimonene,[39] Bi_2O_2Se.[38] Notably, τ and PDP of SiP *n*-MOSFETs surpass the IRDS 2020 requirements for HP target. The EDP values of SiP FETs are in the range of 5×10^{-30} ~ 5×10^{-29} Js/μm. Significantly, the EDP of SiP FETs is lower than that of MoS_2 and Bi_2O_2Se FETs at the ~10 nm L_g, indicating sufficient competitiveness among 2D FETs.

Conclusion

In summary, we investigate the electronic structure of 2D SiP and device performance of the 10-nm L_g MOSFETs. The monolayer SiP has an anisotropic band structure with an indirect band gap of 1.49 eV. The 10-nm L_g *n*-MOSFETs can fulfill the HP requirements of IRDS 2020 for the year 2028 in terms of I_{on} (1292 μA/μm), SS (65 mV/dec), delay time (0.134 ps), and power-delay products (0.131 fJ/μm). Because of the highly degenerate valleys, anisotropic effective masses do not lead to a strong directional dependence of device performance. In addition, the on-current of *n*-MOSFET is higher than that of *p*-MOSFET because the electron effective masses are lighter than the hole effective masses. Hence, we hope that our study could give an optimal path for the experimental investigation of 2D SiP transistors in next-generation HP devices.

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Conflict of interest The authors declare that they have no conflict of interest.

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