ORIGINAL RESEARCH ARTICLE

Gate Capacitance and Off-State Characteristics of E-Mode p-GaN Gate AlGaIn/GaN High-Electron-Mobility Transistors After Gate Stress Bias

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This study investigated the gate capacitance and off-state characteristics of 650-V enhancement-mode p-GaN gate AlGaIn/GaN high-electron-mobility transistors after various degrees of gate stress bias. A significant change was observed in the on-state capacitance when the gate stress bias was greater than 6 V. The corresponding threshold voltage exhibited a positive shift at low gate stress and a negative shift when the gate stress was greater than 6 V, which agreed with the shift observation from the I - V measurement. Moreover, the off-state leakage current increased significantly after the gate stress exceeded 6 V during the off-state characterization although the devices could be biased up to 1000 V without breakdown. The increase in the off-state leakage current would lead to higher power loss.

Key words: AlGaIn, GaN, E-mode, p-GaN, HEMT

INTRODUCTION

AlGaIn/GaN high-electron-mobility transistors (HEMTs) have been widely applied in switching power supplies because of their superior GaN-based properties.^{1–10} These excellent properties include high electron mobility, a high breakdown field, and good thermal characteristics. At the interface of the AlGaIn and GaN layers, a two-dimensional electron gas (2DEG) with a high concentration of electrons is formed as a device channel because of spontaneous and piezoelectric polarizations to further reduce on-resistance.^{11–19} An enhancement-mode (E-mode) transistor is preferred in power switching circuits; therefore, AlGaIn/GaN HEMTs with a p-GaN or p-AlGaIn gate layer for depleting the underneath 2DEG channel are the major technology currently used to achieve E-mode operation.^{20–23} If a p -type ohmic contact metal is used for the gate electrode, the gate will start to turn on at relatively low

positive gate voltages and induce a high gate leakage current, thereby limiting the input gate voltage swing in E-mode operation. However, if a Schottky contact metal is used for the gate electrode, the gate leakage current can be reduced at a high positive gate voltage and the input gate voltage swing can be increased. When a positive gate bias is applied, diode D1 (formed by Schottky gate metal/p-GaN) is reverse-biased and D2 (formed by p-GaN/AlGaIn/GaN) is forward-biased. At a high positive gate bias, the D1 formed at the gate metal and p-GaN dominate the gate leakage current because of the drop in reverse voltage on the Schottky diode. Several published studies have investigated the device characteristics of p-GaN gate AlGaIn/GaN HEMTs, including their threshold voltage shift, leakage current, and degradation mechanisms.^{21,24–33} However, prior research focused on the device I - V characteristics. The present study investigated the gate capacitance and device off-state characteristics of E-mode p-GaN gate HEMTs with Schottky gate metallization after gate stress for the first time. To use C - V measurement to investigate the p-GaN gate characteristics can

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further understand the Schottky gate diode and p-GaN/AlGaIn/GaN diode after various gate bias stress. The off-state current measurement right after the gate bias stress is to reproduce the real on-off operation during the high-frequency switching. To understand the effect after positive gate bias if any effect on the off-state current and breakdown voltage.

EXPERIMENTAL RESULTS AND DISCUSSION

Commercially packaged 650-V-rated devices with a gate width of 118 mm were studied. E-mode p-GaN/AlGaIn/GaN HEMTs were grown on 6-in. Si substrate and fabricated by Taiwan Semiconductor Manufacturing Company. The gate length and the gate-to-drain distance are 1.4 μm and 18 μm , respectively. To investigate the p-GaN gate stability, various gate positive biases were applied for 10 s before C - V and the off-state measurements.

The gate positive biases ($V_{GS, \text{stress}}$) were 1, 2, 3, 4, 5, 6, 7, 8, V with $V_{DS} = 0$ V. After each $V_{GS, \text{stress}}$, the gate C - V ($V_{DS} = 0$ V) and off-state characteristics ($V_{GS} = 0$ V) were measured and compared with the without-stress measurements. After the measurement, all voltage biases were removed for 30 min before the next stress measurement to confirm if the device could be fully recovered. Figure 1 plots the measured C - V characteristics after different gate stress voltages under frequencies of 1 kHz, 10 kHz, 100 kHz, and 1 MHz.

The measured gate C - V characteristics revealed a typical off-to-on transient as the gate voltage increasing from 1 V to 3 V, indicating the threshold voltage (V_{TH}) was approximately 2 V. Once the device was turned on, the measured capacitance remained constant. The measured capacitances in the off-state did not exhibit distinct differences; however, the capacitances measured in on-state bias conditions (for example $V_{GS} = 5$ V) exhibited significant differences in the values under different gate stresses. Figure 2 shows the normalized capacitance measured at $V_{GS} = 1$ V and 5 V versus various gate stresses ($V_{GS, \text{stress}}$) under different measurement frequencies. The normalized capacitance is the measured capacitance of each gate-stress divided by the capacitance without gate-stress. The change in the measured capacitance at $V_{GS} = 1$ V was small but still demonstrated an effect from gate stress. However, a significant change was observed when the gate stress was greater than 6 V, as shown in Fig. 2b. The increase in the measured capacitance was more than 20% at low frequencies. When the device is turned on, the gate structure from the gate electrode to the 2DEG channel consists of a Schottky diode (D1) formed of gate-metal/p-GaN and a p-GaN/AlGaIn/GaN diode (D2) in series, as shown in Fig. 3. As described in Ref. 23, when the V_G is higher than 1.5 V, the voltage drop across D2 is almost saturated (due to the forward bias at D2) and the applied V_{GS} is mostly across D1. Therefore, at a high positive V_{GS} bias, the Schottky diode (D1) limits the leakage current because of reverse bias. Because the capacitance value of D1

Fig. 1. C - V characteristics of the E-mode p-GaN gate HEMT after different gate stress voltages. Measured at frequencies of (a) 1 kHz, (b) 10 kHz, (c) 100 kHz, and (d) 1 MHz ($V_{DS} = 0$ V).

Fig. 2. Normalized capacitance versus gate stress voltage ($V_{GS, stress}$) obtained at (a) $V_{GS} = 1$ V and (b) $V_{GS} = 5$ V in Fig. 1 ($V_{DS} = 0$ V).

from the depletion region is smaller than that from the forward-biased D2, the measured capacitance is the result of D1 in series with D2. Therefore, the change (increase) in Fig. 2b was attributed to the change inside D1, which was mostly in the depletion region of D1, as shown in Fig. 3c.³⁴ Based on the two-junction model described in Ref. 34, a junction capacitor (C_{D1}) due to the Schottky metal/p-GaN junction was added in series with the AlGaIn barrier capacitor (C_{D2}). The total capacitance value (C_{total}) is given by:

$$\frac{1}{C_{total}} = \frac{1}{C_{D1}} + \frac{1}{C_{D2}}. \quad (1)$$

The C_{D2} is simply calculated by using the ideal dielectric constant of the AlGaIn and assumed to be constant. At $V_{GS} = 5$ V and $V_{DS} = 0$ V, most of the applied gate voltage drops across the depletion region in the diode D1 once the 2DEG has been formed. The small-signal capacitance C_{D1} is given by:

$$C_{D1} = \frac{dQ_{g-pGaN}}{dV_g}. \quad (2)$$

Therefore, an increase of the measured capacitance is mostly due to the change in the charge density (Q_{g-pGaN}) within the p-GaN layer. This was mainly because of hole/electron injection into the p-

Fig. 3. (a) Device cross section and (b) equivalent diodes (D1 and D2) and band diagram (at 0 bias), (c) band diagram (at high V_{GS} bias) in the gate structure of an E-mode p-GaN gate HEMT.

GaN region after high positive gate stress and the carriers being trapped in the p-GaN region.²⁵ The trapped carriers resulted in a change in the measured capacitance, especially in the low-frequency measurement where the trapping/detrapping time constant was long. At measurement frequencies less than 10 kHz, the effect from high positive gate stress was significant and exhibited an increase of

more than 20%. Using this characterization measurement, the quality of p-GaN can be revealed when the gate is under high positive bias.

As described previously, the measured gate C - V characteristics in Fig. 1 exhibit the typical off-to-on transient as the gate voltage increased from 1 V to 3 V. To study the shift in threshold voltage (V_{TH}) after gate stress, the peak values of ΔC versus V_{GS} from the C - V curves in Fig. 1 were studied, and the corresponding V_{GS} (defined as $V_{G,peak}$ and V_{TH}) in the peak values of ΔC versus various gate stress voltages ($V_{GS, stress}$) was derived and plotted in Fig. 4. In this figure, the $V_{G,peak}$ (V_{TH}) shift is referred to as the value change of $V_{G,peak}$ compared with that without gate stress ($V_{GS, stress} = 0$ V). The obvious trend in Fig. 4 is a negative shift at $V_{GS, stress}$ of 1 V, and then a positive shift before $V_{GS, stress}$ increases to 6 V. Once $V_{GS, stress}$ is greater than 6 V, a significant negative shift is observed. A higher value of -0.23 V was obtained after positive 8-V gate stress was applied for 10 s. This observation is similar to the results in²⁹ for a Schottky p-GaN HEMT from a typical I_D - V_{GS} characteristic. The first positive shift was related to the electron injection, which accumulated or was trapped in the p-GaN layer. The negative shift at high gate stress bias was caused by the additional hole injection, which resulted in the negative shift observed in Fig. 4.

The off-state characteristics were measured immediately after various gate stress voltages were applied. For example, the off-state leakage current I_D was measured up to V_{DS} of 1000 V at $V_{GS} = 0$ V right after $V_{GS, stress}$ of 1 V for 10 s. After the off-state measurement, all voltage biases were removed for 30 min before the next stress measurement to confirm whether the device could be fully recovered. Figure 5 illustrates the measured off-state current versus the drain bias after various gate stress voltages. The packaged devices could be biased up to 1000 V without breakdown. The off-state current was as low as 10^{-8} mA/mm before 200 V, and then increased to 10^{-4} mA/mm at 1000 V. However, the off-state current increased significantly after the gate stress exceeded 6 V during the off-state characterization when the V_{DS} was within 300 V.

Fig. 4. $V_{G,peak}$ shift versus the different gate stress voltages ($V_{GS, stress} = 0$ is for without stress).

Figure 6 shows a plot of the off-state current versus various gate stress voltages ($V_{GS, stress}$) at different V_{DS} values. Clearly observed is the off-state current increasing significantly at V_{DS} of 100 and 200 V after the $V_{GS, stress}$ exceeds 6 V. The increase is approximately three orders of magnitude. A possible reason is the negative shift of the threshold voltage while $V_{GS, stress}$ is larger than 6 V as shown in Fig. 4 because the off-state current was measured at $V_{GS} = 0$ V. The voltage difference between the gate bias (0 V) and the V_{TH} is reduced, thus the leakage current is possibly increased. Because of the negative shift in V_{TH} at high gate stress bias was caused by the additional hole injection. The accumulated holes in the p-GaN slightly induce the electrons in the channel and cause the leakage current.

However, the impact of the gate stress bias was limited and the increase in the off-state current was small when the V_{DS} was greater than 700 V.

CONCLUSIONS

This study investigated the gate capacitance and off-state current of 650-V E-mode p-GaN gate AlGaIn/GaN HEMTs after various gate stress voltages. The changes in the measured capacitance in the off- and on-states demonstrated the different effects of gate stress bias. The measured off-state gate capacitance did not significantly change because no 2DEG was in the channel under the

Fig. 5. Off-state drain current (I_D) characteristics after different gate stress voltages ($V_{GS} = 0$ V).

Fig. 6. Off-state drain current at $V_{DS} = 100$ –600 V ($V_{GS} = 0$ V) after different gate stress voltages.

gate, and thus, the capacitance was small and changed little. However, the measured on-state capacitance significantly increased when the gate stress bias was greater than 6 V, especially at low measurement frequencies. Moreover, the on-off transient voltage shifted because of the gate stress bias. A negative shift was observed when the gate stress bias was greater than 6 V. Finally, the off-state current was measured after various levels of gate stress bias; the off-state current exhibited a significant increase after larger gate stress biases when the drain bias was low, which is related to the threshold voltage shift. In conclusion, the threshold voltage, gate capacitance, and off-state current changed significantly after gate stresses greater than 6 V for the studied p-GaN gate AlGaIn/GaN HEMTs. This is why most commercial p-GaN gate HEMTs are unsuitable for biases greater than 6 V.

CONFLICT OF INTEREST

All authors declare that they have no conflict of interest.

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