On the Multi-parallel Diodes Model in Au/PVA/n-GaAs Schottky Diodes and Investigation of Conduction Mechanisms (CMs) in a Temperature Range of 80–360 K

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Au/PVA/n-GaAs (MPS) type Schottky diodes (SDs) were fabricated and investigated in a temperature range of 80–360 K to explain their possible conduction mechanisms (CMs). Three distinct linear regions with different slopes were observed in $\ln(I)$ – V plots. The first region (R1), is within the range of 0.22–0.60 V, the second region (R2), is within the range of 0.64–0.90 V, and the third region (R3), is within the range of 1.1–1.5 V. It was shown that both ideality factor (n) and zero-bias barrier height (Φ_{B0}) are strong functions of temperature for all three regions. It was noticed that n values decreased and Φ_{B0} values increased with increasing temperature. In order to ascertain the possible CMs, $\Phi_{B0} - n$, $\Phi_{B0} - q/2kT$, and $(n^{-1} - 1) - q/2kT$ plots were also examined. In each of these plots, two linear regions were obtained within each of the three regions. The region from 80–180 K is called the low-temperature range (LTR), and the region from 200–360 K is called the high-temperature range (HTR). It has been revealed that the reason for the deviation from the classical thermionic emission (TE) theory cannot be explained only by the existence of the interface layer, interface states (N_{SS}) or quantum mechanical tunneling mechanisms, which can be also explained by the double Gaussian distribution (DGD) due to barrier inhomogeneity. Finally, the experimental Richardson constants (A^*) were calculated from the interception point of the modified Richardson curve in LTR and HTR for all three regions. It was calculated as 6.22 and 8.13 A/cm²K² for R1, 7.77 and 8.14 A/cm²K² at R2, and 7.07 and 8.13 A/cm²K² at R3 for low- and high-temperature ranges, respectively. It is clear that especially HTR results are quite close to the known theoretical A^* value of 8.16 A/cm²K² for n-GaAs.

Key words: Au/PVA/n-GaAs SDs, possible conduction-mechanisms, multi-parallel diodes, double Gaussian distribution (DGD) of BH

INTRODUCTION

While Schottky diodes (SDs) were initially prepared by the tight contact of a metal and semiconductor (M/S), later, a polymer interface material was laid between the metal and the semiconductor, thereby composing a metal/polymer/semiconductor

(MPS) type SD. In addition, metal/insulator/semiconductor (MIS) type SDs have also been obtained by using an insulator as an interface material. Thus, the aim is to prevent diffusion in the M/S interface and to increase the quality of SDs by deactivating the interface states.^{1–4} Polyvinyl alcohol (PVA) polymer, which is used frequently in the literature, is preferred by researchers due to its physical and chemical properties such as high water solubility, large crystalline range, processability, low cost and ease of production.^{5,6} On the other hand, the low electrical conductivity of PVA can be increased up to 10^6 times with proper dopant material.^{5,7}

One of the most important reasons why SDs are still the topic of current research is that the current-transport mechanisms (CMs) in the interface of M/S become complicated at low temperatures. Therefore, it is essential to peruse the I – V characteristics of SDs over a wide temperature range.^{8–10} As it is known, I – V characteristics are examined with the thermionic emission (TE) theory which is valid at 300 K and above. At high temperatures, deviations from the ideal case can be observed due to interface states (N_{ss}), series resistance (R_s) and interface layer.¹¹ However, in order to have more detailed information about the barrier height (Φ_{Bo}) of SDs, measurements should be taken and analysed at low temperatures. Thus, there may be more data about possible CMs and the form of the barrier, as well as the opportunity to determine which of the possible CMs are dominant alone or together.

According to experimental results, as the temperature decreases, a rapid increase in ideality factor (n) and a decrease in barrier height (Φ_{Bo}) are generally observed.^{12,13} This behaviour of Φ_{Bo} is in agreement with the negative temperature coefficient (α) of forbidden bandgap (E_g) for GaAs semiconductors and BH for ideal SDs. This is because Φ_{Bo} is expected to decrease with increasing temperature, such as in the forbidden bandgap of the semiconductors due to its expansion under the temperature effect.^{9,14} At low temperatures and high-doped semiconductors, quantum tunnelling mechanisms such as field emission (FE) or thermionic field emission (TFE), multi-step tunnelling via surface states/traps, or T_0 anomaly are effective.^{14–19} In this case the slopes of $\ln(I)$ versus V plots are almost constant, and hence $n \cdot t$ becomes also constant. But, the higher value of experimental ideality factor at low temperatures and very-low value of Richardson constant (A^*) obtained cannot be explained by only tunnelling mechanisms. The obtained value of A^* is several orders lower than the theoretical value, and higher values of n is more important evidence to deviate from TE theory which is already often reported by many researchers recently.^{8–16} Such fluctuation in A^* , BH and n values can be attributed to the spatial inhomogeneous BH at the M/S interface, which consists of low and high barrier or patches, and hence an effective

active area is much smaller than the diode rectifier contact area.^{8,17–23} Lately, this case is explained by Gaussian distribution (GD) which reveals that the barrier in the M/S interface is not the only one, and it is predicted that there are many big or small barriers around an average barrier.^{13,17–19} If the carriers do not have enough energy to exceed the average barrier, they pass through these small barriers, which are called patches. Thus, the current and ideality factor is increased and the height of the barrier faced by the carrier is reduced.

In the literature, it can be seen that the low electrical conductivity of PVA, used as an interface material, is aimed to be increased by doping materials such as Zn and Gr.^{5,9} Nevertheless, it has not been found in the literature that CMs of an Au/PVA/n-GaAs MPS type SD, which can be seen as a reference sample, were examined in a wide temperature range. If the results of studies on this subject and application of semiconductor devices in technology are taken into account, in order to make a comparison, this study is considered to be important. Therefore, in this study, I – V measurements of Au/PVA/n-GaAs MPS type SD were taken in the range of 80–360 K in 20 K steps and such diode parameters n , Φ_{Bo} , and saturation current (I_0) is calculated by the forward bias I – V characteristics. As a result of semi-logarithmic I – V measurements, with different slope, three distinct linear regions such as low (0.22–0.60 V), intermediate/moderate (0.64–0.90 V) and high (1.1–1.5 V) bias regions were observed. This condition is called the three- or multi-parallel diode model in the literature.⁸ In addition, the results showed that for all three regions, there is a double Gaussian distribution (DGD), which is attributed to barrier inhomogeneity.

METHODOLOGY

On account of the preparation of Au/PVA/n-GaAs (MPS) type SDs, an n-type GaAs crystal with resistivity of 1–10 Ω cm, (100) float zone, and 300 μ m thickness is used. The n-GaAs wafer that was cut in 1 cm $\times$ 1 cm, was subjected to the cleaning process frequently used in the literature. Then, in order to prepare the ohmic contact of the diode by the thermal evaporating method, under 1.333 kPa pressure, 99.99% purity Au is deposited onto the whole back-matte side of the n-GaAs wafer with the mask which is 150 nm. The annealing process was performed in N_2 atmosphere for 3 min in order for ohmic contact to have low resistance. After formation of ohmic contacts, a PVA interlayer was deposited on the front, bright side of n-GaAs wafer by electrospinning. Finally, under a pressure of 0.533 kPa, again by the method of thermal evaporation, Schottky contacts with an area of 7.85×10^{-3} cm² were deposited on the polymer PVA interlayer by a mask with 150 nm dots. In our previous study,⁵ the preparation stage of the sample

was explained in detail. The I - V measurements of Au/PVA/n-GaAs MPS type SD were attained using a Keithley 2400 current-voltage source meter in the temperature range of 80–360 K in 20 K steps. The temperature of the sample was controlled by a Janis vpf-475 cryostat and Lakeshore model 321 temperature control systems.

RESULT AND DISCUSSION

Figure 1 shows the plot of the semi-logarithmic current-voltage (I - V) measurements of the Au/PVA/n-GaAs type SD. It is clear that the positive bias I - V curve has an exponential increase. In addition, there are three distinct linear regions with different slopes in the forward bias I - V curve. These linear regions are named Region 1, which is at low bias region (LBR) in the 0.22–0.60 V voltage range, Region 2, which is at moderate bias region (MBR) in the 0.64–0.90 V voltage range, and Region 3, which is at high voltage region (HBR) in the 1.1–1.5 V voltage range. These multi-linear regions are known as the multi-parallel diode model in the literature.⁸ Since each linear region is thought of as a different diode, it is beneficial to examine possible conduction mechanisms (CMs) separately. An Au/PVA/n-GaAs type SD can be defined as a three-parallel diodes model as there are three linear regions in the I - V curve of SD. The behavior of the three linear regions can be associated with the transmission of these diodes at different voltage values. For example, the first diode transmits at a voltage of 0.22 V, while the second diode transmits at a voltage of 0.64 V and the last diode at 1.1 V, as in the circuit shown in Fig. 2. In this way, three different linear regions appear at different voltage ranges.

Deviation from linearity due to the effect of R_s is observed under a sufficiently forward bias. The following equation is achieved using Kirchoff's current law on the circuit in Fig. 2.

$$I_{D1} + I_{D2} + I_{D3} + \frac{V_D}{R_{sh}} - I_t = 0 \quad (1)$$

It also seen that the circuit in Fig. 2 is

$$V_D = V - I_D R_s \quad (2)$$

Accordingly, the following equation is obtained:

$$I_t = I_{D1} + I_{D2} + I_{D3} + \frac{V - I_D R_s}{R_{sh}} \quad (3)$$

Using the obtained results of I - V measurements and Eq. 3, the basic diode parameters, namely, n , Φ_{Bo} , and I_o , were calculated using the following thermionic emission theory (TE) equations for all three regions^{8,20,21}:

Fig. 1. Semi-logarithmic I - V plot of Au/PVA/n-GaAs between 80 K and 360 K; (a) Region I, (b) Region II and (c) Region III.

$$I_t = I_{o1} \left[\exp \left(\frac{q(V - I_D R_s)}{n_1 k T} \right) - 1 \right] + I_{o2} \left[\exp \left(\frac{q(V - I_D R_s)}{n_2 k T} \right) - 1 \right] + I_{o3} \left[\exp \left(\frac{q(V - I_D R_s)}{n_3 k T} \right) - 1 \right] + \frac{(V - I_D R_s)}{R_{sh}} \quad (4)$$

$$n = \frac{q}{kT} \left(\frac{dV}{d(\ln I)} \right) \quad (5)$$

$$\Phi_{Bo} = \frac{kT}{q} \ln \left[\frac{AA^* T^2}{I_o} \right] \quad (6)$$

where n is the ideality factor, A is the rectifier contact area (0.00785 cm^2), A^* is the theoretical Richardson constant that is equal to $8.16 \text{ A/cm}^2 \text{ K}^2$ for n-GaAs, Φ_{Bo} or $\Phi_{Bo}(V)$ is the apparent barrier height for any bias voltage range, I_o is the reverse-bias saturation current and $I R_s$ is the voltage drop on the series resistance. k , T , and q are physical quantities known to all.^{20,21} To obtain the results seen in Table I, n values are calculated from the slope and Φ_{Bo} and I_o from the intercept point of the linear regions.

Looking at Fig. 3 and Table I, it is seen that n values decrease and Φ_{Bo} values increase with increasing temperature for all three regions. This can be thought of as the first clue that there is a deviation from the classical TE for Au/PVA/n-GaAs SD.^{22–24} This behaviour of Φ_{Bo} is in agreement with the negative temperature coefficient of BH for an ideal SD.^{12,17,25} With all these results, the n value being far from the ideal case ($n \gg 1$) can be explained by the existence of the interfacial PVA layer, image-force lowering, and interface states and is also attributed to barrier inhomogeneity due to strong dependence to the temperature.^{26,27} At low temperatures, carriers do not have enough energy to pass the barrier and attend to the transmission.

Fig. 2. Sketch of three/multi-parallel diodes circuit model of Au/PVA/n-GaAs type SD.

On the other hand, it is expected that Φ_{B0} must be decreased with increasing temperature like forbidden bandgap of semiconductor. However, considering that some points of the barrier in the metal–semiconductor interface are high or low (pinch-off), the carriers can transmit by tunnelling in the points where the barrier is low. This is known as Gaussian distribution (GD).^{12,13,17,28}

In order to study the existence of field emission (FE) and thermionic field emission (TFE) mechanisms, which are quantum mechanical tunnelling mechanisms due to deviation from classical TE, E_{oo} ($= nkT/q$) and E_o , which are tunnelling parameters that are the function of temperature, are theoretically calculated using the following equations^{29,30}:

$$I = I_{\text{tun}} \left[\exp \left(\frac{q(V - IR_s)}{E_o} \right) - 1 \right] \quad (7)$$

$$n_{\text{tun}} = \frac{E_{oo}}{kT} \coth \left(\frac{E_{oo}}{kT} \right) = \frac{E_o}{kT} \quad (8)$$

$$E_{oo} = \frac{h}{4\pi} \left(\frac{N_D}{m_e^* \epsilon_s} \right)^{1/2} \quad (9)$$

where m_e^* is the effective mass of the electron that is equal to $0.0067m_o$, ϵ_s is the dielectric constant of GaAs that is equal to $13.1 \epsilon_o$ and N_D is the doping concentration of donor atoms that is equal to $2.6 \times 10^{16} \text{ m}^{-3}$. At room temperature, theoretical E_{oo} and E_o values were calculated to be 33.6 meV, equally. It can be said that the FE is valid because the calculated E_{oo} or E_o value is greater than kT/q at room temperature is equal to 25 meV.

Also, the fact that E_{oo} and E_o values are theoretically equal to each other indicates the existence of a straight linear line.^{18,30,31} It is also seen in Table I that nT values are almost unchanged with changing temperature which is clue to TFE. When looking at the kT/q versus nkT/q plots shown in Fig. 4, for each of the three regions, the experimental E_o values were found as 113.2 meV, 157.2 meV, and 99.3 meV, respectively. As can be seen, these experimental values are higher than the theoretical E_o

values. Therefore, it can be surmised that TFE and T_o effect dominates like FE.^{8,32} It is known that one or more CMs can be dominant together or alone.³³ These results indicate that quantum mechanical tunnelling CMs are dominant over TE at low temperatures.

When looking at the plot of n versus Φ_{B0} in Fig. 5, there are two distinct linear regions with different slopes for all three regions. These are the low-temperature Region (LTR) in the range of 80–180 K and high-temperature Region (HTR) in the temperature range of 200–360 K. Also, the inverse proportion between n and Φ_{B0} is clearly seen. In the case of n equals 1, Φ_{B0} values were found different from each other for LTR and HTR in all three regions. In the literature, these results are attributed to the double Gaussian distribution (DGD) due to the lateral barrier inhomogeneities in the M/S interface.^{8,22,34} According to the results obtained so far in this study, the existence of DGD due to barrier inhomogeneity at low temperatures can be mentioned. In order to get more evidence of this, standard deviations (σ_o) and voltage coefficients (ρ_2 and ρ_3) were obtained by using the interpolations of the $q/2kT$ versus Φ_{B0} and $q/2kT$ versus $n^{-1} - 1$ plots of Au/PVA/n-GaAs type SD and the following equations^{12,35,36}:

$$\phi_{\text{ap}} = \phi_{B0}(T = 0) - \frac{q\sigma_o^2}{2kT} \quad (10)$$

$$\left(\frac{1}{n_{\text{ap}}} - 1 \right) = \rho_2 - \frac{q\rho_3}{2kT} \quad (11)$$

As can be seen in Fig. 6, there are two distinct linear regions for every three regions, which diverge into LTR (80–180 K) and HTR (200–360 K). σ_o and Φ_{ap} were obtained from slopes and intercept points of HTR and LTR, respectively.³³ As can be seen in Table II, σ_o values obtained in HTR have greater value than values obtained in LTR within all three regions. It can be concluded that the height of the barrier in HTR is higher and wider than in LTR. If the voltage dependence is compared by comparing the σ_o values of Region 1, Region 2 and Region 3, it

Table I. Temperature-dependent experimental I_0 , n , Φ_{B0} and nT values of Au/PVA/n-GaAs SD for all three regions

T (K)	Region 1 (low bias)				Region 2 (moderate bias)				Region 3 (high bias)			
	I_{01} (A)	n_1	Φ_{B01} (eV)	n_1T (K)	I_{02} (A)	n_2	Φ_{B02} (eV)	n_2T (K)	I_{03} (A)	n_3	Φ_{B03} (eV)	n_3T (K)
80	1.79×10^{-8}	17.23	0.165	1378.62	4.03×10^{-8}	21.13	0.159	1690.12	1.55×10^{-9}	13.63	0.182	1090.71
100	2.64×10^{-8}	14.33	0.206	1433.15	3.75×10^{-8}	15.95	0.203	1594.80	2.95×10^{-9}	11.27	0.225	1126.74
120	2.02×10^{-8}	11.60	0.254	1391.86	3.75×10^{-8}	13.76	0.248	1651.60	2.15×10^{-9}	9.25	0.277	1109.49
140	1.90×10^{-8}	9.79	0.301	1370.47	3.42×10^{-8}	11.42	0.294	1599.20	2.26×10^{-9}	7.92	0.327	1108.43
160	2.08×10^{-8}	8.80	0.346	1408.77	3.26×10^{-8}	10.00	0.340	1599.20	2.47×10^{-9}	7.08	0.376	1132.25
180	2.12×10^{-8}	7.74	0.393	1393.53	2.86×10^{-8}	8.54	0.388	1537.69	2.35×10^{-9}	6.20	0.427	1115.90
200	4.06×10^{-8}	7.30	0.429	1460.23	1.46×10^{-8}	6.35	0.447	1269.90	1.35×10^{-8}	6.13	0.448	1226.90
220	5.53×10^{-8}	6.88	0.470	1513.60	1.57×10^{-8}	5.67	0.494	1248.03	1.81×10^{-8}	5.63	0.491	1238.70
240	4.62×10^{-8}	6.08	0.520	1460.23	2.92×10^{-8}	5.76	0.529	1383.56	9.64×10^{-10}	3.99	0.600	958.20
260	6.69×10^{-8}	4.99	0.558	1296.89	1.35×10^{-8}	3.92	0.594	1017.93	9.98×10^{-8}	4.63	0.549	1203.97
280	1.18×10^{-7}	5.64	0.591	1579.59	3.13×10^{-8}	4.51	0.623	1261.61	4.32×10^{-9}	3.54	0.671	990.11
300	1.18×10^{-7}	5.13	0.637	1539.73	1.86×10^{-8}	3.82	0.685	1146.81	9.33×10^{-9}	3.46	0.702	1038.91
320	1.46×10^{-7}	4.97	0.677	1590.43	2.39×10^{-8}	3.67	0.727	1173.50	1.22×10^{-8}	3.29	0.745	1052.11
340	1.33×10^{-7}	4.53	0.725	1539.73	7.47×10^{-8}	4.10	0.743	1393.53	1.26×10^{-8}	3.11	0.795	1058.83
360	1.76×10^{-7}	4.28	0.763	1539.73	2.75×10^{-8}	3.14	0.821	1130.04	4.27×10^{-8}	3.16	0.807	1138.92

can be said that the highest barrier height is in Region 3.

In Fig. 7, again two distinct linear regions, which are LTR (80–180 K) and HTR (200–360 K), are seen in the plot of q/nkT versus $n^{-1} - 1$. ρ_2 and ρ_3 parameters obtained from the intercept point and slope of these linear regions, respectively. According to the results shown in Table II, ρ_2 in the LTR and ρ_3 in the HTR have higher values for all three regions. In other words, contrary to TE, it can be said that the barrier height in HTR is wider and larger than the barrier height in LTR for all three regions.

In Fig. 8, modified Richardson plots of Au/PVA/n-GaAs type SD are seen that are obtained by the combination of Eqs. 2 and 9. Still, two different linear regions LTR and HTR, which are at the same temperature range with previous plots, were achieved for all three regions.^{1,8,9}

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\phi}{kT} \quad (12)$$

Experimental Richardson constants were calculated from the intercept points for the constant diode area (0.00785 cm^2), Φ_{ap} values were calculated from slopes of the linear regions, for both three regions. The theoretical Richardson constant for n-GaAs is known to be $8.16 \text{ A/cm}^2\text{K}^2$,²¹ so it is clear that the A^* values in the HTR of all three regions are very close to the theoretical value.

In accordance with all these obtained results, it can be said that the homogeneity of the barrier height and potential change, especially at low temperatures, significantly affects the forward bias I - V characteristics. In addition, it has been successfully shown that the possible CMs of Au/PVA/n-GaAs type SD can be successfully explained on the basis of the TE by DGD due to barrier inhomogeneity. Lastly, the results of two different studies selected in the literature were compared with the results of this study. One of the samples is Au/n-GaAs MS type SD,³⁷ the other is Au/Zn-doped PVA/n-GaAs MPS type SD.⁹ Similarly, temperature-dependent CMs of these studies are also explained by DGD in the TE Base. The results of this comparison show us that in MS or MPS type SDs, especially at low temperatures, CMs are highly affected by barrier inhomogeneities.

CONCLUSION

To interpret the possible CMs of Au/PVA/n-GaAs type SD in detail, I - V measurements were carried out over the temperature range of 80–360 K. Three separate linear regions with different slopes from forward bias I - V measurements were assigned. These regions are R1 is in the range of 0.22–0.60 V, R2 is in the range of 0.64–0.90 V and R3 is in the range of 1.1–1.5 V. Basic diode parameters such as I_0 , n , and Φ_{B0} were calculated for all three

Fig. 3. Temperature-dependent n and Φ_{B0} values of Au/PVA/n-GaAs; (a) Region I, (b) Region II and (c) Region III.

Fig. 4. nkT/q versus kT/q plots of Au/PVA/n-GaAs; (a) Region I, (b) Region II and (c) Region III.

Fig. 5. n versus Φ_{B0} plots of Au/PVA/n-GaAs; (a) Region I, (b) Region II and (c) Region III.

Fig. 6. $q/2kT$ versus Φ_{B0} plots of Au/PVA/n-GaAs; (a) Region I, (b) Region II and (c) Region III.

Table II. Experimental σ_o , ρ_2 , ρ_3 and A^* values of Au/PVA/n-GaAs for LTR and HTR for all regions

	Region 1 (low bias)				Region 2 (moderate bias)				Region 3 (high bias)			
	σ_o (V)	ρ_2	ρ_3	A^* (A/cm ² K ²)	σ_o (V)	ρ_2	ρ_3	A^* (A/cm ² K ²)	σ_o (V)	ρ_2	ρ_3	A^* (A/cm ² K ²)
LTR	0.074	0.823	0.0017	6.23	0.074	0.84	0.0016	7.77	0.077	0.781	0.002	7.07
HTR	0.16	0.661	0.0071	8.13	0.168	0.533	0.011	8.14	0.171	0.463	0.013	8.13

 Fig. 7. $q/2kT$ versus $n^{-1} - 1$ plots of Au/PVA/n-GaAs; (a) Region I, (b) Region II and (c) Region III.

Fig. 8. The modified Richardson plots of Au/PVA/n-GaAs; (a) Region I, (b) Region II and (c) Region III.

regions. As a result, it was observed that the values of n and Φ_{B0} obtained in all three regions are strongly dependent on temperature and voltage. In contradiction with TE, it was observed that n values decreased and Φ_{B0} values increased with increasing temperature in all three regions. It was concluded that the FE mechanism is effective at low temperatures since theoretically and experimentally calculated E_o values are more than kT/q . In order to get more information about possible CMs of Au/PVA/n-GaAs, n versus Φ_{B0} , $q/2kT$ versus Φ_{B0} , $q/2kT$ versus $(n^{-1} - 1)$ and modified Richardson plots were investigated for both three regions. In each plot, there are two different linear regions, LTR (80–180 K) and HTR (200–360 K). These results were attributed to the dominance of DGD especially at low temperatures due to barrier inhomogeneities. In addition, the experimental Richardson constant from the

modified Richardson curve was calculated for each region. In HTRs of Region 1, Region 2 and Region 3, experimental Richardson constants were obtained very close to the theoretical Richardson constant (8.16 A/cm²K² for n-GaAs) as 8.13, 8.14 and 8.16 A/cm²K², respectively. It has been clearly indicated that the I - V characteristics of Au/PVA/n-GaAs type SD can be explained by DGD, together with quantum mechanical tunnelling CMs at low temperatures, based on TE with the fact that one or more than one CMs can be active at the same time.

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CONFLICT OF INTEREST

None.

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