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# Cryogenic Materials and Circuit Integration for Quantum Computers

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Over the last decade, quantum computing has experienced significant changes and captured worldwide attention. In particular, superconducting qubits have become the leading candidates for scalable quantum computers, and a number of cryogenic materials have scientifically demonstrated their potential uses in constructing qubit chips. However, because of insufficient coherence time, establishing a robust and scalable quantum platform is still a long-term goal. Another consideration is the control circuits essential to initializing, operating and measuring the qubits. To keep noise low, control circuits in close proximity to the qubits require superior reliability in the cryogenic environment. The realization of the quantum advantage demands qubits with appropriate circuitry designs to maintain long coherence times and entanglement. In this work, we briefly summarize the current status of cryogenic materials for qubits and discuss typical cryogenic circuitry designs and integration techniques for qubit chips. In the end, we provide an assessment of the prospects of quantum computers and some other promising cryogenic materials.

**Key words:** Cryogenic materials, qubits, quchip, quantum processing unit, quantum computer

## INTRODUCTION

To date, progress in conventional computing has relied heavily on the density of transistors on silicon chips doubling every 18 months, a trend known as Moore's law after Intel cofounder, Gordon Moore, who predicted the phenomenon in 1960s. But spiraling costs and falling yields associated with further miniaturization have stimulated the search for sophisticated alternative structures and new

materials. One possibility is to apply new concepts and new physics to the current technologies, as schematically shown in Fig. 1. Quantum computing (QC) is one of the most revolutionary computing models, in which information is stored and processed more efficiently using switches—known as quantum bits, or "qubits"—that can be on and off at the same time. The full applications of QC are expected to produce globally revolutionary and profound changes in computation. At present, QC draws huge investments from both nations and industries, as well as intensive studies from academic communities. A complete ecological environment for QC research and development (R&D) is

gradually being established. Although QC has made rapid progress in the past decade, there are still many unresolved problems. For example, as the number of qubits increases, crosstalk and fan-out issues tend to degrade the performance of the quantum processor. To be effective, QC eventually will require a noise level low enough to allow error correction to be performed, which demands improvements over the current state of both qubit design and external circuitry.

With the rapid development and breakthroughs being made in recent years, many industry giants (e.g., Google, IBM) and startup companies (e.g., Rigetti, OriginQ) have poured increasing resources and efforts to compete in this race. To date, some machines, such as educational quantum instruments and noisy intermediate-scale quantum (NISQ) devices, have been manufactured for commercial applications. However, the large-scale and error-corrected quantum computers, which would be capable of performing useful quantum algorithms, still require long-term effort. Over the last twenty years, scientists have found that cryogenic quantum materials and cryogenic circuit designs are both important for the future of QC. Moreover, the focus in upscaling qubits has gradually shifted from fundamental physics to engineering problems.

There are quite a few candidate materials for qubits, each of which has its own pros and cons. Spin in semiconducting quantum dots (QDs),[1] phase in superconducting circuits,[2] and non-commutative exchange in non-Abelian anyons[3] offer promising degrees of freedom for realizing solid-state qubits. In the pursuit of upscaling, many important developments have been reported in superconducting qubits, thus it is generally thought that superconducting implementations are currently ahead of all other qubit implementations. In 2019, quantum supremacy was demonstrated[4] in a circuit of 53 working superconducting qubits with 86 couplers, and the largest qubit number announced by Google is 72.[5] Recently, materials with distinct band structures, two-dimensional (2D) natures and topological properties have attracted considerable attention. Apart from the ongoing development of spin qubits in silicon, graphene is expected to be a robust material for hosting spin qubits, owing to its weak spin-orbit and hyperfine interactions. Charge carriers in few-layer transition metal dichalcogenides (TMDCs) are simultaneously valley- and spin-polarized, providing more degrees of freedom that can be controlled as qubits.[6] Topological materials, such as 2D/3D topological insulators (TIs), Dirac semimetals and Weyl semimetals, for their topologically protected edge and surface states, are immune from defect scatterings and thus can transmit current effectively.[7,8] When topological materials are in contact with s-wave superconductors, it is possible to host a type of quasiparticles called Majorana bound states (MBSs).[9] These quasiparticles obey non-Abelian (non-commutative)
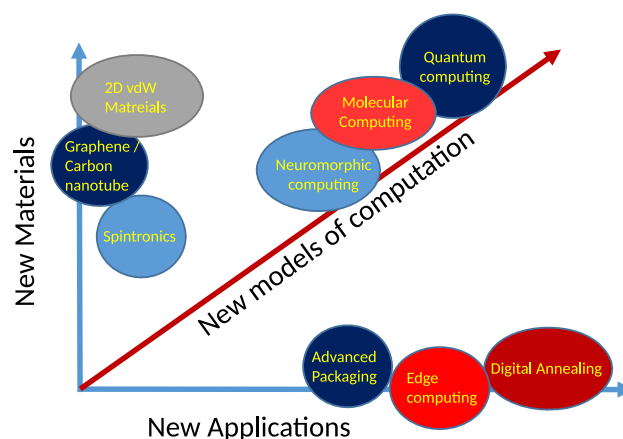


Fig. 1. The strategies beyond Moore's law. New applications with current technology, new materials in replacement of semiconductors and new computation models introduced in industry.

exchange statistics and are candidates to perform fault-tolerant topological quantum computing (TQC). Although lots of effort needs to be made before practical QC applications are possible, these aforementioned materials are under heavy investigation for use in many different QC platforms, such as QDs and superconducting circuits.

On the other hand, external circuitry design is as important as pursuing high-quality qubits, since QC relies on both qubits and well-established control means to communicate with them. Solid-state qubits (e.g., QDs and superconducting circuits) generally operate in the 10mK environment inside a dilution refrigerator, with high electron mobility transistor (HEMT) amplifiers thermally anchored at 4K, and control electronic devices placed at room temperature. In practice, it is hard to thermally isolate the qubits from the measurement elements, thus noise cannot be completely avoided, inevitably introducing decoherence of the qubits. To address this issue, a cryogenic control chip based on a complementary metal-oxide-semiconductor (CMOS) ($<$ 10K) has been used to prevent the thermal noise caused by room temperature. This highly-integrated system-on-a-chip (SoC) will simplify system design and replace the original bulky room temperature instruments. For example, Google Bristlecone has used an integrated circuit (IC) of a pulse generator in a 4K environment to directly control low-temperature qubits.[5]

In this article, we will discuss the new opportunities for cryogenic materials and cryogenic circuitry designs for quantum computers. In particular, we will briefly review the current status of quantum materials and circuit integration for quantum computers.

## QUANTUM MATERIALS FOR QUBITS

Many QC platforms have been investigated and developed. QC platforms can be classified into atomic systems, photonic systems, NMR systems

and solid-state systems. For solid-state systems, superconducting quantum devices, semiconductor QDs and topological materials are very important platforms that are under heavy investigation. We will focus on solid-state platforms which work in the microwave regime, and discuss the opportunities for new materials.

## Superconducting Qubits

Superconductivity happens when certain materials are cooled below a critical temperature $T_c$ and electrons form pairwise (Cooper pair) condensate, switching from fermions to bosons. A wavefunction exists in macroscopic scale and governs quantities such as charge density and phase in a quantum flux across the entire superconductor. A Josephson junction (JJ) is formed by two superconductors separated by an insulating layer, with a typical thickness of 1 nm. When a superconducting loop is interrupted with a JJ, the phase difference $\phi$ across the JJ and the number of extra charges $n$ stored in the capacitance of the JJ obey the commutation law $[\phi, n] = i$. This second quantization enables the loop to be an artificial atom, thus a qubit. Superconducting quantum integrated circuits[10] usually consist of JJs, capacitors and inductors. Common IC fabrication processes like optical/electron-beam lithography and thin film deposition are used to pattern these circuit elements on a silicon substrate. The popular superconducting materials are aluminum ($T_c = 1.2$ K) and niobium ($T_c = 9.3$ K). Moreover, the JJ's nonlinear inductance creates an anharmonic structure with unequal energy levels, thus making the superconducting quantum circuit a good candidate for physical qubits. Superconducting qubits usually operate in frequencies around 5 GHz, which is equivalent to $\sim 250$ mK in temperature. Superconducting quantum circuits are put in dilution refrigerators of 15 mK to reduce thermal noise.

There are various designs of JJ-based superconducting qubits.[11] A very popular qubit, called transmon, as shown in Fig. 2, is formed by a JJ SQUID loop shunted by a large capacitor with edge size of $\sim 200\,\mu$m. The transmon Hamiltonian can be given as $\widehat{H} = 4E_C(\hat{n} - n_g)^2 - E_J \cos \hat{\phi}$ where $\hat{n}$ is the number of charges across the total capacitance, $n_g$ is the effective offset charge controlled by $U(t)$, and $\phi$ is the phase difference across the JJ.[12] $E_C$ and $E_J$ denote single electron charging energy and the JJ's coupling energy, respectively. The qubit's transition frequency $\omega_{01} = \sqrt{8E_C E_J}/\hbar$ from the ground state $|0\rangle$ to excited state $|1\rangle$ is typically several GHz. $E_J$ can be controlled by applying an external magnetic flux $\Phi_{\text{ext}}$ through the SQUID loop, thus making $\omega_{01}$ tunable. The large shunt capacitor $C_s$ reduces $E_C$, thus minimizing the noise from spurious charge fluctuations. The $\cos \phi$ term introduces an anharmonicity necessary for assuring that energy states are not equally spaced. The anharmonicity is defined as $\omega_{12} - \omega_{01}$, which is about $-200$ MHz.

Coherence time of a qubit is evaluated by relaxation time $T_1$ and dephasing time $T_2$. To measure $T_1$, a Pauli-x operator is applied to excite a qubit to state $|1\rangle$ and read it afterwards. This process is repeated with different time periods.[13] The relaxation time $T_1$ is then estimated by the equation $S(t) = S(0)\exp(t/T_1)$ (Fig. 3a). Dephasing can be easily influenced by noise from control and readout operations, so the measured dephasing time $T_2^*$ is usually smaller than $T_2$. Additionally, the period of the Rabi oscillation signal can determine the $\pi$-pulse precisely for correcting phase errors, as well as calibrating the quantum gates (Fig. 3b).

## Semiconducting Qubits

A semiconducting QD is an artificially structured system that can be filled with only a few electrons or holes. The charged carriers in this system are generally confined in a submicron area, and the confinement potential in all directions is strong enough that results in quantized energy levels. These energy levels can be observed at low temperatures. The electronic properties of QDs are dominated by several effects.[1] First, the Coulomb repulsion between electrons on the dot leads to an energy cost called charging energy $E_C = e^2/C$, where $C$ is the total capacitance of the dot, for
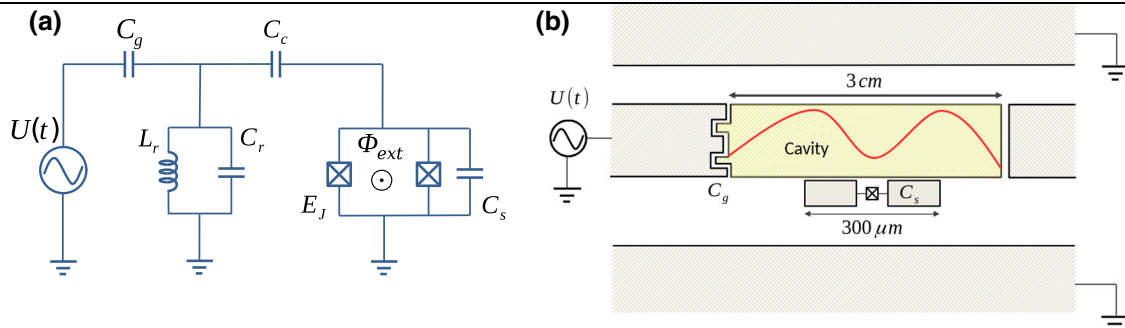


Fig. 2. (a) Circuit diagram of an external-flux tunable transmon qubit and (b) schematic of its physical layout. It is connected via coupling capacitance $C_c$ to the cavity formed by $C_r$ and $L_r$. Signal $U(t)$, coupled by $C_g$, drives the cavity around the resonant frequency of $\sqrt{1/L_r C_r}$. A transmon placed very closely to a cavity forms a capacitance coupling $C_c$.
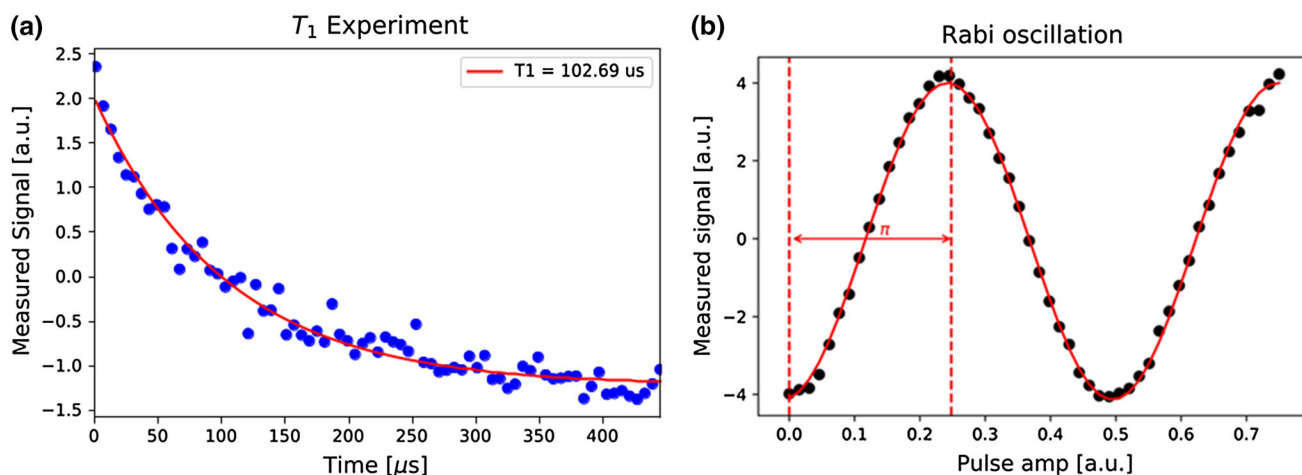
Fig. 3. (a) Spin-relaxation diagram of a single qubit. The exponential decay of the $|1\rangle$ density is the signature of decoherence (credit: IBM Q hub at NTU). (b) Using a Rabi experiment to calibrate the $\pi$-pulse, which is also known as a Pauli-x gate, and can invert the population from $|0\rangle$ to $|1\rangle$. Assuming that $|0\rangle$ is the initial state of our system, a well-calibrated $\pi$-pause can create $|1\rangle$ with good fidelity (credit: IBM Q hub at NTU).
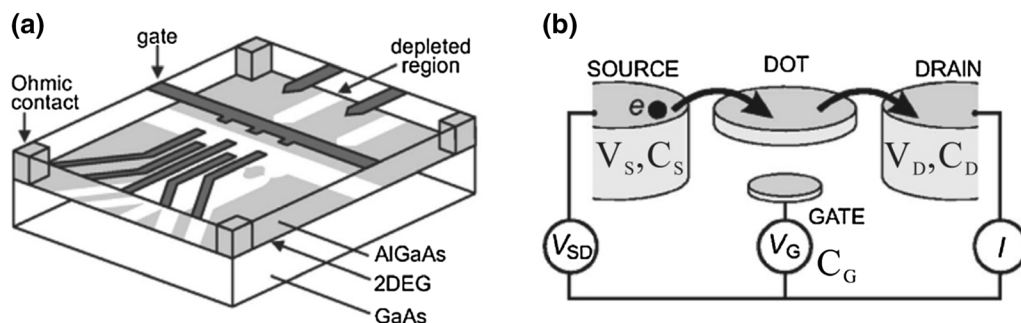


Fig. 4. (a) Schematic view of a lateral QD device defined by metal surface electrodes on a GaAs/AlGaAs 2DEG system. (b) Electrical network diagram of a single QD. Adapted with permission from Ref. 1.

adding an extra electron to the dot. Because of this charging energy, the tunneling of electrons to the reservoirs can be suppressed at low temperatures (when $E_C > k_B T$), which leads to a phenomenon called Coulomb blockade. Second, the tunnel barrier resistance $R_t$, which describes the coupling of the dot to both the source and drain reservoirs, has to be sufficiently opaque such that the electrons are located either in the source, in the drain, or on the dot. In two-dimensional electron gas (2DEG) systems, the dot is defined by a gate-depleted area (Fig. 4a) and is tunnel-coupled to the reservoir on each side, as indicated by a schematic model shown in Fig. 4b. Thus, varying the voltages on the surface gates enables several important parameters, such as the number of electrons and the tunnel barrier resistance, to be finely tuned. Qubits based on semiconducting QDs have several forms but mainly utilize the spin properties of electronic states confined in the dots. For example, spin-up and spin-down states in a single QD, two-electron singlet and triplet states in a double QD and spin-exchange interaction in a triple QD are all candidates for use in quantum information processing.[1,14] In

isotopically purified $^{28}$Si QDs, where nuclear spin is greatly reduced compared to GaAs-based QDs, the dephasing time $T_2^*$ can approach 120 $\mu$s[15] with a gate operation time around 100 ns.[16] The single qubit gate fidelity in this system can surpass 99.9% while the two-qubit gate fidelity exceeds 98%.[17,18]

While development of superconducting and semiconducting qubits based on the aforementioned composing materials continue to advance, quantum materials, for their distinct band structures and topological properties, have also attracted substantial attentions for opportunity in synthesizing new type of qubits, as will be discussed in the next section.

## Novel Materials for Qubits

Owing to weak spin-orbit and hyperfine interactions, graphene is expected to be a robust material to preserve spin properties and therefore ideal for making spin qubits. Attempts to confine and manipulate single charges in graphene quantum dots (GQDs) have been widely studied since 2008,[19] when a series of GQDs fabricated on $SiO_2$ substrate
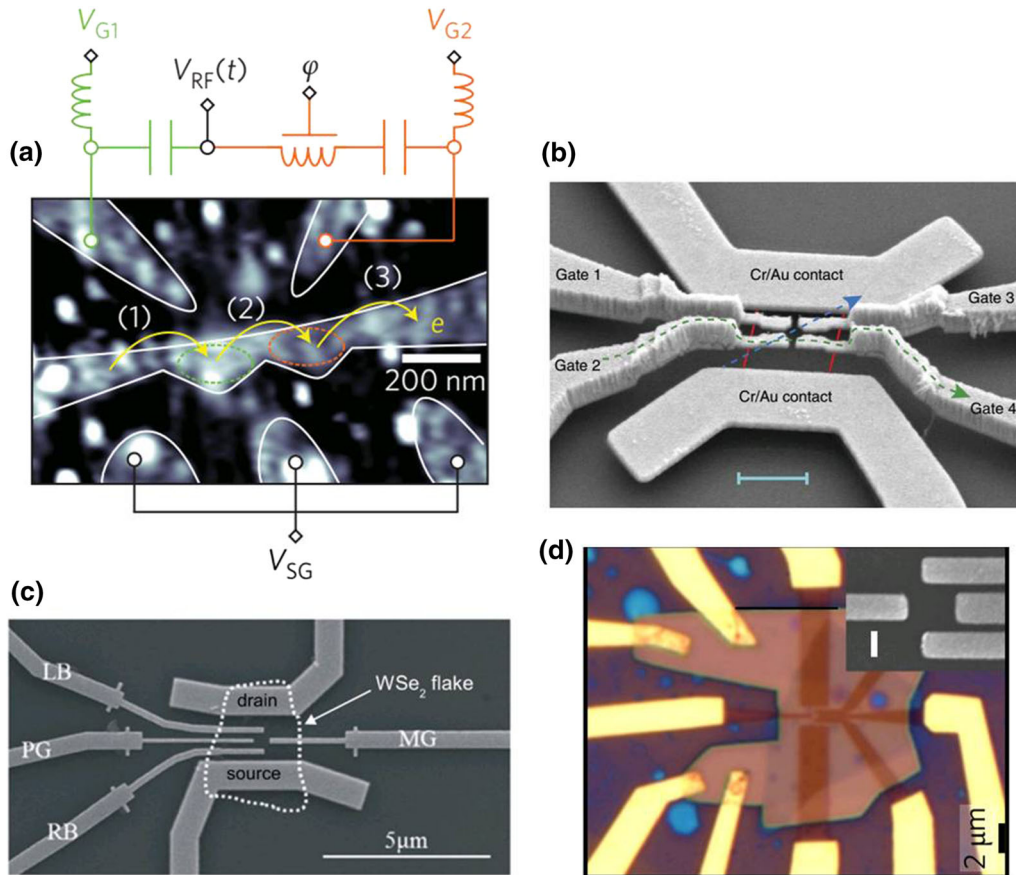
Fig. 5. Novel candidate materials for QD qubits. (a) Single electron transport in GQDs on $SiO_2$ substrate. (b) Gate-defined QDs in suspended bilayer graphene. The scale bar is 1 $\mu$m. (c) A 2H-phase $WSe_2$ QD device on $SiO_2$ substrate. The $WSe_2$ flake (4.5 nm in thickness) is highlighted by the white dotted line. (d) 2H-phase $MoS_2$ QD encapsulated by hBN device with graphene contacts. (a, b, c, d) Adapted with permission from Ref. 22,32–34 respectively.

was reported (Fig. 5a).[6,20] However, early studies of GQDs on $SiO_2$ have indicated an absence of spin-related phenomena, such as spin blockade and the Kondo effect. In order to reduce substrate disorder, which is one of the major sources of fast spin relaxation, subsequent efforts have been focused on GQDs on inherently flat substrates, e.g., hexagonal boron nitride (hBN),[21] electrically gated suspended bilayer graphene (Fig. 5b)[22] and electrically gated bilayer graphene on hBN.[23] Although spin relaxation time has been extracted from spin injection measurements in monolayer graphene flakes,[24] it has not been reported in the aforementioned GQD systems. The possible causes can be resonant scattering of electrons off magnetic moments and interplay between the spin and pseudospin quantum degrees of freedom.[6] On the other hand, the ballistic nature of Dirac fermions in graphene provides a good weak link to transmit supercurrent efficiently in its JJs.[25] Because of graphene's 2D and gatable nature, which allows the critical current and qubit energy to be tuned by gate, several gate-tunable transmons (gatemons) made of graphene JJs have been recently reported (Fig. 6a).[26,27] The first coherent control of such a qubit shows Rabi

oscillation, and qubit relaxation time $T_1$ and dephasing time $T_2^*$ at the scale of 36ns and 51ns, respectively.[27] Gatemons based on other semiconducting materials emerged as a branch in superconducting qubit research since their first realization in InAs nanowire (Fig. 6b)[28] and subsequently in InGaAs/InAs-based 2DEG. (Fig. 6c).[29] The corresponding relaxation and dephasing times are $T_1 \sim 0.8\,\mu$s and $T_2^* \sim 1\,\mu$s in the former and $T_1 \sim 1\,\mu$s and $T_2^* \sim 2\,\mu$s in the latter. Although the qubit's performances are relatively low compared to the state-of-the-art flux-tunable transmons,[30] it provides a platform for more materials to be integrated with, and opportunity for exploring novel material-based superconducting qubits.[31]

Although the relatively weak spin-orbit interaction in graphene is advantageous for preserving spin coherence, it also implies relatively slow operation of graphene-based spin qubits.[35] In addition, the small band gaps in monolayer and bilayer graphene also present more challenges to confining particles in GQD devices. Alternatively, 2D semiconductors, such as 2H-transition metal dichalcogenides (TMDCs), exhibit direct band gap in monolayer and broken inversion symmetry in an
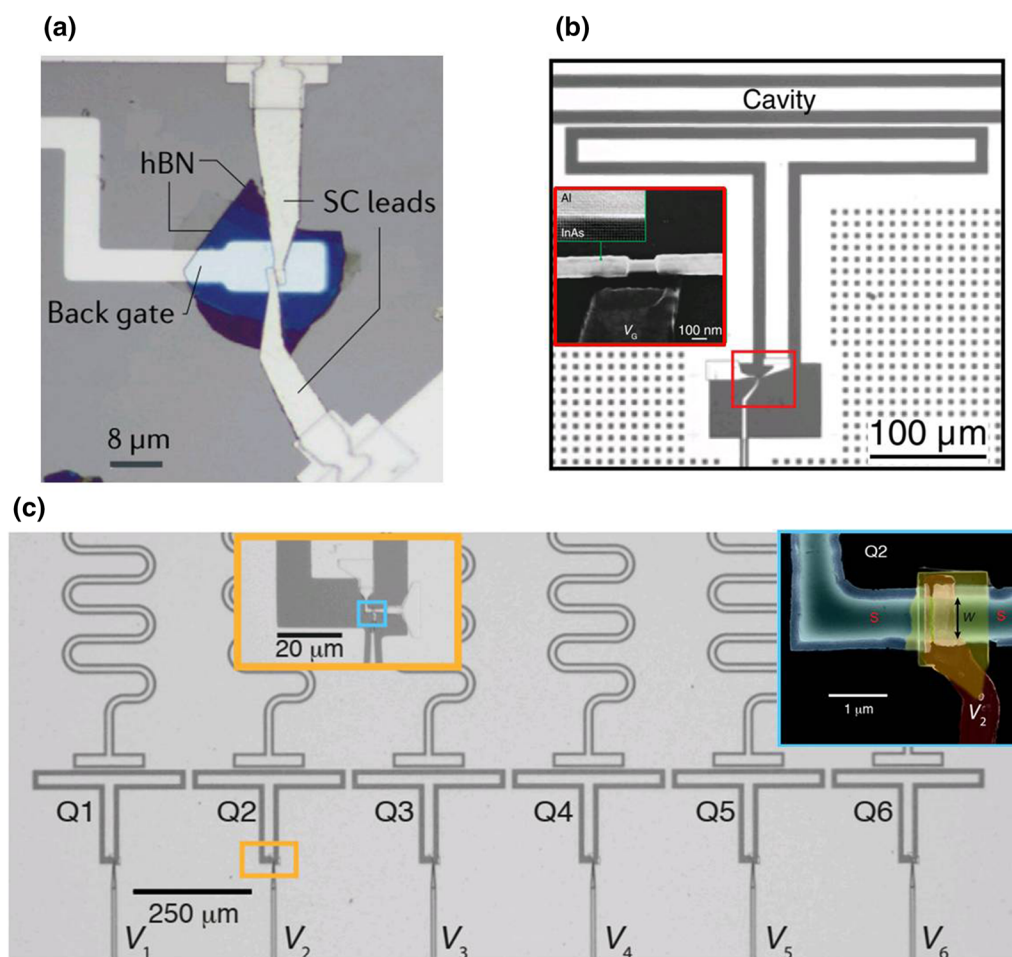
Fig. 6. Candidates for materials-based superconducting qubits. (a) Graphene-based gate-tunable qubit (gatemon) consisting of hBN encapsulated graphene and Al leads. (b) InAs nanowire-based gatemon qubit. The gatemon is defined between the T-shaped island and the surrounding ground plane. The inset shows a scanning electron microscope (SEM) image of the Al-InAs-Al JJ. (c) InGaAs/InAs-based 2DEG gatemons. The right inset shows the SEM of the gate controlled 2DEG JJ of width $W$. (a, b, c) Adapted with permission from Refs. [27–29] respectively.

odd number of layers. In combination with TMDC's strong spin-orbit coupling, this allows the charge carriers to be simultaneously valley- and spin-polarized, providing more degrees of freedom that can be controlled as qubits.[36–38] The Fock–Darwin spectrums have shown that the lowest levels (Kramers pairs) in TMDC QDs are simultaneously spin-and valley-polarized[6] and can in principle serve as valley or spin qubits, in which the former can be manipulated by electron spin resonance while the later can be controlled with an AC electric field without affecting the spin.[35] The physical realization of TMDC-based QDs often suffers from the high Schottky barriers existing in metal/TMDC interfaces, which leads to high contact resistance at low temperature. While a series of experiments has demonstrated successful quantum confinement and single electron transport in both 2H-TMDC single QDs and double QDs (Fig. 5c and d),[34,39–41] studies on spin or valley properties of single-particle states remain unreported in these systems.

Majorana fermions (MFs) or Majorana bound states (MBSs) are a special type of excitation in condensed matter systems which obey non-Abelian (non-commutative) exchange statistics, i.e., particle exchange with different routes will lead to different end states (Fig. 7a).[42–44] By braiding a few MFs, bits of information can be encoded (final state is dependent only on the topology of the braids and not on the specific geometry), forming the scheme of TQC.[45,46] Because the qubit operations are protected by topological symmetry, MFs are expected to have a very long coherence time and very high gate fidelity, which is generally referred to as quantum error correction at the hardware level.[43,47] With the help of theoretical predictions,[46] the signature of MFs has been experimentally observed in several solid state systems, such as in 1D magnetic atoms on an s-wave superconductor,[48] in s-wave superconductor proximatized topological insulators (TIs),[49,50] in quantum anomalous Hall insulators,[51] and in semiconducting nanowire with a large g-factor and strong spin-orbit coupling.[52–55]
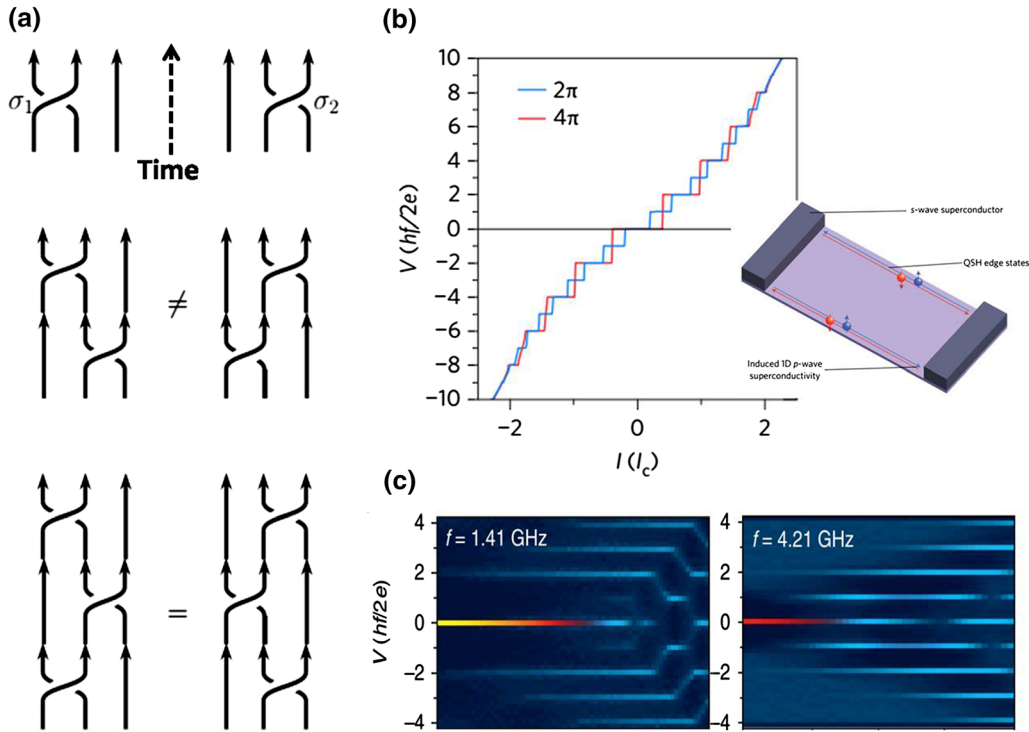
Fig. 7. Majorana bound states for TQC. (a) Illustration of braiding. Top: The two elementary braid operations $\sigma_1$ and $\sigma_2$ on three particles. Middle: Braiding showing $\sigma_2\sigma_1 \neq \sigma_1\sigma_2$ hence the braid group is non-Abelian. Bottom: The braid relation $\sigma_i\sigma_{i+1}\sigma_i = \sigma_{i+1}\sigma_i\sigma_{i+1}$. (b) Shapiro steps for $2\pi$- and $4\pi$-periodic supercurrent. Inset shows a topological JJ consisting of 2D TI and superconductor, for hosting $4\pi$-periodic supercurrent. (c) Experimentally measured Shapiro steps as a function of RF power at frequency 1.41 GHz and 4.21 GHz in a topological JJ made of Dirac semimetal $Bi_{1-x}Sb_x$. In both cases, the missing $n = 1$ steps are present. (a, b, c) Adapted with permission from Refs. 46, 56, and 57 respectively.

Topological materials, such as topological insulators, Dirac semimetals and Weyl semimetals, for their topologically protected edge and surface states,[7,8] are also promising candidates for use in materials-based QC devices. In 2008, Fu and Kane predicted that in a hybrid system consisting of 2D TI edge states and an s-wave superconductor, the Andreev Bound states (ABS) result in an exotic $4\pi$-periodic supercurrent, which serves as an indication of the existence of MBS.[58] However, such a non-trivial phenomenon cannot be directly observed in DC measurement, because in a time scale of $\mu$s the occupation of ABS tends to couple with the continuum of superconductors, resulting in an averaged trivial $2\pi$-periodic supercurrent.[9] An alternative way to circumvent this issue is to exploit the AC Josephson effect, in which a JJ would respond to an applied AC bias and develop a series of voltage steps with step height proportional to AC frequency, a phenomenon known as Shapiro steps (Fig. 7b). Experimentally, for a pure $4\pi$-periodic supercurrent, only even Shapiro steps should be present and the suppression of the $n = 1$ step is usually more pronounced than other steps.[59,60] In fact, not only the missing $n = 1$ steps have been observed in 2D TI system,[56,61] they also have been observed in other topological JJs consisting of topological materials with helical bulk and edge states (Fig. 7c).[57,59] The Td-phase of TMDC family provides many distinct topological natures for material scientists to explore for MBS-related properties.[62] For example, monolayer $1T' - WTe_2$ is a natural 2D TI[63,64] and revealed a superconductivity upon electrical gating.[65] It serves as an opportunity to engineer all gate-control topological junction in one single flake. On the other hand, bulk $WTe_2$ and $MoTe_2$ are type-II Weyl semimetal,[66,67] as identified by their surface Fermi arc state in Angle-resolved photoemission spectroscopy (ARPES)[68,69] and non-saturating magnetoresistance in transport.[70,71] The $4\pi$-periodic supercurrent has not been studied in the topological junctions made of these aforementioned materials. Dirac semimetals, such as $Cd_3As_2$ and $Bi_{1-x}Sb_x$, have been studied for the missing $n = 1$ Shapiro steps as a signature of MBS, as mentioned previously.[57,59] While the search for signatures of MBS is still ongoing, the ultimate goal is to exchange these quasiparticles and confirm their non-Abelian statistics. There are several ways for realizing exchange of MFs, including the T-junction geometry in nanowire systems[72,73] and moving vortex by tips in 3D TI/superconductor systems.[49,74] The 2D and gate-controllable TI phase in $1T' - WTe_2$ may

provide an easier way to design exchange geometry by electrical gating, thus simplifying the fabrication and exchange processes.

## QUBIT OPERATIONS AND CIRCUITRY

Universal quantum computations are realized by virtue of qubit operations which are closely related to the quantum coherence. Scientists are trying to fabricate new types of qubits for obtaining much longer coherence time, easier controllability and connection, higher designability, and better scalability. Taking superconducting qubits as an example, the coherence time has been increased in the past decade from initial nanoseconds for a charge qubit[75] to around 100 $\mu$s for a transmon qubit[76] inside a 3D cavity. Single qubit operations, implemented by resonant pulses applied through on-chip wires, have been improved from several times to now $10^5 \sim 10^6$ times within the coherence time, and the fidelities of single- and two-qubit gates can reach 99.92% and 99.4%.[77] Scientists are making efforts to further improve the coherence time such that it can be much longer than a threshold time for certain classes of fault-tolerant quantum error correction codes. However, solving the decoherence problem is not an easy task. We know that low frequency noise $(1/f)$ is a main intrinsic limitation on the coherence of superconducting qubits, and mainly results from the fluctuations of critical-current, charge, and flux, but the microscopic origin and mechanism of these fluctuations are not well understood. High frequency noise around the qubit frequency makes energy exchange between environment and superconducting qubits, and mainly contributes to energy relaxations of the qubit. It is believed that the coherence time can be extended by optimizing designs of circuits, removing impurities and defects of materials, improving fabricating

technologies of devices, and developing new methods for material engineering on the microscopic scale. Eliminations of decoherence still remain the biggest challenges in quantum circuits.

The current designs of quchips usually feature multiple qubits with different transition frequencies to avoid qubit crosstalk. For superconducting quantum circuits, the qubits on circuits can be coupled either directly by capacitance and inductance or indirectly by SQUIDs, transmission line resonator (cavity), and other means. We mention that the transmission line resonator usually consists of a long ($\sim 1$ cm)[78] winding superconducting metal wire with the surrounding grounded. If the transmission line resonator facilitates two-qubit operations as a frequency coupling agent (Fig 8), then it is usually designed with resonant frequency $\omega_{qr} = \sqrt{1/L_r C_r}$ detuned from qubit transition frequencies $\omega_{q1}$ and $\omega_{q2}$. When the transmission line resonator is coupled to flux or transmon qubits, the external flux can control their couplings by changing qubit transition frequencies. Various superconducting qubits can be coupled to either a transmission line resonator or a three-dimensional resonator, which are extensively applied to transfer microwave information or measure superconducting qubit states.

To achieve universal QC, arbitrary single-qubit logic gates and a nontrivial two-qubit logic gates are required. Not only precise control of the qubit but also switch-on or -off coupling between two qubits is a very crucial issue. The mechanism of these gates will be discussed in the following two paragraphs.

*Single-qubit gate* A single-qubit gate is performed by applying a microwave signal [frequency$\omega_d$, voltage$V_0$s(t), phase$\phi$] with energy about one microwave photon to the qubit. If the coupling capacitor $C_c$ is relatively small comparing with $C$ and $C_s$ (Fig. 2a), the Hamiltonian can be
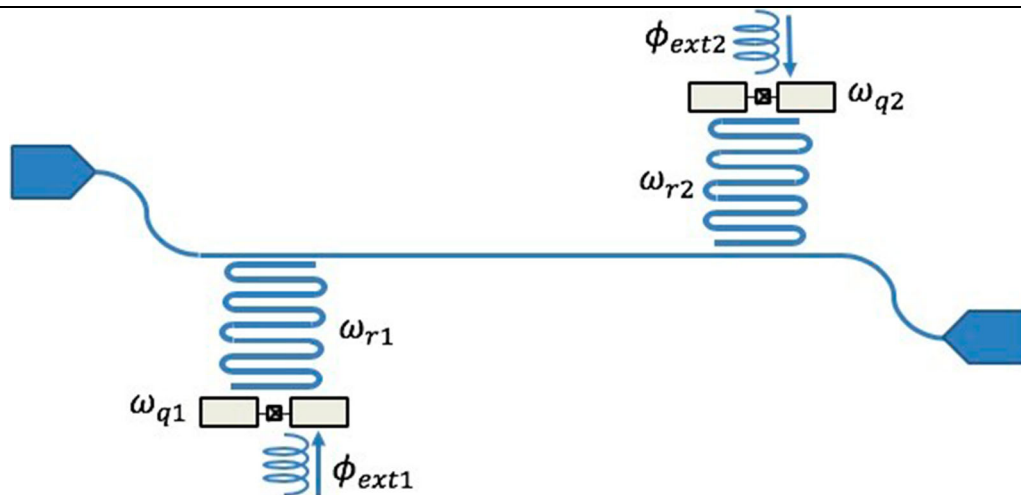


Fig. 8. General quchip architecture showing multiple qubits with frequencies tunable by external flux sources $\phi_{\text{ext}}$. Qubits resonate with and through the cavity to achieve two-qubit operation.
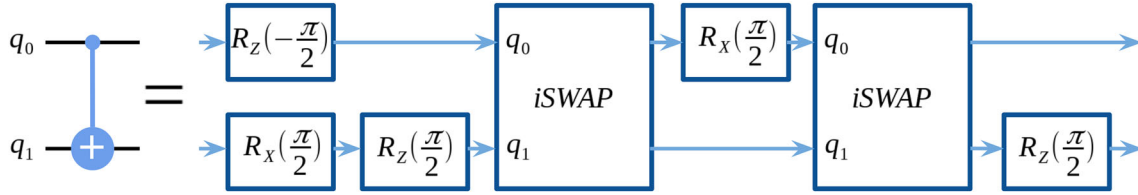
Fig. 9. Constructing a CNOT gate.

written as $H_{drive} = -\frac{1}{2}Q_d V_0 s(t)(I\sigma_x + Q\sigma_y)$. $I = \cos\phi$ and $Q = \sin\phi$ are components of rotation axis in x-y plane.[79,80] By changing signal phase $\phi$, the operation can represent different single-qubit gates. A simple example is when $\phi = 0$, the qubit can operate an x-axis $\pi$ rotation and transit from $|0\rangle$ to $|1\rangle$ with a proper signal time period. The signal profile $s(t)$ is generated by an arbitrary waveform generator (AWG), which shapes the constant-amplitude base signal $V_0$ generated by a local oscillator (LO). Driving frequency $w_d$ is the sum of frequencies from AWG and LO and is tuned to equal to $\omega_{01}$. In the current quchip design, AWG and external magnetic flux are two tunable elements forming the major scheme for addressing particular qubits in a quchip.

*Two-qubit gate* A two-qubit gate can be realized by coupling two qubits through a common cavity (Fig. 8). One possible scheme is to tune the two qubits to the same frequency $\omega_{01}$. In this case, the effective Hamiltonian representing the combined system is $H = \frac{1}{2}g(\sigma_{1x}\sigma_{2x} + \sigma_{1y}\sigma_{2y})$. The propagator $U(t) = \exp(-iHt)$ becomes an entanglement operator coupling rotations of both qubits.[2] For example, when $t = \frac{\pi}{4}g$, it defines a universal gate $\sqrt{\text{iSWAP}}$.[81] When time lapses twice as long, it becomes a iSWAP gate. A CNOT gate can be constructed with two iSWAP gates and a few single-qubit gates (Fig. 9).

In superconducting qubit circuits, experimenters have realized controlled-NOT, Controlled-Z, Controlled-R, iSWAP-like, $\sqrt{\text{iSWAP}}$ and other two-qubit gates. Currently the operation time for two-qubit is around 40 ns.[82] The switchable couplings are now realized via various techniques, e.g., large detuning, time-dependent variable controls, dressed states, sideband excitations, parametric tunable couplings, and longitudinal field modulations. These control techniques and methods still need to be optimized or improved.

The readout or measurement of superconducting qubit states is the final step for QC. There are different categorizations for measurements. If we specify measured observables, such as charge, flux and phase of the charge, flux and phase qubits, respectively, then there are three different methods to measure qubit states. The charge of a charge qubit can be detected by a single-electron transistor (SET). The current in the SET indicates the qubit states. The flux of a flux qubit can be detected by a direct current (DC) SQUID. By switching the bias current applied to the SQUID to a dissipative state, we can obtain the information of qubit states. The phase of a phase qubit is measured by using the tunneling out of the zero-voltage state of a current-biased JJ. Roughly speaking, when the bias current is below the value of the critical current of the JJ, the qubit is in the zero-voltage state. Quantum tunneling of the phase will switch the zero-voltage state to a finite-voltage state when the qubit is in excited state.

The measurements on superconducting qubits can also be categorized according to quantum mechanical interpretations, such as quantum non-demolition (QND) measurements,[2] which is different from measurements mentioned above. QND measurement is currently considered the main way to realize high-fidelity readout of qubit states. A QND measurement is usually performed using either a dispersive coupling between a qubit and a cavity field or the coupling between a qubit and a nonlinear resonator. This method can be applied to any kind of superconducting qubits that are dispersely coupled to a single-mode cavity field.

Taking QND measurement as an example, a readout operation is performed by applying a signal with frequency $\omega_{RD}$, amplitude $V_{RD}$ and duration $\tau_{RD}$ to the cavity, coupled to the qubit, with $\omega_{RD}$ properly detuned with the qubit frequency $\omega_{01}$ so that energy exchange between cavity and qubit is largely prohibited for QND measurement. The dispersive effect from the interaction of cavity and qubit will cause $\omega_{RD}$ to shift $+\chi$ or $-\chi$ depending on the readout state being $|0\rangle$ or $|1\rangle$, respectively. The phase of the superposition state can also be extracted by analyzing the dispersive signal. As shown in Fig. 10, a proper duration $\tau_{RD}$ yields a quality readout by producing sharp and distinguishable dispersive wave forms. The readout signal is fed through a frequency multiplier along with a signal from LO, then the output goes through a low-pass filter and results in a much lower intermediate frequency $\omega_{IF} = \omega_{RD} - \omega_{LO}$. The $\omega_{IF}$ is designed such that it is common to all qubit readings, thus made convenient for further processing. It is further amplified by parametric amplifier (PA) to enhance S/N ratio.[83] The final signal is then digitized by analog-to-digital converter (ADC) for data processing at room temperature.
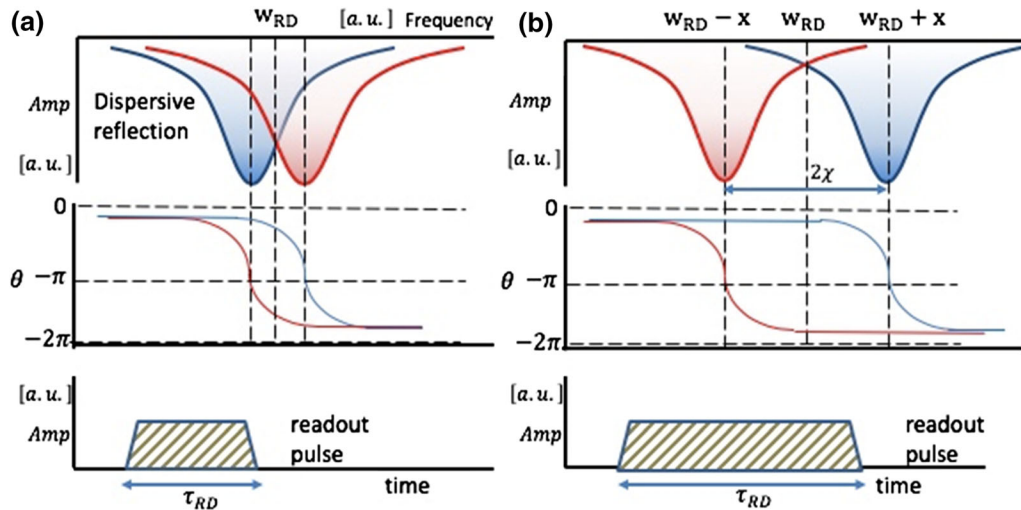
Fig. 10. Dispersive readout signal with frequency $\omega_{RD}$, amplitude $V_{RD}$ and duration $\tau_{RD}$, (a) readout signal without proper time length shows an unclear readout, and (b) a successful readout by reaching dispersive frequency $2\chi$.

The executions of quantum algorithms rely heavily on extracting characteristics of each single-qubit and two-qubit operations. Given a quchip of $N$ qubits, there are at least $p_q \times q + p_c \times c$ parameters needed for the peripheral circuits to be accurately calibrated for generating control and readout signals. $p_q$ and $p_c$ are numbers of parameters of a single-qubit and two-qubit operation, respectively, and $q$ is the number of qubits and $c$ is the connectivity. There are hundreds of parameters for near term quantum computers with about 100 qubits. This task is not only laborious, but also mixed with trade-offs, consisting of circular sequences of pulse-measure-analyze. In current practice, quantum computers are calibrated frequently due to sensitivity to environmental changes.

## QUCHIP SCALE-UP AND 3D INTEGRATION FOR QPU

With numbers of qubits growing from 10's to 100's and even up to millions, problems that CPUs and GPUs have encountered in scale-up will also appear in designs of quantum processing units (QPUs). A QPU consists of multiple quchips, where each quchip is a monolithic substrate with qubit circuitry patterned on one or both surfaces. Problems encountered in designing a quchip can be roughly categorized as (1) qubit accessibility and qubit-qubit connectivity, and (2) control signals and noise management. A common superconducting quchip usually consists of the following key elements: tunable qubits, microwave cavities, DC bias lines and microwave buses. It is desired that every qubit can be individually addressed and can be connected to or isolated from any other qubit. With qubits and cavities getting gradually crowded in a quchip, electromagnetic interferences between conducting geometries have to be well managed to avoid crosstalk. A wide variety of noise modes generated by quasiparticles from material defects are also a major consideration for large quchip designs.

Recent progress in the area of cryogenic CMOS device physics and circuit design have proposed to move analog signal processing functions from room temperature to 4 K. This will benefit all physical qubits requiring cryogenic temperature. The number of waveguides attaching to a single quchip is getting unmanageable as a bottleneck for scale-up and noise management. The ultimate goal is to move all waveguides to room temperature. In Feb 2020, Intel and QuTech announced the co-developed Horse Ridge, a chip fabricated with Intel's 22nm FFL (FinFET Low power) CMOS process for qubit control.[84] This chip is composed mainly of a digital core, an SRAM, and an analog and RF circuit. The RF line frequency is between 2 GHz and 20 GHz, while the mainstream superconductor qubit frequency is between 4 to 7 GHz, which means that Horse Ridge is suitable for beyond superconducting qubits and it should be a universal cryogenic interface between qubits and data acquisition systems. The chip has a total of 4 RF channels and uses frequency division multiple access (FDMA). Each channel can control 32 qubits and a total of 128 qubits. The information that controls the RF waveform is stored in SRAM, which can be processed quickly with reference to a look up table. The device physics model at 4 K is different from current mainstream CMOS physics and design. However, Horse Ridge proves that the CMOS IC fabrication can be leveraged in the QC domain. We foresee that complicated calibration procedures can be stored in and carried out by a small to medium size memory and CPU. More research resources will pour into this area, paralleled with 3D QPU integration.
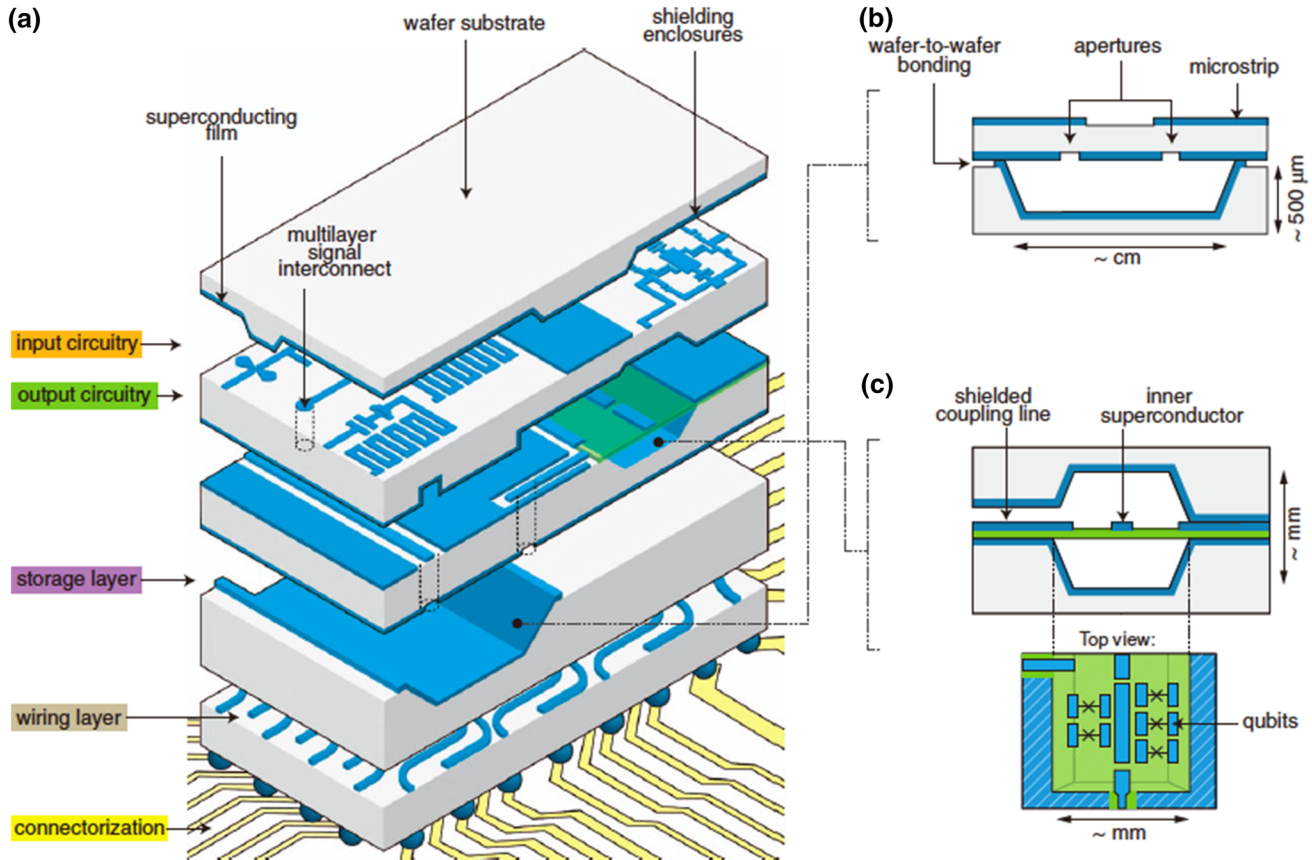
Fig. 11. A conceptual 3D integration of QPU, (a) on the top, the input and output driving circuitry, in the middle layer, microchip with qubits and transmission lines, and at the bottom two layers, cavities and wirings. (b) shows qubits and interface lines in a shielded space. (c) shows that transmission line cavities are well shielded. Adapted with permission from Ref. 87.

Here, some problems and solutions for scaling up superconductor-based quchip and QPU are reviewed.

## Geometric Considerations

A common transmon with a large shunt capacitor usually spans about 200 $\mu$m in size. A $\lambda/4$ cavity is usually scaled about 1cm in length. With this large different in physical scale, a coplanar cavity is usually patterned as a highly winding superconducting metal line occupying an area with a reasonable aspect ratio. Since a large percentage of quchip area is occupied by cavities, the ground plane is divided into complicate geometries, which can be a source of noise. Air bridges over cavities are proposed to connect both sides of ground planes to improve the distribution of current density.[83,85] Air bridges also facilitate two cavities crossing each other and provide a geometric flexibility for quchip layout.[85] One disadvantage of coplanar cavities is that more than 80% of electrical field travels through the dissipative silicon substrate resulting in energy loss. Comparing with cylindrical 3D cavities, the resonance lifetime is about one magnitude of order shorter. William O'Brien and the other co-workers proposed a superconducting ground

plane on top of quchip/cavity plane with a gap of few microns. In this design, dissipation by the silicon is reduced to less than 50%.[86] Teresa Brecht and the other co-workers proposed a full superconducting ground enclosure and suspended qubit/cavity substrates with low dielectric constant so as to mimic 3D cavity designs (Fig. 11).[87]

## Frequency Management

Executing a gate model algorithm involves a timely multiple stream of signals. A common band of a few GHz is usually divided into many sub-bands with enough side-band gaps for avoiding inferences among neighboring qubits/cavities. Qubits and cavities are geometrically designed to operate in different frequencies. A cavity is usually designed to properly detune with coupled qubits for readout operations. Frequency assignments are driven by two criteria: (1) Geometrically adjacent qubits/cavities should operate in different frequencies to avoid crosstalk and unwanted excitations, and (2) Frequencies of qubits coupling to the same cavity should operate within a tunable band so that one qubit can be tuned to interact with another during two-qubit operations. In some designs, cavities are made tunable, too, with a SQUID circuit for more

flexible bandwidth management. The FDMA scheme is employed to manage simultaneous operations of qubits attached to the same driving line. In order to fully utilize limited quchip I/O points, several cavities may capacitively couple with a microwave driving bus. Readout and control signals can address one or more qubits with the FDMA scheme.

### Control Sequence Management

During execution of a quantum algorithm, each operation requires a varying time duration. Execution following logical sequence defined by algorithms can result in poor utilization of qubit resources. Many solutions have been proposed to solve this problem with software approaches. Quantum computer makers provide compilers that map logical sequences into packets of physical signal sequences best suited for a given qubit topology. More sophisticated ones perform certain optimizations, such as maximizing fidelity according to a qubit characteristics table, and inserting pulses for error correction. While FDMA addresses the resource utilization in frequency space, concepts like time division multiple access (TDMA) can be applied to improve hardware efficiency in the time domain. Kangbo Li and co-workers proposed that a qubit operation can be divided into a sequence of small pulses with precisely single flux quantum (SFQ) $h/2e$.[88] Since each SFQ pulse is about 2ps, there is ample time margin within 40 ps when using a central clock of 25 GHz (about 5 times of qubit frequency) to adjust phase shifts and accommodate the different qubit frequencies. Further claims have suggested that operations fidelities could also be improved by intermixing correction signals into SFQ pulses. Combining with FDMA, the quchip mimics wireless cellular phone networks, which optimize bandwidth and time utilization for the best total throughput.

### QPU-3D Integrations

For the past few years, several research groups have experimented with multi-layer 3D integration. In addition to an obvious purpose of scaling up qubit numbers, connection flexibility is also an important motivation. Many schemes have been applied to stack multiple silicon substrates in the z direction and form a 3D circuitry. For example, superconducting through silicon via (STSV) connects circuits on both sides of a silicon substrate. A cavity can span across a STSV and still maintain very high resonance quality.[85] Large numbers of STSV's are used to connect ground plans on both sides. A silicon substrate with 200 $\mu$m thickness has proved to be thick enough to provide a proper distance so that crosstalk between circuits on top and bottom can be minimized. On the substrate surface, holes of STSV are usually 10 $\mu$m to 20 $\mu$m in diameter, which are very economical for area utilization.

Another stacking scheme is flip-binding two circuitry planes face to face with $\sim 1\,\mu$m gap. With precise alignment, one qubit on one plane can couple with a cavity on the other. In order toensure gap uniformity across the two substrates, one substrate is etched so that hard stop pillars are formed in multiple places.[89] The results show comparable qubit lifetime and operation fidelity as those of 2D circuitry. STSV and flip-chip binding enable multi-layer integration of QPU, which increases qubit counts and flexibility of connections. Layers of switching and routing circuitry for microwave signals can be 3D-integrated with qubit layers, too.[85] Control/readout signals and bias DC lines from QPU can be connected to multi-layer PCB's for on-board signal processing or transmitted to external data collectors.[85] There are proposals suggesting that some classical functions, such as sequence timers be integrated inside QPU. More research is needed for digital circuits working in qubit cryostats and thermal noise issues.

### CONCLUSIONS AND PROSPECTS

QC now is related not only to fundamental physics research but also to engineering problems. Like IC designs, quchip designs will need tools as well.[90] We think that there will be computer aided design (CAD) tools specialized for cryogenic circuits with design parameters very different from those of current IC circuitry. With the great effort from interdisciplinary experts, scaling qubit numbers and error reduction are both possibly following a similar Moore's law for the next decades. Besides, quantum internet represents another attempt to increase scalability.[91] It creates a QC cluster by linking multiple QPUs together. If the QC cluster can be applied to distributed quantum computing, the entire computation landscape will be significantly changed.[92]

The ongoing superconducting qubits using Al or Nb materials is promising. However, other gate-tunable nanostructures[28,29] and topological materials with exotic surface states[57,59] may play an important role in designing new type of qubits. Although the same approach may be applied to semiconducting QDs, the current challenges of semiconducting QDs lie in the small number of entanglements, which is hindered by the fabrication difficulty (shorter gate separation required) resulting from the heavy effective mass of silicon. Other quantum materials, such as graphene and TMDC, have attracted considerable attention due to their distinct band structures, but more progress must be shown to justify their advantages. Layered 2D TI system, such as monolayer $1T' - WTe_2$, is a newly emerged material with gate-tunable

superconductivity. The gate-tunable switching between TI and superconductivity may allow exchange structures, like T-junctions, to be designed by gate in a single flake to verify the non-Abelian exchange statistics of MFs.

In this review, we have focused on the current status and possible future development of low-temperature qubit materials and cryogenic CMOS circuit designs. This is a brief summary of the basic physics of quantum materials and cryogenic circuits. In addition to superconducting qubits and silicon QDs, other possible two-dimensional and topological qubits were also introduced. Moreover, the importance of developing cryogenic peripheral electronic devices and understanding the solid-state physics of cryogenic CMOS circuits at deep low temperatures were also described as important R&D directions for future scale-up of quantum computers. Although QC is still in its early stages, educational quantum instruments and NISQ devices have gradually started to be promoted for different applications and can be purchased on the market. Cryogenic qubits and cryogenic circuitry design will remain the main trends for commercial quantum computers in the foreseeable future.

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## CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

## OPEN ACCESS

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