CORRECTION

Correction to: Influence of Substrate Surface Finish Metallurgy on Lead-Free Solder Joint Microstructure with Implications for Board-Level Reliability

MARION BRANCH KELLY,¹ TAPABRATA MAITY,¹ A.R. NAZMUS SAKIB,²
D.R. FREAR,² and NIKHILESH CHAWLA^{1,3}

1.—Center for 4D Materials Science, Arizona State University, Tempe, AZ 85281, USA. 2.—NXP Semiconductors, Austin, TX, USA. 3.—e-mail: nchawla@asu.edu

Correction to:

Journal of ELECTRONIC MATERIALS,
Vol. 49, No. 5, 2020
<https://doi.org/10.1007/s11664-020-08013-0>

In the original article, there is an error in Fig. 1.
Following is the corrected Fig. 1.

Fig. 1. Microstructural characterization of SAC 305 solder reflowed on matte Sn-plated (a, c, e) and Ni-plated (b, d, f) samples. Schematic diagrams of the top solder/substrate interface for the (a) matte Sn-plated and (b) Ni-plated samples, showing interface metallizations. The dashed line in (a) refers to the original matte Sn plating that dissolves into the SAC 305 solder during reflow and is not visible in subsequent SEM images. SEM images of cross sections of the as-fabricated (c) matte Sn-plated and (d) Ni-plated solder joints showing similar solder microstructures, but (e, f) higher-resolution images of the interfaces show variation in structure.