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A High-Efficiency 220 GHz Doubler Based on the Planar Schottky Varactor Diode

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In this paper, we present the design, analysis and measurement of a 220 GHz doubler, based on a planar Schottky varactor diode. The 3D model of the varactor diodes were firstly established in a high-frequency structure simulator, then the parasitic parameters were extracted and imported into advanced design system, in order to optimize the whole circuit. The experiment on the doubler was carried out, and the measured results showed the maximum output power of 21.39 mW with a corresponding efficiency of 24% at 218 GHz, which agreed well with simulation results. The conversion efficiency exceeded 10% in the frequency range of 197–230 GHz.

Key words: Terahertz wave, doubler, Schottky varactor diode, high conversion efficiency

INTRODUCTION

A terahertz source is the core part among all the research in terahertz technology; terahertz waves are acquired mainly from optical and electronic methods.[1–3] A large number of reliable terahertz sources have emerged. The gyrotron, traveling wave tube and other vacuum electronic devices are the main sources that can produce a high power. However, these sources have many limitations such as difficulty integrating with other circuits, inability to operate at room temperature and they are difficult to miniaturize.[4–6]

Although the output power is less than thaat of vacuum electronic devices, the diode, the transistor and other microwave devices can generate a continuous wave source with simple structure, high stability and reliability, and can operate at room temperature.[7–9] With the mentioned advantages, these devices can be widely used in THz circuits and systems when the requirement of driving power is not that high. At present, the research in terahertz source technology mainly focuses in millimeter and submillimeter wave bands, especially in several atmospheric transmission windows such as 140 GHz, 220 GHz, 340 GHz,[10] which is also the reason for choosing 220 GHz frequency band in this paper.

Solid-state terahertz sources are mostly obtained by frequency multiplication. A signal generation scheme for several important terahertz bands is presented in Fig. 1. As the solid-state amplifier is already developed at 3 mm wave band, the frequency multiplication chain usually begins from the 100 GHz (90–110 GHz). The doublers are often used in the front stage of the frequency multiplication chain because comparing to triplers, the efficiency of doublers are higher due to the simple structure and less loss in the circuit. Meanwhile, the front stage driver is often more important because it determines the performance of the whole circuit, if the driving power of the front stage is insufficient, the whole frequency multiplication chain may even fail to work. This is also the reason why the doubler in the terahertz frequency band draws more attention.

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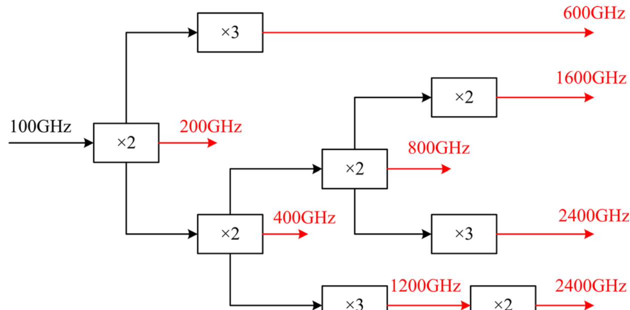

Fig. 1. Signal generation scheme for several important terahertz bands.

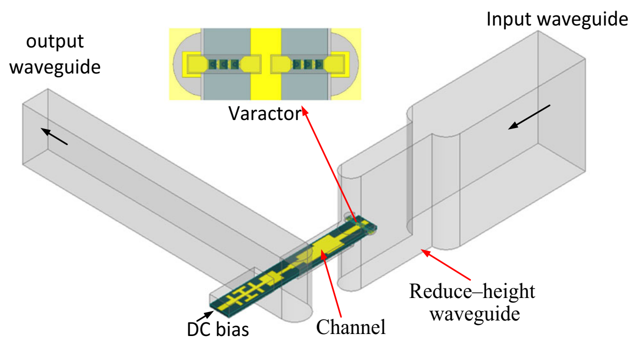

Fig. 2. 220 GHz doubler circuitry.

In this paper, a hybrid integrated balanced multiplying circuit is designed with planar Schottky varactors. In order to make the simulation results close to the real value, a 3D model of the planar Schottky varactor was studied and built. The planar Schottky varactor model, combined with the *S*-parameters and the intrinsic model of the diode model in the electromagnetic environment, is used to characterize the linear and nonlinear characteristics, and the high frequency parasitic effect. In order to solve the problem of poor accuracy in high-frequency circuit simulation, the method of structure joint simulation has been proposed. All passive networks are analyzed and designed using HFSS simulator. The non-linear behavior of the varactor diodes and optimization of the whole circuit is simulated by the ADS, based on the function of harmonic balance analysis.

DOUBLER DESIGN

The 220 GHz doubler circuitry is shown in Fig. 2, including the input and output waveguides-to-stripline transitions, the planar Schottky varactor diodes, DC bias, as well as the matching networks, in a balanced structure. In the balanced doubler, the matching networks are the most important parts, which consist of the input and output matching circuits. The matching networks make the fundamental wave transmitted to the diode pair as much as possible, while the output of the second harmonic is made as much as possible. In addition, the matching networks also match the impedance of the peripheral circuit to the extracted embedded impedance of the diode, thus maximizing the diode-generated second harmonic while suppressing other high-order harmonics.

In our doubler, the input signal is fed through the standard waveguide WR-8 and passes through the reduced waveguide to the diode pair. The diode pairs are placed at the center of the broad edge of the waveguide, because the value of the electric field here is the largest. The input signal produces all the harmonic waves because of the nonlinear effect of the Schottky varactor diode, and the output matching circuit selects the second harmonic wave and suppresses other harmonics. Because of the balanced structure, the odd harmonic waves counteract each other while the even harmonic waves remain unaffected.

Accurate Diode Modeling

Semiconductor devices are the basis for the design of solid-state frequency conversion circuits. Accordingly, semiconductor varactor diodes, which directly influence the performance of the mixer, are key components of the high efficiency doubler circuitry. As the operating frequency increases, issues become prominent such as high-frequency effects of semiconductor materials and the distribution parameter effect of the device package. The precision of the nonlinear model and the accuracy of parameter extraction have a direct impact on circuit performance and the efficiency of the circuit design. Whether the influence of the semiconductor diode structure to the circuit can be accurately simulated is the focus of the high-efficiency doubler design. Thus, a modeling approach combining the field and the circuit is a good way to solve the problem. In order to make the simulation close to reality, the research on diode models and performance is essential.

The basic composition and hierarchical structure of the Schottky diode are shown in Fig. 3. The Schottky diode consists of several layers including:

1. GaAs substrate: high-purity gallium arsenide on which the doped layers are grown; it also supports the whole device.
2. Buffer layer (n + GaAs): has a high concentration of doping and is located between the epitaxial layer and the substrate, which prevents the impurity of the GaAs substrate from spreading into the epitaxial layer; hence, it is called the buffer layer. At the same time, it forms an ohmic contact with the cathode and the high concentration of doping ensures a smaller ohmic resistance. Generally, the concentration of doping of the buffer layer is of the order of magnitude of 10^{18} cm^{-3}.

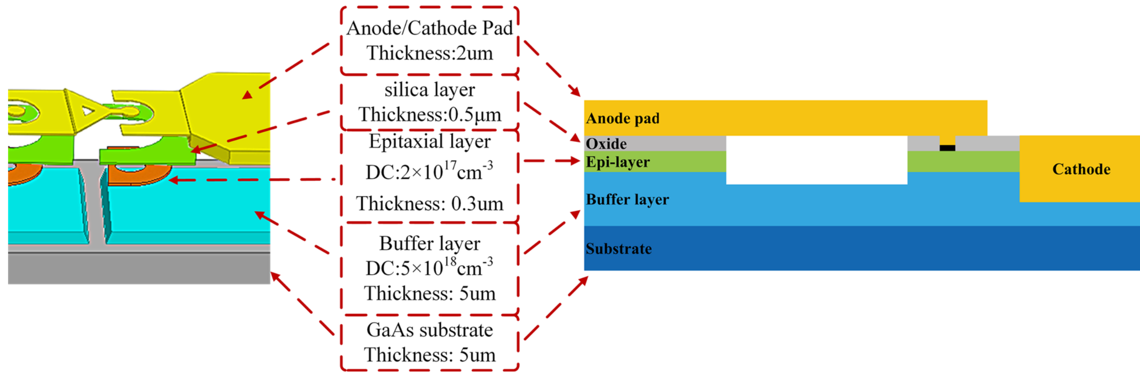

Fig. 3. Cross-sectional view of Schottky diode.

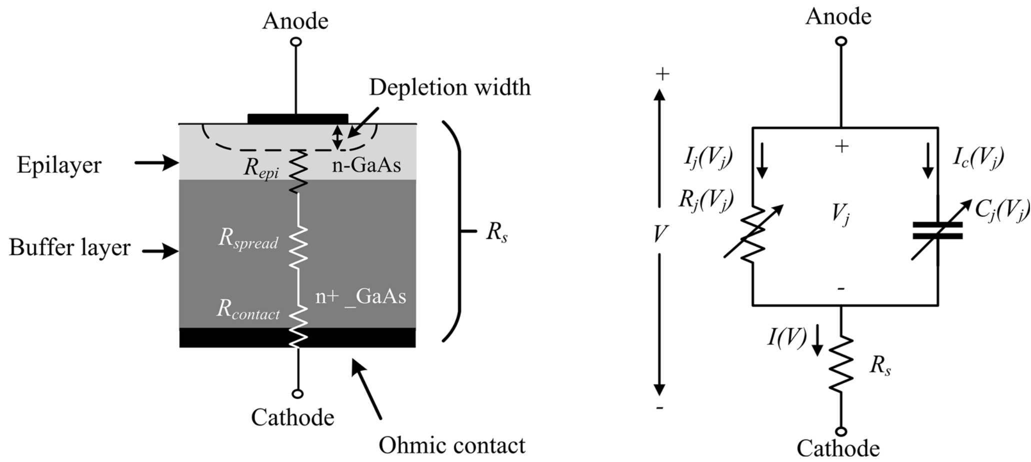

Fig. 4. Equivalent circuit model of the Schottky diode.

3. Epi-layer (n-GaAs): lightly doped and forms a Schottky contact with the anode; it is the layer where the nonlinear effect is generated. The doping concentration of the epi-layer is usually 1–2 orders of magnitude lower than the buffer layer (5×10^{16} cm^{-3}–5×10^{17} cm^{-3}); the specific value depends on the application and working conditions of the device.
4. Air bridge: suspended over the surface channel, which separates the anode pad from the cathode pad.

Schottky diodes can be analyzed accurately using relatively simple quasi-static approximations for the I–V and C–V, as shown in Eqs. 1 and 2.[11,12] The nonlinear capacitance C_j is caused by the changing depletion depth and is modeled as an abrupt junction capacitor with parallel plate spacing determined by the depletion region. The series resistance R_S is a parasitic element and accounts for ohmic losses in the structure. In addition to this basic model several high-frequency phenomena affect diode operation at THz frequencies.

$$I_d = I_{SAT}\left(e^{\left(\frac{v_j - I_d R_s}{v_0}\right)} - 1\right) \quad (1)$$

$$C_j = \frac{C_{j0}}{\sqrt{1 - V_j/V_{bi}}} \quad (2)$$

in which I_d is diode current, I_{SAT} is saturation current, V_j is junction voltage, C_j is junction capacitance, C_{j0} is zero bias capacitance, V_{bi} is applied voltage bias.

The equivalent circuit model of the Schottky diode[11,12] is shown in Fig. 4. The equivalent circuit model only considers the Schottky junction and does not take into account the influence of the parasitic parameters of the diode package. The model consists of a nonlinear junction resistance paralleled with a nonlinear junction capacitance and then cascaded

with a cascade resistor. The cascade resistance R_s is mainly composed of epitaxial layer resistance R_{epi}, buffer layer resistance R_{spead} and ohmic contact resistance $R_{contact}$, all of which are cascaded.

$$R_s = R_{epi} + R_{spread} + R_{contact} \tag{3}$$

$$R_{epi} = \frac{t_{epi}}{\sigma_{epi} A_a} = \frac{t_{epi}}{q\mu_{epi} N_d A_a} \tag{4}$$

$$\sigma_{epi} = q\mu_{epi} N_d \tag{5}$$

in which t_{epi} represents epi-layer thickness, σ_{epi} represents epi-layer conductivity, A_a represents anode area, μ_{epi} represents epi-layer electron mobility.

$$R_{spread} = \frac{1}{4\pi\delta_{buffer}\sigma_{buffer}} \tag{6}$$

$$\delta_{buffer} = \frac{1}{\sqrt{\pi f \mu_0 \sigma_{buffer}}} \tag{7}$$

$$\sigma_{buffer} = q\mu_{buffer} N_{buffer} \tag{8}$$

in which δ_{buffer} represents buffer layer skin depth, $\sigma_{bufffer}$ represents epi-layer conductivity, μ_0 represents magnetic permeability in free space, μ_{buffer} represents buffer layer electron mobility, N_{buffer} represents buffer layer doping concentration.

$$R_{contact} = \frac{2 \times 10^{-6} (\Omega \cdot \mathrm{cm}^2)}{A_{ohmic}} \tag{9}$$

in which $A_{\Omega ic}$ represents ohmic contact area.

Expression of junction capacitance $C_j(V_j)$ is shown in Eq. 8.

$$C_j(V_j) = \frac{dQ_j}{dV_j} = A_a \sqrt{\frac{qN_d \varepsilon_s}{2(V_{bi} - V_j)}} = \frac{A_a \varepsilon_s}{d} \tag{10}$$

When the junction voltage is zero, zero bias capacitance is obtained.

$$C_{j0} = A_a \sqrt{\frac{qN_d \varepsilon_s}{2V_{bi}}} \tag{11}$$

The cut-off frequency of the Schottky diode can be seen in Eq. 12. It can be used as a physical quantity to characterize the quality of the Schottky diode. The larger the diode, the better its quality and the more suitable it is for use in the higher frequency band.

$$f_c = \frac{1}{2\pi R_s C_{j0}} \tag{12}$$

The following parameters should be considered for the varactor used in the doubler:

1. Epitaxial layer doping concentration N_d. According to the principle of diode junction, the smaller the epitaxial layer doping concentration N_d, the larger the absolute value of the reverse breakdown voltage, which means the diode can bear the higher input power, but with the decrease in N_d, the cascade resistance increases and the frequency doubling efficiency is reduced.
2. Epitaxial layer thickness t_{epi}. The larger the thickness of the epitaxial layer, the larger the cascade resistance, which decreases the efficiency of frequency doubling.
3. Epitaxial layer thickness A_a. Under the same junction voltage, the larger the anode area, the larger the junction capacitance, and accordingly, the ability of the diode to accept higher input power. However, the larger the anode area, the more difficult the design of the matching circuit.[11]

Although only a few parameters of the varactor must be determined, it is not a simple process to design a varactor, as it involves comprehensive consideration of many aspects of the circuit performance. The design of the varactor needs to be based on the actual requirements of the circuit performance, so that it is more optimally targeted.

In order to increase the power capacity of the diode, a common approach is to integrate more anodes on the diode chip, which will inevitably lead to an increase in the diode size. As the doubler operates at the terahertz band, the geometric size of the circuit decreases correspondingly. The increase of the chip size tends to have a negative impact on the electromagnetic characteristics of the circuit, hence, the ability to increase the number of anodes is limited. Finally, the 5VA30-13 varactor diode produced by ACST is adopted, and a 6-die balanced

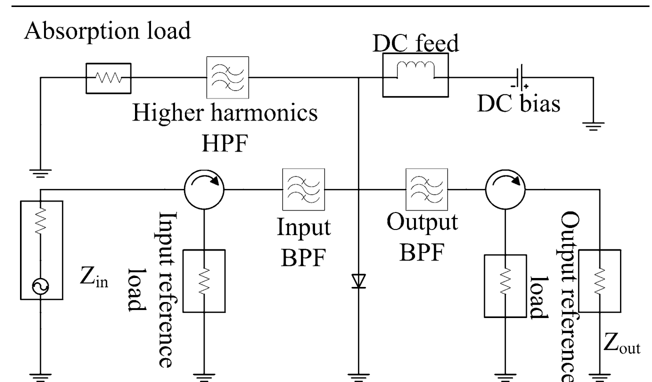

Fig. 5. Load pull analysis of the doubler.

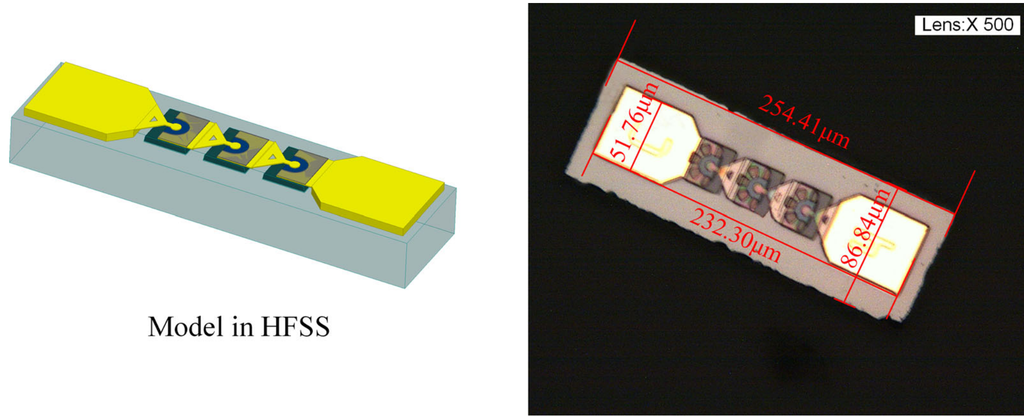

Fig. 6. ACST 3-anode diode chip model.

Table I. Main parameters of the ACST diode

I_S	Saturated current (A)	5×10^{-15}
R_S	Junction resistance (Ω)	3
N	Emission coefficient	1.2
C_{j0}	Zero bias junction capacitance (fF)	40
V_j	Barrier voltage (V)	0.9
M	Junction capacitance gradient coefficient	0.5
B_v	Reverse breakdown voltage (V)	10
I_{bv}	Reverse breakdown current (μA)	10
E_g	Band gap width (eV)	1.42

double frequency circuit obtained by using two 5VA30-13.

Based on the idea of the optimal working state of the diode, the load-pull analysis of the doubler is set up in the ADS as shown in Fig. 5. The optimal performance of the varactor is evaluated using the load-pull method. The influence of varactor parameters on the doubler performance is analyzed. The performance of a single anode is analyzed in this model, so that the number of anodes on the diode chip can be determined according to the circuit requirements.[13]

The simulated results show that the conversion efficiency of a single anode is greater than 44% in the 200–240 GHz frequency band when the optimum driving power of the anode is 14.8 dBm and bias voltage is − 3.3 V. The source impedance is $12.6 + j*68.86$ Ω and the load impedance is $15.5 + j*34.42$ Ω at this condition.

The model of the varactor is built in the HFSS by measuring the size with a microscope and consulting the relevant data, as shown in Fig. 6. It contains three anodes in series and the size of the package is 254.4 μm*86.8 μm*35 μm. Table I shows the main parameters of the 5VA30-13.

Overall Circuit Simulation

The accurate 3D model of the varactor diode is established in the "Accurate Diode Modeling" section. The model can accurately simulate the effects of the varactor diode on the circuit and its parasitic characteristics based on electromagnetic field theory. However, it cannot simulate the nonlinear characteristics. Therefore, in order to get the complete varactor diode model by combining the semiconductor peripheral structure model and the Schottky junction nonlinear model, the method of combining 3D electromagnetic field with a nonlinear circuit is adopted. In addition, the harmonic balance algorithm and an ideal PN junction diode is adopted to build the overall circuit in ADS, as illustrated in Fig. 7.

The simulation results are carried out after optimizing the circuit; the best DC bias proves to be − 3.1 V per anode, as shown in Fig. 8a. The bias voltage changes the parameters of the die, so at different frequencies, the bias voltage required for the multiplier to achieve optimal operation are different. As described in Fig. 8b, the best driven power of the 220 GHz doubler is 80 mW, and the

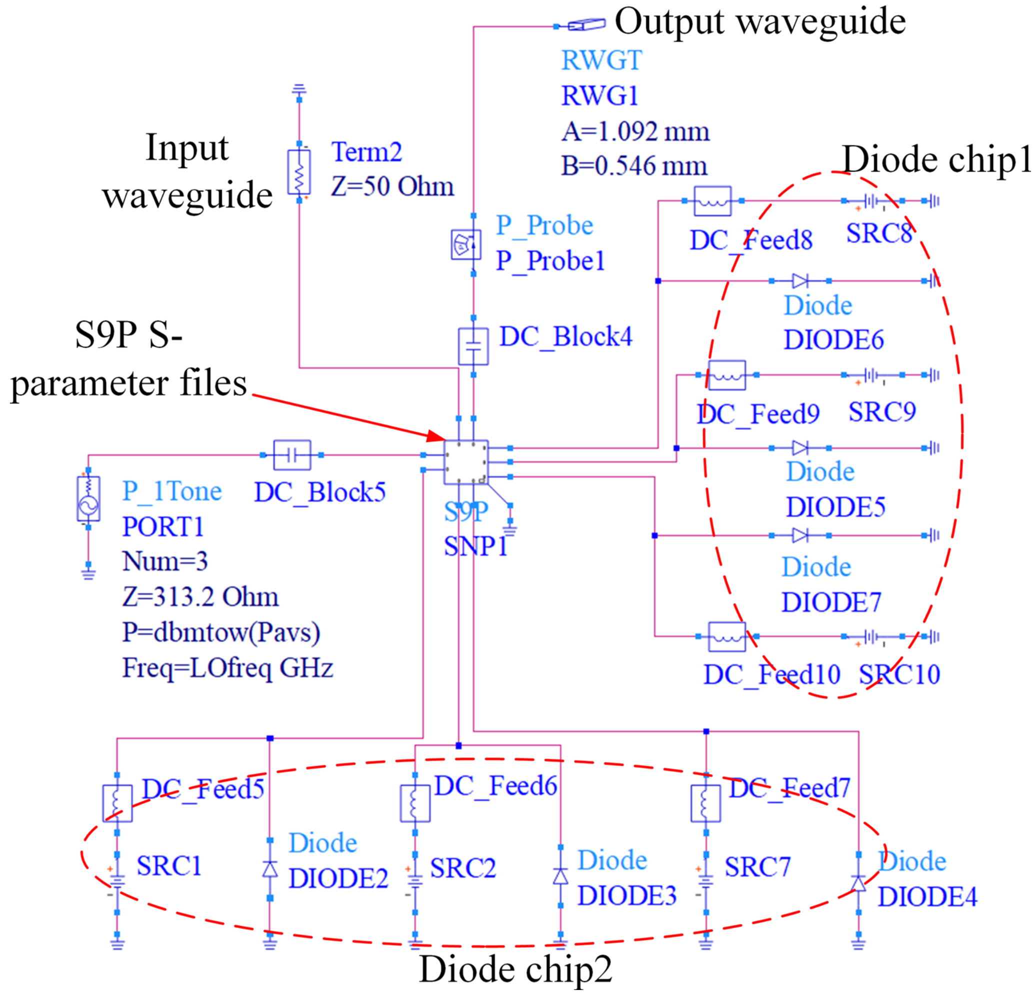

Fig. 7. The entire circuit simulation diagram of the high-efficiency doubler in ADS.

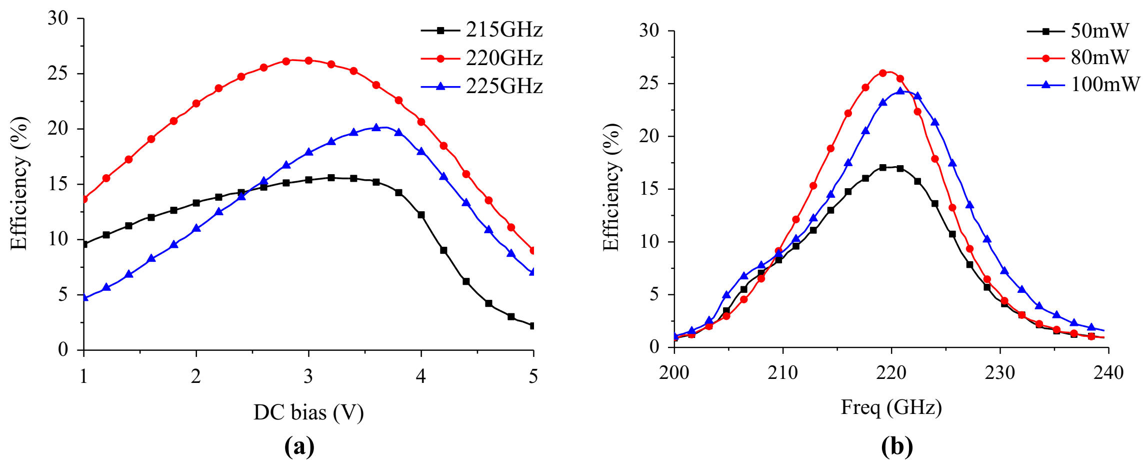

Fig. 8. (a) Simulation efficiency varies with bias voltage (negative) at three frequencies, (b) simulation efficiency with different driven power when the DC bias is − 3.1 V.

efficiency in the 214–225 GHz band is greater than 15%, and the efficiency is 27.44% at 220 GHz. The DC bias of the doubler has good consistency with the optimal impedance voltage (− 3.3 V) of a single chip established in "Accurate Diode Modeling".

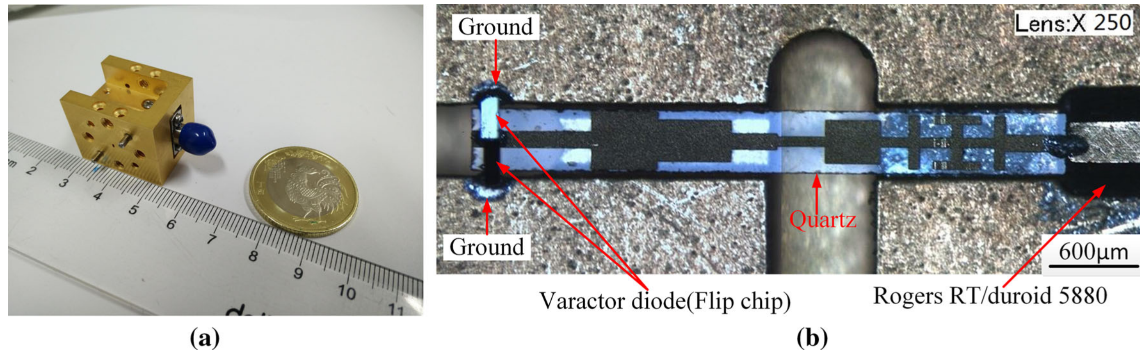

Fig. 9. Physical photograph of 220 GHz doubler: (a) overall appearance; (b) the image of the lower part of the assembled mixer block.

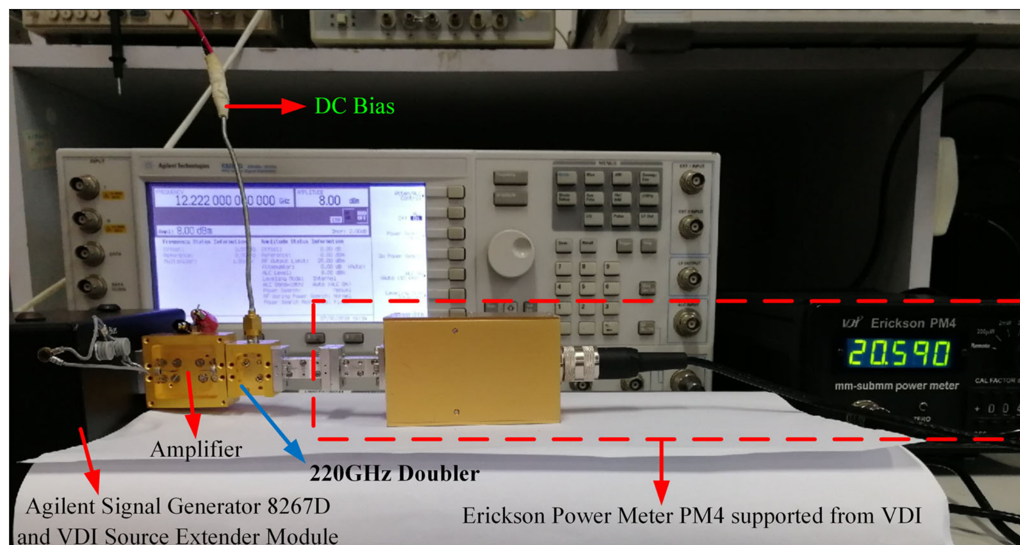

Fig. 10. Test platform of the 220 GHz doubler.

FABRICATION AND MEASUREMENTS

The entire doubler is set in an *E*-plane split-waveguide copper block with a volume of 20 mm × 20 mm × 20 mm, as shown in Fig. 9a. The high-efficiency 220 GHz doubler circuit inside the waveguide block is shown in Fig. 9b. The copper cavity is gilded. Silver glue is used on both sides of the varactor to connect the microstrip line with the cavity as earthing. At the same time, the silver glue fixes the quartz substrate on the groove of the cavity to construct a suspended structure, and the quartz substrate is linked to the *K* connector through a 50 Ω microstrip line based on Rogers RT/Duroid 5880.

The experimental test platform is shown in Fig. 10. The input signal is provided by driving a 9X doubling chain with Agilent Technologies E8257D, then fed into the 220 GHz doubler, while the output power is tested by a thermal power meter PM4. Moreover, the DC power supply provides bias voltage to the double frequency through the coaxial line. The bias voltage is adjusted until the maximum output power of the doubler is obtained at 220 GHz as shown in Fig. 11a. This is very close to the − 3.1 V obtained from the simulation results. The output power of the doubler is test with different driven power, as shown in Fig. 11b, when the driven power is about 80mW, the output power is optimal, which is highly consistent with the simulation results. Adjusted the simulated bias voltage to − 2.9 V with the best driven power, simulated and measured are shown in Fig. 11c, the maximum output power of the doubler achieved is 21.39 mW at 218 GHz. The output power is larger than the 12 mW in the 210–225 GHz frequency

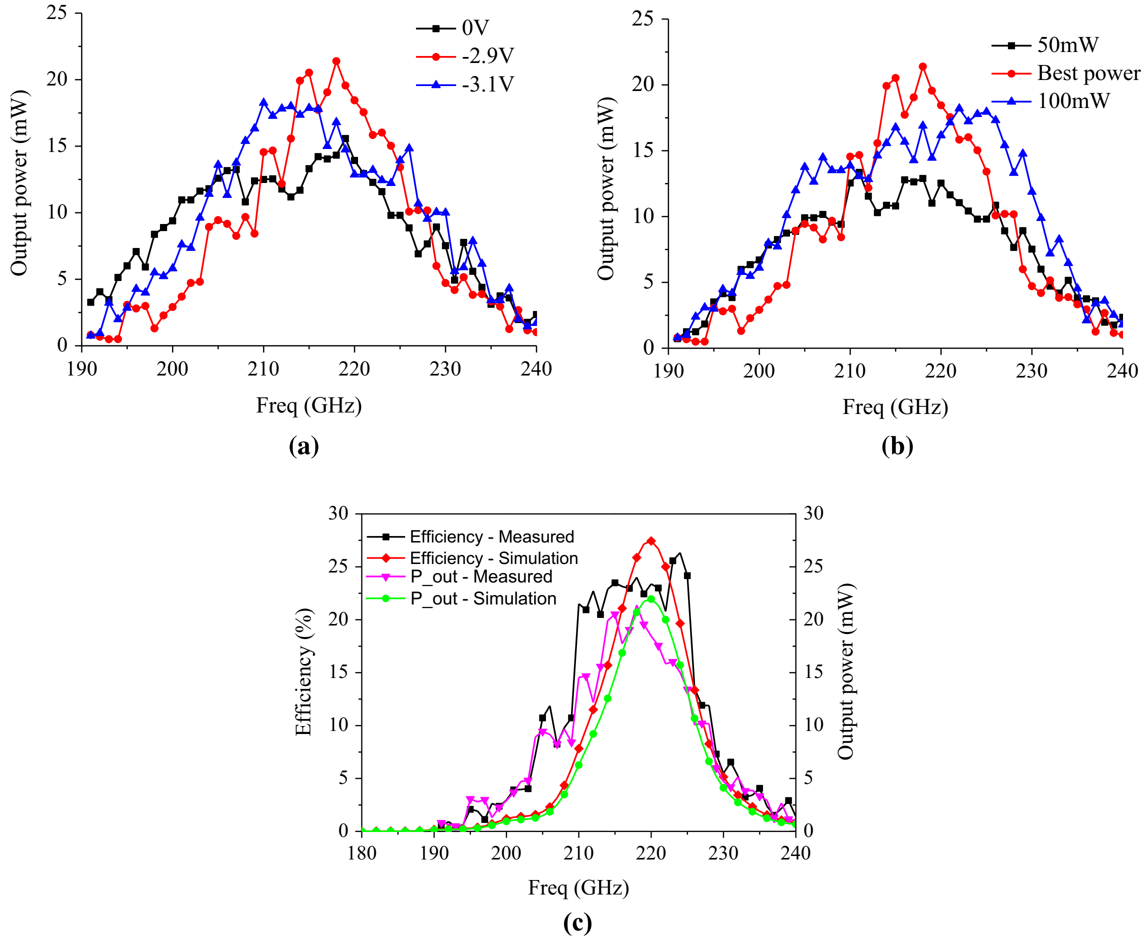

Fig. 11. (a) Measured output power with different DC bias with the best driven power, (b) measured output power with different driven power when the DC bias is − 2.9 V (best power is about 80 mW), (c) simulated and measured results of the 220 GHz doubler with the best driven power when the DC bias is − 2.9 V.

Table II. Summary of published doubler performance in the same frequency range

Reference	Frequency (GHz)	Output power (mW)	Efficiency
14	190–198	20@198 GHz	> 2%@191–198 GHz 8%@193 GHz
15	190–225	8.25@202 GHz	> 6%@190–225 GHz 9.6%@202 GHz
16	212–232	15@219 GHz	> 4%@212–230 GHz 5.8%@215 GHz
This paper	190–235	21.39@218 GHz	> 10%@197–230 GHz 24%@218 GHz

band. The efficiency in the 210–225 GHz band is greater than 20%, and the efficiency achieved is 26.34% at 224 GHz. In addition, since silver glue is used to fix the diode and earth, the offsets of the diode and the quartz substrate will have an uncertain effect on the matching circuit of the doubler, which results in the fluctuation of the measured curves with the input frequency. But the test and simulation curves are consistent in the basic trend and output power value, which verifies the correctness of our design.

A summary of doubler performance, published in both domestic and foreign research papers, is listed in Table II. The comparisons show that the efficiency and output power of the doubler in this paper, have achieved good results.[14,16]

SUMMARY

A 220 GHz doubler based on a GaAs Schottky varactor diode is presented in this paper. A 3D electromagnetic model of the diode was established in the HFSS and its characteristic parameters were extracted. Then, the harmonic balance method was used to optimize the overall circuit of the frequency doubler. Finally, an experimental study of the doubler was carried out. The simulation results showed that when the driving power is 150 mW, the doubler efficiency is higher than 15% in the 210–230 GHz frequency band and it can achieve a maximum efficiency of 41% at 211 GHz. The measurement results show that doubler efficiency is higher than 10% in 197–230 GHz. The maximum output power is 21.39 mW at 218 GHz and the corresponding efficiency is 24%, which is consistent with the simulation results under the same conditions.

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