Effect of Doping Concentration Variations in PVT-Grown 4H-SiC Wafers

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Synchrotron white beam x-ray topography studies carried out on 4H-SiC wafers characterized by locally varying doping concentrations reveals the presence of overlapping Shockley stacking faults generated from residual surface scratches in regions of higher doping concentrations after the wafers have been subjected to heat treatment. The stacking faults are rhombus-shaped and bound by Shockley partial dislocations. The fault generation process is driven by the fact that in regions of higher doping concentrations, a faulted crystal containing double Shockley faults is more stable than a perfect 4H-SiC crystal at the high temperatures ($>1000^{\circ}\text{C}$) that the wafers are subject to during heat treatment. We have developed a model for the formation mechanism of the rhombus-shaped stacking faults. Our studies show that during heat treatment of the wafer, such double Shockley faults can be generated in regions where dislocation sources are presents (e.g. scratches or low-angle boundaries) and when the nitrogen doping concentration exceeds a certain level.

Key words: 4H-SiC, double Shockley stacking faults, heat treatment, x-ray topography, doping, rhombus-shaped

INTRODUCTION

4H-SiC is an outstanding material due to its superior properties such as large band gap, high thermal conductivity and excellent chemical and physical stability. The unique combination of those properties makes it a candidate material to gradually replace conventional semiconductors in high-temperature, high-power and high-frequency applications.^{1,2} In addition, SiC is widely used as a substrate for nitride-based light emitting diodes (LEDs) due to its smaller lattice mismatch ($\sim 3.4\%$)

compared with sapphire ($\sim 16\%$). However, SiC device performance can be severely affected by the presence of defects inside the crystals. Stacking faults can be particularly detrimental since they introduce quantum wells that serve as recombination centers. This has the effect of reducing the minority carrier lifetime, increasing the resistance of the drift region, which in turn introduces undesirable forward voltage drift during device operation.³

Double Shockley stacking faults (DSSFs), comprising pairs of Shockley faults on adjacent basal planes, are known to spontaneously form in 4H-SiC when the N doping level is above a certain critical threshold and where Si core partial dislocations can

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overcome the activation barrier to their motion (by way of high temperature or a combination of high temperature and applied stress). In this study, we focus on DSSFs formed in localized regions of 4H-SiC wafers where the doping threshold is surpassed and which were subjected to a high-temperature annealing. There have been several reports of such spontaneous fault formation. Okojie et al.⁴ reported the observation of a high density of DSSFs in a nitrogen-doped epitaxial layer deposited on a *p*-type substrate after the sample had been oxidized at 1150°C. In another study by Kuhr et al.,⁵ the existence of DSSFs was revealed in highly nitrogen-doped 4H-SiC samples following annealing at 1150°C in an Ar environment. Pirouz et al.⁶ reported the generation of DSSFs from scratches in highly *n*-doped 4H-SiC which were subjected to either a high-temperature annealing or a combination of an annealing plus applied stress. Kuhr et al.⁵ proposed an electronic mechanism for the DSSF formation and expansion.

EXPERIMENT

4H-SiC wafers used in this study were sliced from single crystal boules grown by seeded physical vapor transport (PVT) method. The nitrogen doping concentration varies across the wafer surface form. After slicing, the wafer was subjected to chemical mechanical polishing (CMP) followed by a high-temperature heat treatment. Residual surface scratches have been left over on both faces by the CMP process. Using synchrotron white beam x-ray topography (SWBXT), the area contrast of stacking faults is observed in the high doping regions. 1–100 and $-110-1$ reflections were recorded in transmission geometry in order to analyze the different contrast behaviors of those stacking faults. In order to determine the Burgers vectors of the bounding

partial dislocations of these stacking faults, three types of 11–20 reflections were also recorded in transmission geometry. SWBXT experiments were carried out at the Beamline 1-BM-A facility of the Advanced Photon Source in Argonne National Laboratory.

RESULTS AND DISCUSSION

Experimental Observation and Analysis of DSSFs

Using an SWBXT technique, the existence of stacking faults can be confirmed by observing the area contrast arising from the phase shift experienced by the x-ray wavefields as they cross the fault plane. A large number of overlapping stacking faults are observed decorating around the residual surface scratches (from the CMP process) in regions of higher doping concentration, as shown in Fig. 1, which implies the stacking faults are generated from the scratches after the wafer was subjected to the high-temperature treatment. The white dashed lines in Fig. 1 delineate the locations of the scratches in those more highly doped regions from where the stacking faults are generated. Based on $g\cdot R$ analysis, inside the highly doped regions, all the stacking faults are determined to be Shockley type since the contrast are very well marked in -1100 and -1101 topographs (Fig. 1).

More details of the faults are revealed in the higher magnification images shown in Fig. 2 recorded from the border between high and low doped regions. Inside the higher doped regions, each stacking fault appears as a rhombus shape bounded by partial dislocations. The overlapping of multiple SFs can be discerned through the relative intensities of their contrast. In contrast, the relatively lower doped regions are free from such stacking faults.

Fig. 1. DSSFs inside the high doping region of 4H-SiC wafer recorded in (a) $g = -1100$, (b) $g = -1101$ using SWBXT in transmission geometry. The white dashed lines delineate the scratches in the high doping region, from where several stacking faults are generated.

Fig. 2. High-magnification topographs showing overlapping, rhombus-shaped, double Shockley faults in the high-doping area in (a) $g = -1100$, (b) $g = -1101$.

Fig. 3. Transmission x-ray topographs showing the contrast from partial dislocations from the same area recorded in (a) $g = 11-20$, (b) $g = -12$ to 10, (c) $g = -2$ to 110. Rhombuses with long axes along $10-10$ disappear in -12 to 10 reflection indicating a Burgers vector of $1/3[10-10]$. Rhombuses with long axes along $01-10$ disappear in -12 to 10 reflection indicating a Burgers vector of $1/3[01-10]$.

The Burgers vector of those bounding partials can be determined by analysis of their contrast behavior on different reflections. All partial dislocations making up the rhombus shapes disappear whenever the g vector is perpendicular to the long axes of the rhombus. According to $g \cdot b$ contrast analysis, the Burgers vectors for all the partials comprising the rhombus-shaped loops are determined to be along $\langle 1-100 \rangle$. This is demonstrated in Fig. 3 in which the same area was imaged using 3 different $11-20$ reciprocal lattice vectors. We observed that the rhombuses with long axes along $[10-10]$ disappear on the $-12-10$ reflection. Meanwhile, the rhombuses with long axes along $[01-10]$ disappear on the $-12-10$ reflection.

Expansion Directions

Generally, the stacking faults can be nucleated at scratches on either the C or Si face of the 4° off-cut single crystal wafer. Depending on which face the scratches are located on, the rhombic-shaped stacking faults should expand toward different

directions. A schematic illustration of this is shown in Fig. 4. On the Si face, they should expand toward the upstep direction, while on the C-face, they expand toward the downstep direction. The confirmation from the experimental observation is shown in Fig. 5. The $11-20$ (Fig. 5a) and -1100 (Fig. 5b) reflections are recorded from the same area. On the $11-20$ reflection, only the bounding partial dislocations are visible while the stacking faults are out of contrast as predicted for Shockley stacking faults. On the -1100 reflection, both the stacking faults and the partials are in contrast. Those faults expanding towards the downstep direction are marked with dark arrows and were expected to be generated from the C face, while those expanding towards the upstep direction are marked with white arrows and were expected to be generated from the Si face.

Formation Mechanism

At relatively high temperatures, but below the brittle-to-ductile transition temperature, surface

Fig. 4. Schematic illustration of stacking fault expansion from scratches on the Si face (a), and on the C face (b) of the wafer. The tilted plane inside the crystal is the basal plane which has an offcut angle with respect to the crystal surface.

Fig. 5. Transmission images recorded from the same area showing the contrast of bounding partials in (a) $g = 11-20$, and the contrast of the stacking faults in (b) $g = -1100$. The direction toward the left is the projected downstep direction. Those faults expanding towards the downstep direction are marked with dark arrows, while those expanding towards the upstep direction are marked with white arrows (show the downstep direction on the figure).

scratches on 4H-SiC can nucleate hexagonal-shaped partial dislocation loops. Each of the segments of the hexagonal loop initially lie in the low-energy Peierls valley, i.e. $\langle 11-20 \rangle$ directions. In addition, the partial segments has a Burgers vector of $1/3\langle 1-100 \rangle$; each partial segment comprising the individual hexagonal loop should end up with either 30° or 90° character with cores comprising either Si or C atoms. The configuration of this hexagonal-shaped partial dislocation loop model is illustrated in Fig. 6. At temperatures below the brittle-to-ductile transition temperature, the Si core partial is mobile, whereas the C core partial is sessile, so that both 30° and 90° Si partials glide while the C core partial stays. Additionally, the 90° character Si core partials move faster than the 30° Si core partials, so that the 90° Si core partials eventually move out, leaving behind the 30° Si partials; the 30° C partials

Fig. 6. The rhombus-shaped stacking fault configuration generated by expansion of a hexagonal partial loop with a Burgers vector of $1/3[1-100]$ and sides along $\langle 11-20 \rangle$ Peierls valleys. The 90° Si core partial eventually moves out at the end of the expansion process.

extend toward their line directions simultaneously. Therefore, the final configuration is a rhombus-shaped stacking fault. This expansion process is also illustrated schematically in Fig. 6.

It has been established theoretically that when 4H-SiC is highly doped, the presence of Shockley stacking faults can lower the free energy of the faulted crystal compared to the perfect crystal.⁵ Double Shockley faults, created by the motion of two leading Shockley partials on adjacent basal planes, are predicted to provide a greater energy-lowering effect than single Shockley faults. Therefore, if the barrier to the motion of the Shockley partial dislocations can be overcome, such highly doped crystals are expected to spontaneously fault via the expansion of double Shockley faults. High-temperature heat treatment can provide the partials with the energy necessary to overcome this barrier. Calculations by Kuhr et al.⁵ and observations by Pirouz et al.⁶ showed that a faulted crystal containing these double Shockley faults is more stable than the perfect 4H-SiC crystal at temperatures greater than 1000°C, provided a threshold doping level of around $2 \times 10^{19} \text{ cm}^{-3}$ is exceeded. The fact that we observe such stacking fault formation in more highly doped regions suggests that the doping level in those regions exceeds this threshold value. Since the faults are observed to nucleate at surface scratches, this suggests that the small dislocation loops are expected to be decorating such scratches as the sources for the Shockley partials needed for the fault expansion.

CONCLUSIONS

We observed overlapping rhombus-shaped Shockley stacking faults bound by Shockley partial dislocations generated from residual surface scratches in regions of higher doping concentration after the sample has been subjected to heat treatment. These faults result from the expansion of hexagonal-shaped partial dislocation loops nucleated from the

scratches under the influence of thermal gradient stresses at high temperatures below the brittle-to-ductile transition temperature; and the difference in mobilities of the Si and C core dislocations, and that of 30° and 90° character segments. The faults are double Shockley faults formed by the gliding of two leading partial dislocations on adjacent basal planes. When the doping concentration in some regions of the wafers exceeds the threshold concentration for fault formation, there is sufficient driving force for faulting to occur. Thus, our studies show that double Shockley faults can be generated in regions where dislocation sources are present (e.g. scratches or low-angle boundaries) and when the nitrogen doping concentration exceeds a certain level. The experimental verification of the rhombus partial dislocation loop model for the preferential motion of the Si core partials and for the double layer Shockley faults nature will be published in the next paper.

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