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Effect of Grain Boundary Misorientation on Electromigration in Lead-Free Solder Joints

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Reduction in microelectronic interconnect size gives rise to solder bumps consisting of few grains, approaching a single- or bicrystal grain morphology in C4 bumps. Single grain anisotropy, individual grain orientation, presence of easy diffusion paths along grain boundaries, and the increased current density in these small solder bumps aggravate electromigration. This reduces the reliability of the entire microelectronic system. This paper focuses on electromigration behavior in Pb-free solder, specifically the Sn-0.7 wt.%Cu alloy. We discuss the effects of texture, grain orientation, and grain boundary misorientation angle on electromigration (EM) and intermetallic compound formation in EM-tested C4 bumps. The detailed electron backscatter diffraction (EBSD) analysis used in this study reveals the greater influence of grain boundary misorientation on solder bump electromigration compared with the effect associated with individual grain orientation.

Key words: Electromigration, lead-free solder, grain orientation effect, grain boundary misorientation effect, intermetallic compound, C4 bump

INTRODUCTION

The continued form-factor reduction and miniaturization of flip chip controlled collapse chip connection (C4) solder bumps and the transition to lead-free solders in support of health, safety, and environmental protection have introduced many challenges in terms of reliability issues in microelectronics packaging systems. Maintaining the electromigration (EM) resistance of solder interconnects is critical to ensure that product integrity and performance are preserved during these transitions. Many investigators have reported that electromigration, which involves mass transport of atoms driven by the combined forces of electric field and charge carriers, is influenced by material chemistry, structure/anisotropy, and microstructure. In addition to grain orientation effects, the increase in current density caused by the reduction in interconnect size further aggravates the effects of electromigration. The preferred techniques for studying how these factors impact EM behavior include orientation imaging microscopy and electron backscatter diffraction (EBSD).[1] Industry has focused on solder alloy material development and microstructure control to overcome this increased EM susceptibility.

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Flip Chip Microelectronics Package Design

Flip chip technology and C4 interconnect design are commonly used in microelectronics systems. C4 solder joints provide the signal path between solid-state devices and adjacent levels of electronics packaging. Schematics of C4 interconnect design consisting of solder bumps on wettable copper metal layers and the current pathways in a C4 device are shown in Fig. 1.

Lead-Free Solder Issues

Shifting to lead-free solder systems involves new solder material development, including chemistry

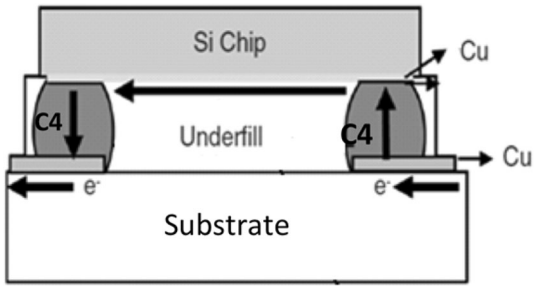

Fig. 1. Schematic of a flip chip package and current path through solder interconnects and trace layers.

modification to compositions containing mixtures of tin, silver, copper, etc. Some of the concerns in transitioning from lead-rich to lead-free solders include:

- Increased melting temperature and higher reflow temperature requirements
- Higher intermetallic compound (IMC) formation at the solder joint, due to the increased dissolution rate and solubility of Cu in solder associated with this higher reflow temperature
- Degraded electrical performance due to reduced conductivity with enlargement of IMC
- Reduction in mechanical integrity due to brittle IMC at solder joints
- Higher thermal loading developed during manufacturing with higher reflow temperature
- Greater coefficient of thermal expansion (CTE) mismatch stress between the substrate and the silicon die
- Increased surface and interfacial energies, which can influence wetting characteristics and increase the contact angle between solder and copper layer
- Reduced EM resistance associated with increased current density and current crowding
- Microstructural differences and the presence of distributed IMC precipitate phases (e.g., Sn_5Cu_6 and $SnAg_3$ in Sn-Ag-Cu solder alloy), impacting material behavior

Tin-Based Solder and IMC Crystal Structure

The primary component in most lead-free solders is Sn, which has a body-centered tetragonal (BCT) lattice structure at temperatures above 13.2°C. The most and least close-packed directions/planes in tin crystals are [001]/(100) and [110]/(001), respectively, and the active slip system is reported to be (100)[001].[2,3] The crystal structure of the Sn_5Cu_6 IMC which forms in Cu-Sn solder joints is hexagonal close-packed (HCP), potentially resulting in IMC grains with basal plane growth front alignment.

Electromigration

Electromigration associated with mass transport due to applied current is of critical concern in microelectronics systems. EM in solder bumps leads to the formation of voids, hillocks [IMCs forming due to limited solubility of migrating under bump metallurgy (UBM) atoms in solder material], and/or IMC. Such changes affect the mechanical, electrical, and thermal properties of the joint, and can result in premature failure of the solder connection. Voids generally form at the cathode side, whereas hillocks/IMC atoms accumulate at the anode side. These void and IMC regions also introduce an impedance mismatch in the interconnects, increasing the resistance and impacting signal integrity and electrical performance.[3] Lastly, increased levels of IMC formed through the EM process can lead to local embrittlement and premature mechanical failure.[4]

The reduced current-carrying ability of the solder due to the formation of IMC and voids not only increases the current density but also introduces current stressing/crowding at the contact area between the solder and UBM. These factors further aggravate electromigration.[5]

Mechanism of Electromigration and Controlling Factors

Electromigration is described as the mass transport of atoms driven by the combined forces of electric field and charge carriers. The drifting electrons collide with atoms, causing one of the atoms to exchange position with a neighboring vacancy during current stressing. The flow of energetic electrons can lead to increased atom migration. This effect furthers the mobility of Cu atoms from UBM into Sn solder, leading to an increased level of IMC growth at the anode side.

Many studies[6–8] have shown an increased level of IMC growth due to electromigration, over and beyond what is expected from thermally diffused atoms. The augmented electromigration is due to the increased movement of atoms when subjected to a current density exceeding a threshold level. After stressing for an extended time, atoms in interconnects accumulate on the anode side, resulting in UBM dissolution on the cathode side that can lead to open failure with time.

The main conditions for electromigration include: (i) sufficient energy for atoms to overcome the barrier for diffusion, with grain boundary migration dominating at low temperature due to its reduced energy requirements, and (ii) availability of sites which are energetically and geometrically favorable "sinks" for the atom to move to. Vacancies, dislocation cores, grain boundaries, and voids are potential sinks or favorable sites for the accumulation of atoms and IMC formation. Current crowding, Joule heating, and solder grain orientation also influence the rate of electromigration.[1,5,9,10]

Many researchers have investigated the effect of grain orientation on electromigration. Kinney et al.[1] studied the influence of crystal orientation on intermetallic growth in lead-free single-crystal solder samples subjected to uniaxial current. The

EM tests in that study were performed at current densities of 10,000 A/cm^2 and 11,500 A/cm^2, held at 100°C for 24 h, 48 h, 96 h, and 120 h. Kinney et al.[1] used EBSD orientation maps constructed per stereographic projection 2 (SP2) in evaluating the grain orientation effect. In SP2 the grain orientation is quantified according to the angle that its *c*-axis [001] makes with the electron flow direction (the direction perpendicular to the solder/Cu joint). The authors concluded that grains oriented with their *c*-axis [001] closely aligned to the electron flow path experience significantly higher IMC growth compared with grains with their *c*-axis perpendicular to the electron flow. They further showed that the IMC growth front was nearly planar, exhibiting a constant orientation along the Cu/Sn interface. Other investigators have also reported similar behavior.[11]

ELECTROMIGRATION IN FIRST-LEVEL INTERCONNECTS (FLIP CHIP C4 BUMPS)

In the study presented here, we demonstrate the effect of grain orientation on EM behavior of lead-free solder in actual C4 bumps. The applicability of the results from simple test configurations reported by other investigators to more complex configurations such as C4 bumps was also evaluated.

Experimental Procedures

The lead-free (Sn-0.7Cu) C4 solder bumps evaluated in this study were sampled from first-level interconnects (FLIs) in flip chip ball grid array (FCBGA) packages supplied by Intel Corporation. The FLI C4 bumps were encapsulated in a nonmetallic underfill layer (a commonly used practice in microelectronic packages). The samples were EM-tested using accelerated life tests (ALTs) at 165°C and 800 mA/bump. The test current density was estimated to be ~24,880 A/cm^2. The current density was calculated using the bump pad diameter measured on pre-EM-tested end-of-line (EOL) sample bumps. Three sets of bumps from three packages, totaling 104 bumps (27, 41, and 36 bumps from package numbers 31, 36, and 39, respectively), were evaluated in this study. Package numbers 31, 36, and 39 were tested for 227 h, 222 h, and 215 h, respectively.

The current direction during ALT was the same in all cases. Figure 2 demonstrates the current and electron flow directions with respect to the cathode (substrate side, shown at the bottom of the solder bumps) and the anode (die side, shown at the top side of the solder bump).

Materials Characterization

The C4 bumps were characterized using orientation imaging microscopy, scanning electron microscopy (SEM), and EBSD analysis. Optical images were used to select representative solder samples for further EBSD analysis. The selection was based on the severity of EM-induced degradation, noted by the extent of IMC formation; 23 solders from three packages were selected for detailed EBSD analysis.

The EBSD sample preparation included brief polishing with 1200 grit SiC paper to improve sample flatness. Additional polishing steps were done using 1-μm alumina followed by 0.3-μm alumina. The final polish was done with 0.02-μm colloidal silica. Finally, a carbon coating of approximately 15 Å and silver paint were applied to improve conductivity and reduce the charging effect.

Optical Analysis

We evaluated IMC growth using optical microscopy and assessed the degree of electromigration in these three samples. Images were captured for the entire row of solders at 500× magnification. Figure 3 shows an optical photomicrograph of sample 31. Individual solders were then selected for EBSD and texture analyses. C4 bumps (and their location in the FLI solder array) selected for the EBSD analysis are shown in Fig. 3. Note that in some cases IMCs are observed in the cathode side in our two-dimensional (2D) picture/cross-section of the representative three-dimensional (3D) solder bump. These cathode-side IMCs could be an extension of the IMC starting on the anode away from the plane of cross-section.

Scanning Electron Microscopy and Electron Backscatter Diffraction Analysis

EBSD maps of representative bumps were collected to quantify the grain orientation and its effect on electromigration. High-quality orientation images were developed for the selected bumps by indexing Kikuchi bands and poles. Reliability of the EBSD analysis was based on confidence index (CI) in excess of 0.7. (CI is a metric with values varying between 0 for low reliability and 1 for high reliability).

Pre- and postpolished images of the solder bumps were evaluated to confirm that the characteristics observed in the original EM-tested bumps were maintained during the EBSD sample preparation steps. Comparison of the optical photomicrograph with the SEM secondary electron (SE) image, shown in Fig. 4 for solder 31-2, validated the traceability of the features to the original optical photomicrographs.

To differentiate the solder material from the intermetallic layers and the copper traces, an elemental map was also obtained (Fig. 4c).

Orientation image maps (OIM) were developed using the EBSD data, in accordance with the SP2 approach used in Ref. 1. Recall that in SP2 the grain orientation is identified based on the angle that its [001] *c*-axis makes with the electron flow direction. Using this approach, grains oriented with their *c*-axis parallel to the electron flow (an angle of 0°)

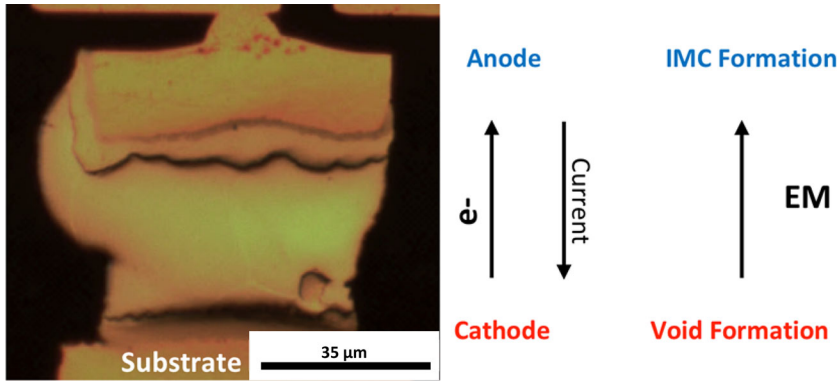

Fig. 2. Example solder bump (31-1) showing the electron flow direction in the solder. Electron flow direction is from the cathode side (bottom of solder joint) to anode side (top of solder joint). Diffusion of atoms occurs along the same direction as the electron flow, creating voids in the cathode side and IMC at the anode side.

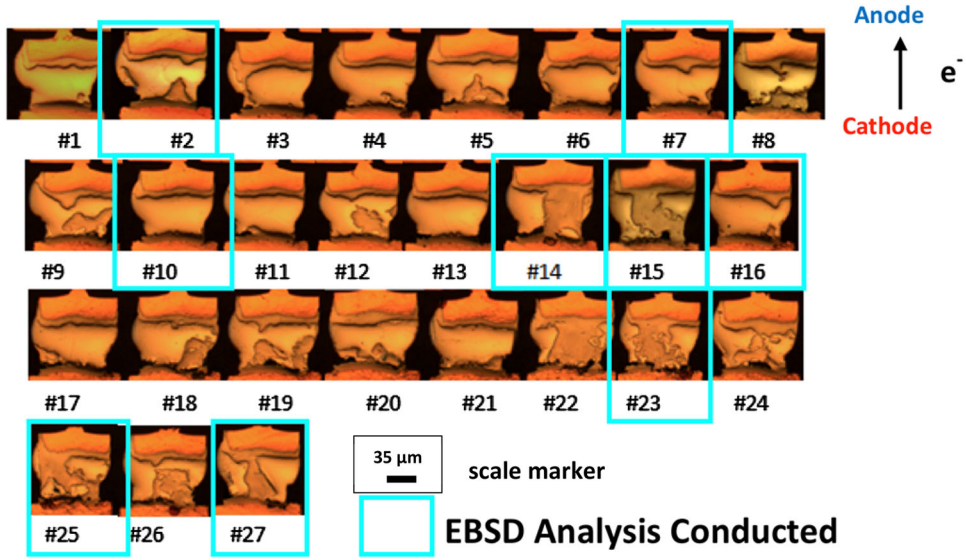

Fig. 3. Optical images for solder array in sample 31.

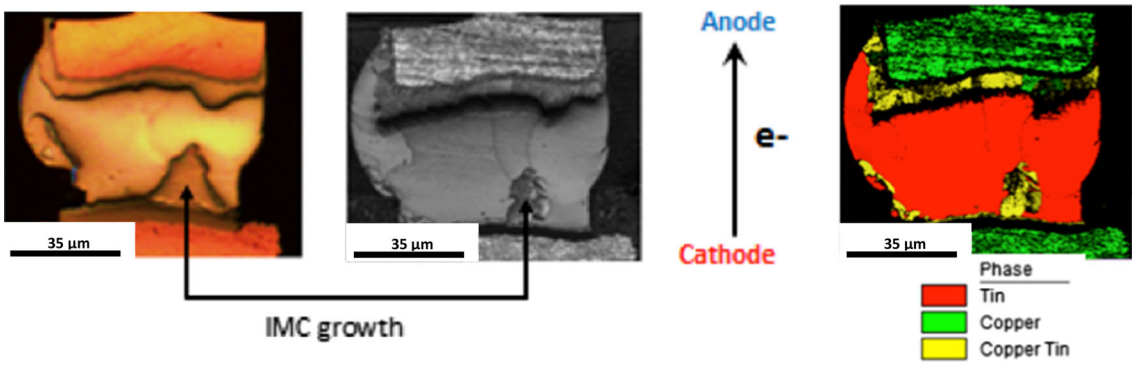

Fig. 4. Optical image (a), SE SEM image (b), and elemental map (c) of solder bump 31-2.

are represented by blue color, while grains with [001] perpendicular to the electron flow (an angle of 90°) are red. The EBSD map of solder 31-2 constructed using this SP2 approach is shown in Fig. 5. It should be noted that, in SP2, any and all grains with their *c*-axis perpendicular to the electron/current

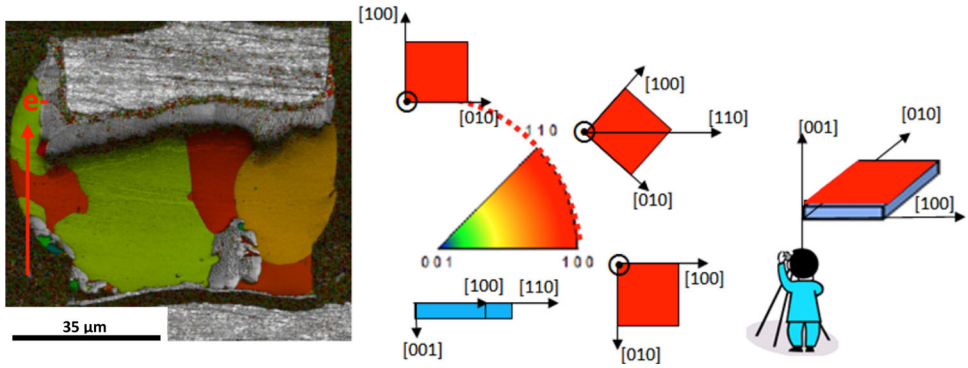

Fig. 5. SP2 map reflecting the [001] orientation of the noted grains w.r.t. the current flow direction (current crowding not considered).

flow (*c*-axis residing in the plane of the solder joint) appear as red. In other words, all [*uw*0]-oriented grains appear red in SP2 (Fig. 5).

RESULTS

OIM data for sample 31 are presented in Fig. 6. Figure 7 shows representative grain mapping data generated for HCP-structured IMC layers in selected solders. Key observations from the EBSD results are highlighted below. It should be noted that the reported results are based on data from two-dimensional cross-sections of the samples.

1. No significant IMC growth was noted within any single grain (e.g., no IMC region surrounded by same-colored grain);
2. The observed IMCs in all cases resided at grain boundaries, neighboring grains with different orientations on two sides;
3. Low-angle grain boundaries (adjacent grains with similar orientations) did not show any IMC (e.g., solders 31-7 and 31-10);
4. Solders 31-15, 36-10, and 39-26 were the only solders with blue grains (grain orientation most susceptible to EM). Only 3 out of 23 solders studied via EBSD contained [001] grain orientation along the current flow direction. However, green grains were more abundant;
5. The majority of IMC grains had preferred orientation with the basal plane (close-packed plane of HCP structure) perpendicular to the electron flow;
6. IMC-rich regions were noted on both the die (anode) and package (cathode) sides. Since IMC is expected to form on the anode side, it is theorized that the IMCs in the package/cathode side are the extension of IMC formed in the die/anode side away from the plane of view. Future 3D tomography is recommended to validate this hypothesis.

DISCUSSION

One of the objectives of this study is to quantify the reported "preferred" grain orientation effect on EM in actual C4 bumps. OIM of 23 EM-tested C4 solder bumps in this study did not show any significant preferential IMC growth in individual grains to validate "preferred" grain orientation promoting EM and IMC formation during ALT (see point 1 in "Results" section).

The critical finding of this study is the effect of grain boundary misorientation angle on electromigration in C4 bumps. A direct correlation between the severity of EM and grain boundary misorientation angle was noted (see point 2 in "Results" section).

The number of grains associated with the most EM-susceptible orientation (blue grains) was very limited. The authors propose further studies to investigate: (i) low probability for nucleation/growth of such grains at reflow, and (ii) consumption of such grains during the EM tests.

Detailed discussion on the observed behaviors is provided in the following sections.

Effect of Crystal Packing on Electromigration in Single-Crystal Solders

Using planar density calculations, we can explain the observed orientation effect on EM in single-crystal solder. Table I shows that, for single crystals and in the absence of defects (such as grain boundary and dislocation), a grain oriented with its least-packed plane (001) aligned with the IMC growth front will have a more open structure for lattice diffusion and migrating atoms, hence facilitating EM and IMC growth. Interestingly, this high EM grain orientation is that represented by the "blue" designation, hence explaining the reported "preferred" orientation effects discussed previously.

Effect of Grain Misorientation on IMC Formation and Electromigration

This study revealed the importance of grain boundary for electromigration. In this section, the effect of grain boundary misorientation angle on the extent of IMC growth is quantified. The misorientation angle data were determined via EBSD analysis

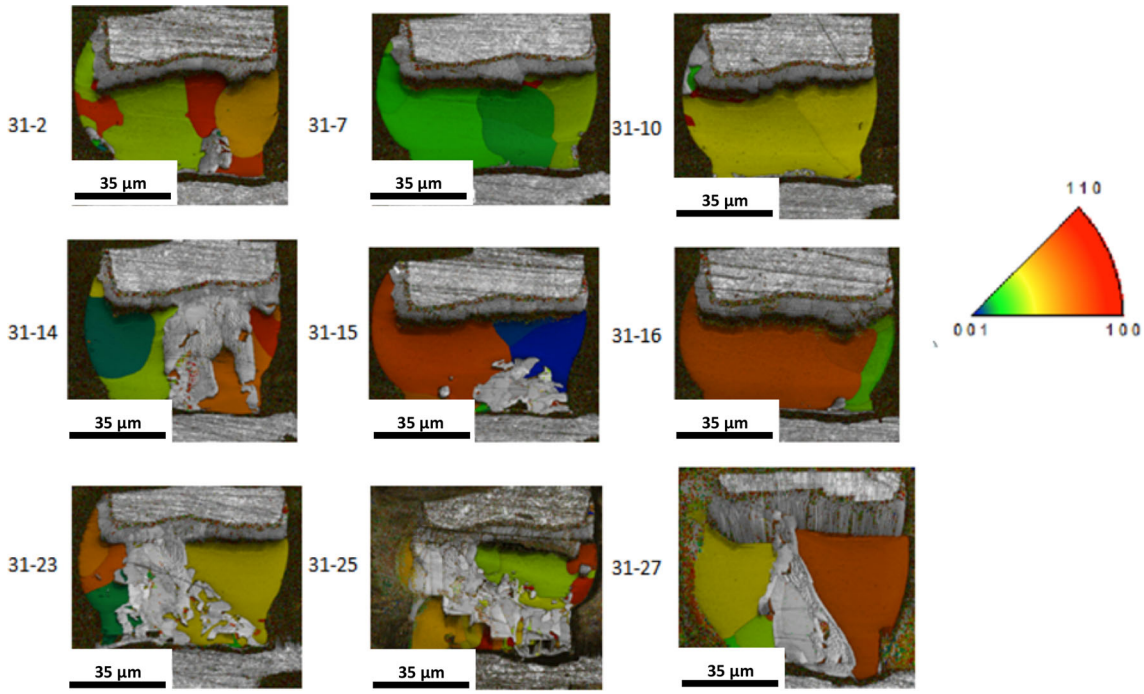

Fig. 6. SP2 maps for selected solder bumps in sample 31.

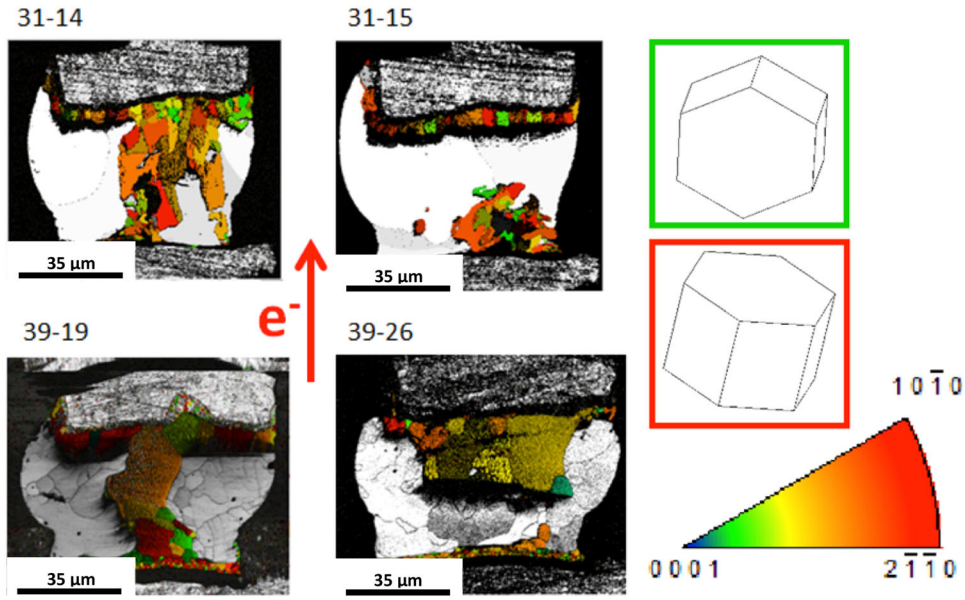

Fig. 7. Representative solders showing HCP crystal orientation w.r.t. basal plane [0001]. Most IMC grains have their close-packed basal planes perpendicular to the electron flow direction.

Table I. Correlation between crystal planar density and reported EM in single-crystal solder

Orientation	Color	Planar Density (atoms/nm^2)	Electromigration
(001)	Blue	2.9	High
(011) and (101)	Green	5.2	Medium–high
(110)	Red	7.6	Low
(100) and (010)	Red	9.7	Low

(see Fig. 8, showing grain boundary misorientation angles in sample 31-2).

The IMC fraction in bulk solder was measured using OIM software on the elemental maps. These data were then plotted against the corresponding misorientation angles. The data clearly show that the large misorientation angles (15° to 53°) display the most IMC formation, while the solders with low-angle grain boundaries exhibit minimal IMC growth (Fig. 9). This behavior is expected, as the increase in misorientation angle provides a more open site for atom migration and a more suitable sink for IMC during EM testing.

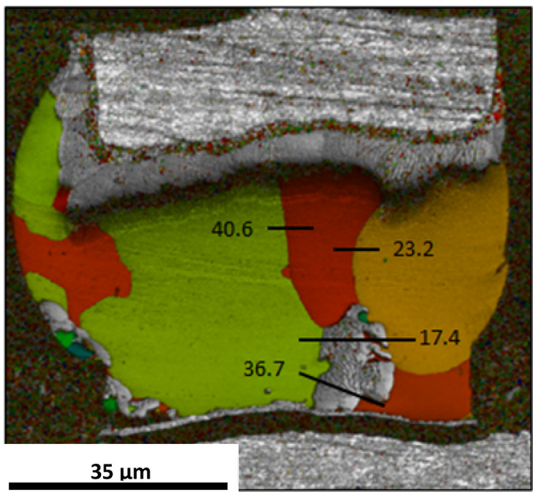

Fig. 8. Misorientation angles measured between different grains in solder 31-2.

The scatter in the data in Fig. 9 is believed to be associated with the fact that %IMC values were based on measurement from 2D cross-sections of solders. IMC data using 3D tomography are recommended for improved accuracy. As mentioned above, the IMC data denoted "cathode side" are believed to be associated with extension of 3D IMC originating on the "anode side" away from the cross-sectioned plane of view.

Our data clearly reveal that the majority of the IMC growth evolved from grain boundaries, and the grain boundary diffusion effect dominates the EM process and atom migration. This effect of misorientation angle on diffusion rate is similar to the behavior shown previously for other materials (Fig. 10). A large misorientation angle between adjacent grains promotes a higher rate of diffusion along the boundary. As the misorientation drops to zero, the diffusion coefficient in the boundary drops to that of lattice diffusion (Fig. 10a).[12] The misorientation angle's effect on diffusivity is due to the fact that the grain boundary surface energy (γ_G) is influenced by this angle (Fig. 10b).[13] The EM trend noted in Fig. 9 correlates well with the trend of the misorientation angle's effect on the grain boundary surface energy and the diffusion rate, shown in Fig. 10a and b, respectively.

Solder diffusivity data were evaluated for further analysis of these observed behaviors. Table II summarizes the reported data.[1,11,14] Diffusivity values reported by Dyson et al.[11] and Kinney et al.[1] correspond to lattice diffusion since the solder samples used in their studies were primarily single crystals, and the IMC growth was observed within the grain. The effect of grain orientation on lattice diffusion is reflected in the $D_{lattice}$ column in this table. These

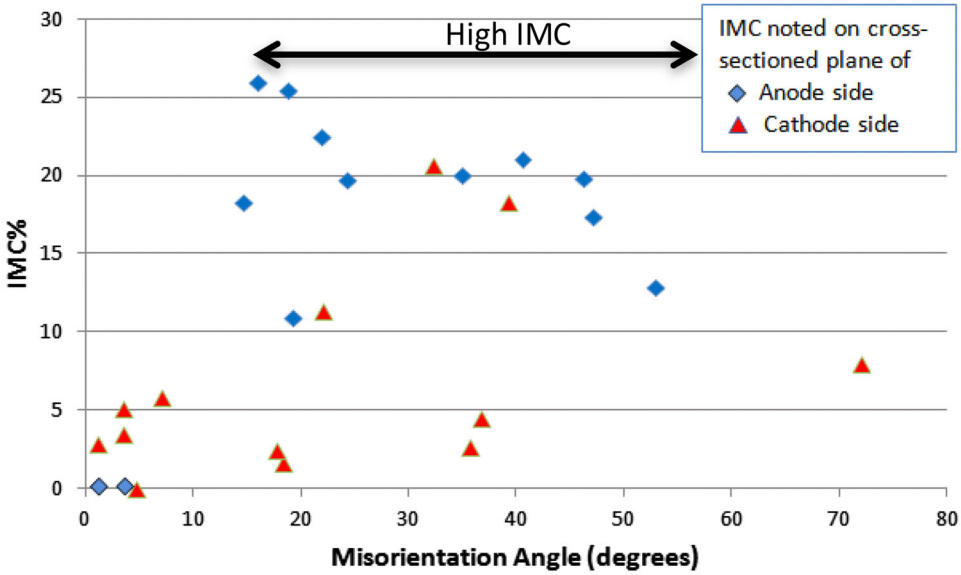

Fig. 9. Effect of grain boundary misorientation on IMC. Note that %IMC data are based on 2D cross-sections; IMC data using 3D tomography are recommended for improved accuracy. The IMC data denoted "cathode side" are believed to be associated with extension of 3D IMC originating on the anode side away from the cross-sectioned plane of view.

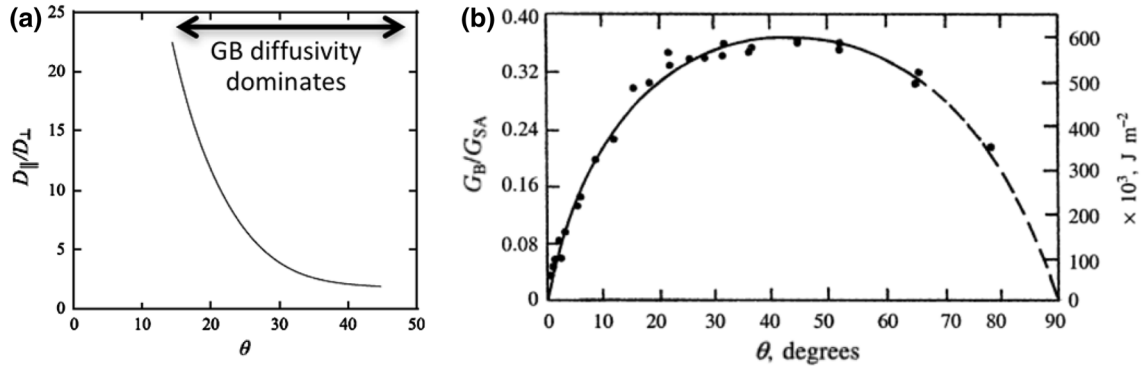

Fig. 10. Effect of grain boundary misorientation angle on (a) diffusion of atoms along grain boundaries (normalized to lattice diffusion), and (b) on grain boundary energy (Cu at 1338 K, normalized to free surface energy γ_S).

Table II. Diffusivity ratios (using data from Refs. 1, 11, 14) comparing lattice and grain boundary diffusivities

Study	$D_{lattice}$	D_{gb}
Dyson et al.[11]	$\frac{D_{\parallel c}}{D_{\perp c}} = 500$	–
Kinney et al.[1]	$\frac{D_{\parallel c}}{D_{\perp c}} = 65$	–
Li and Basaran[14]	–	$\frac{D_{gb}}{D_l} > 10^6$

data show a factor of 65× to 500× higher lattice diffusion along the *c*-axis compared with that perpendicular to the *c*-axis.[1,11] The large scatter in the reported lattice diffusivity ratio data could be associated with differences in the secondary orientation w.r.t. the current trajectory in the two studies (all directions in the {001} plane being perpendicular to the *c*-axis).

The grain boundary diffusivity data reported by Li and Basaran[14] are shown in the D_{gb} column of Table II. A significantly higher diffusivity along the grain boundary (six orders of magnitude) compared with the lattice diffusivity is reported in Ref. 11.

Based on these data,[1,11,14] one would expect the GB diffusion to be at least three orders of magnitude higher than lattice diffusion along any direction within the grain. Therefore, for multigrained solder, GB diffusion will be the dominant mechanism for EM. This could explain why we did not observe the individual grain orientation effect as observed by Kinney et al. in their single-crystal solder study.

Low Occurrence of EM-Susceptible Grains in C4 Array Bumps

The scarcity of the most EM-susceptible (blue) grains in this study was puzzling. The authors propose further studies and EBSD analysis of EOL samples to investigate the possibility of complete consumption of such grains during the EM tests and/or potential preferential grain growth resulting upon solidification from reflow (i.e., lower probability of blue grain nucleation and growth). The statistical distribution of the blue grains in EOL and EM-tested solders should provide valuable insight in validating these hypotheses. Such study will test the grain consumption hypothesis and also shed light on potential preferential stress-assisted grain nucleation and growth occurring during solder solidification. Variation in CTE-induced thermal stresses developed during reflow at different C4 solder locations [with varying distance from neutral points (DNP)] may impact grain nucleation in these solders.

CONCLUSIONS

Electromigration has proven to be a critical reliability issue in Pb-free solder joints. The high current densities in miniaturized solder bumps, the temperatures to which the bumps are exposed during processing and application of microelectronic systems, solder composition, microstructure, and grain orientation greatly impact EM in these interconnects. The effect of microstructure and orientation on electromigration in C4 bumps was the main focus in this study, and the current density, temperature, and solder composition were similar for all samples tested.

This study showed a significant effect of grain boundary misorientation angle on electromigration in C4 bumps. For the ALT duration of this study, minimal/no EM was observed on any single solder grain, and the "preferred" orientation effect reported by others was not evident in C4 bumps. Grain orientations in C4 bumps varied significantly, ranging from the [001] direction of the grain oriented along the current flow (blue grains) to that perpendicular to the current flow (reflected as red grains). A statistically lower number of grains with *c*-axis parallel to the e^- flow, associated with the highest lattice diffusivity, was present in the 23 C4 bumps studied via EBSD compared with other grain orientations.

The amount of IMC on the cross-sectioned surface of EM-tested solders was determined. Extensive IMC formation was noted on some of the EM-tested

C4 solder bumps (in excess of 40% IMC layers consuming the solder in samples 31-25 and 39-22).

EBSD analysis was used in determining the grain orientations, as well as grain boundary misorientation angles. High-angle grain boundaries were noted to be the most dominant path for diffusion and IMC formation in C4 bumps. Transgranular IMC and the lattice orientation effect reported by others[1] under idealized single-crystal testing were not observed during the course of this study. The grain orientation effect reported by other investigators and the observations from this study were explained using lattice and grain boundary diffusivity data. The observed trend for the effect of grain boundary misorientation on EM and IMC formation was explained through the grain boundary surface energy and diffusion data found in literature.

Even though an individual grain orientation effect on EM was not evident in this study, we do expect the anisotropic properties in EM to act for single-grained BCT tin solder, in the absence of grain boundary.

FUTURE WORK

The extent of IMC formation and the severity of EM in C4 bumps should be further quantified using 3D x-ray tomography and/or serial sectioning in conjunction with EBSD analysis. This approach will provide valuable data on the IMC distribution and the misorientation angles involved throughout the solder volume. Such analysis should be helpful in explaining the cathode-side IMCs noted on the 2D cross-sectional views in this study. In addition, EBSD analysis of EOL samples is recommended to obtain statistical data on the number of blue grains in untested conditions. This will provide information on whether blue grains are consumed during EM testing and/or whether package processing influences bump grain orientation.

Electromigration testing of controlled bicrystal solder samples, with various degrees of misorientation angles, is recommended in developing a more accurate analytical model.

Solder alloy development and processing methods to control the grain boundary diffusivity and grain orientation should be further investigated. Addition of alloying elements to reduce grain boundary diffusion, and developing a solidification process to achieve preferred single-crystal solder orientation (and/or limiting secondary grain formation to low-angle boundaries), are potential improvement methods in managing electromigration.

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