Journal of ELECTRONIC MATERIALS, Vol. 37, No. 10, 2008
DOI: 10.1007/s11664-008-0513-5
© 2008 TMS
Regular Issue Paper

Air-Gaps for High-Performance On-Chip Interconnect Part II: Modeling, Fabrication, and Characterization

SEONGHO PARK,[1] SUE ANN BIDSTRUP ALLEN,[1] and PAUL A. KOHL[1,2]

1.—School of Chemical and Biomolecular Engineering, Georgia Institute of Technology, 311 Ferst Drive, N.W., Atlanta, GA 30332-0100, USA. 2.—e-mail: paul.kohl@chbe.gatech.edu

Air-gaps are the ultimate low-*k* material in microelectronics due to air having a low dielectric constant close to 1.0. The interconnect capacitance can further be reduced by extending the air-gaps into the interlayer dielectric region to reduce the fringing electric field. An electrostatic model (200 nm half-pitch interconnect with an aspect ratio of 2.0), was used to evaluate the dielectric properties of the air-gap structures. The incorporation of air-gaps into the intrametal dielectric region reduced the capacitance by 39% compared with SiO_2. Extending the air-gap 100 nm into the top and bottom interlayer SiO_2 region lowered the capacitance by 49%. The ability to fabricate air-gaps and 'extended air-gaps' was demonstrated, and the capacitance decrease was experimentally verified. Cu/air-gap and extended Cu/air-gap interconnect structures were fabricated using high-modulus tetracyclododecene (TD)-based sacrificial polymer. The aspect ratio of the air-gap was 1.8 and the air-gap was extended 80 nm and 100 nm into the top and bottom interlevel SiO_2 region, respectively. The measured effective dielectric constant (k_{eff}) of the Cu/air-gap and the extended Cu/air-gap structures with SiO_2 interlevel dielectric was 2.42 and 2.17, respectively. The effect of moisture uptake within the extended Cu/air-gap structure was investigated. As the relative humidity increased from 4% to 92%, the k_{eff} increased by 7%. Hexamethyldisilazane was used to remove adsorbed moisture and create a hydrophobic termination within the air-cavities, which lowered the effect of humidity on the k_{eff}. A dual Damascene air-gap and extended air-gap fabrication processes were proposed and the challenges of using a sacrificial polymer placeholder approach to form air-cavities are compared to other integration approaches of dual Damascene air-gap.

Key words: Air-gap, low-*k*, Damascene

INTRODUCTION

The performance of semiconductor devices has improved due to scaling of transistor parameters.[1] However, with the shrinkage of the minimum feature size, the interconnect structure became multilayered, complex, and smaller in size. Thus, the performance of interconnect has deteriorated and interconnect challenges such as resistance–capacitance (RC) delay, crosstalk noise, and power dissipation have become barriers to the performance of semiconductor devices.

Integrated circuit (IC) interconnects are composed of multilevel metal lines to transport signals and power, and dielectric materials to insulate adjacent metal lines. The performance of the interconnect is determined by the properties of the metal and dielectric materials, and their geometry. The interconnect geometry is a function of the design rules. The dual Damascene copper metallization processes was developed in 1997[2] in order to incorporate copper into the interconnect structure. Copper has lower resistance, higher allowed current

(Received December 23, 2007; accepted June 10, 2008; published online July 25, 2008)

density, and increased scalability in comparison with aluminum.[2–4] Numerous low-dielectric-constant (low-k) materials, including fluorine-doped silicon dioxide (F-SiO_2), polymers, spin-on glasses, foams,[5] plasma-enhanced chemical vapor deposition (PECVD) SiOC,[6] PECVD SiCOH,[7] and air-gaps[8–12] have been developed to decrease the interconnect capacitance and for integration into a Damascene process flow. The incorporation of air, in the form of air-gaps, is the lowest dielectric constant available.

The concept of air-gap integration as an intrametal dielectric material was first introduced by Havemann and Jeng[13] using the removal of a spin-coated disposable solid material (e.g., photoresist) between the metal lines. The metal lines were formed by wet etching, and the disposable solid material was spin-coated. A porous oxide layer was then deposited, and the disposable solid material was removed by wet etching or oxidation (using oxygen from the air) through the porous material, resulting in the formation of an air-gap between the metal lines, one layer at a time. The metallization-first process is generally not preferred over the dielectric-first process because it is easier to fill high-aspect-ratio voids (height-to-width) with metal than to fill voids with dielectric. Thus, numerous methods to integrate air-gaps into a dual Damascene process were developed and are categorized into three approaches, as shown in Fig. 1 and Table I.

The first approach is to use a thermally decomposable sacrificial polymer as a temporary placeholder in between metal lines, as shown in Fig. 1a. After finishing the chemical mechanical polishing (or planarization) (CMP) step of the dual Damascene process, a second interlayer dielectric is deposited, which encapsulates the temporary trench patterns of the sacrificial material. Then, the sacrificial polymer is thermally decomposed, and the gaseous byproducts diffuse out through the second interlevel dielectric layer, while air diffuses in, forming an air-cavity. Two lithography steps are needed for via and trench patterning, and three additional steps (spin-coating, etching, and decomposition of sacrificial polymers) were used beyond those required for traditional dual Damascene processes.[8,9] Daamen et al. used a spin-on thermally degradable polymer and an embedded via-first dual Damascene air-gap process.[10] The number of lithography steps is two (via and trench patterning), and no additional process steps are needed compared with the dual Damascene structure due to the embedded via-first process.

The second approach is the removal of the sacrificial material by wet etching, as disclosed by Gosset et al.[11] and shown in Fig. 1b. After finishing a CMP step of a dual Damascene process and deposition of a SiC capping layer, an additional lithography step is used to open an etching solution pathway in the SiC capping layer. A sacrificial layer of SiO_2 between the copper lines is dissolved using

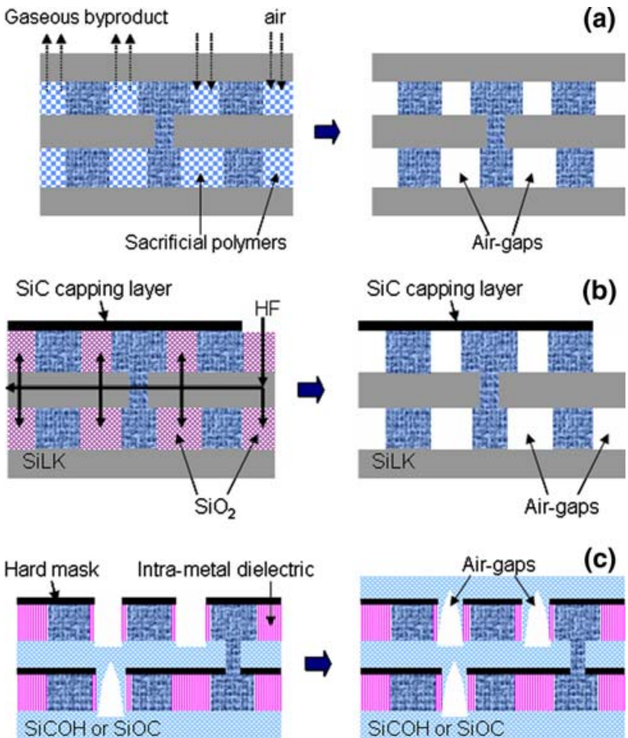


Fig. 1. The three different integration approaches of dual Damascene air-gaps: (a) thermal decomposition of the sacrificial polymer;[8,9,10] (b) wet etching of the SiO_2 intrametal dielectric;[11] and (c) etch back of the intrametal dielectric and nonconformal deposition of the interlayer dielectric.[12,13]

hydrofluoric acid introduced through the physical pathway, leaving air-cavities in the intrametal dielectric regions. The organic dielectric SiLK (Dow Chemical) as an interlayer dielectric does not dissolve in the hydrofluoric acid, leaving it intact as the overcoat dielectric. Three lithography steps are needed for via, trench, and SiC etching (creating the hydrofluoric acid pathway). Four additional process steps are needed compared with the dual Damascene process, including lithography and etching of the SiC capping layer to open the hydrofluoric acid pathway.

The formation of air-gaps during nonconformal CVD deposition of the interlayer dielectric material is the third approach.[12] After finishing a CMP step of a dual Damascene process and depositing the hard mask, an additional lithography step is used to etch back the intrametal dielectric material in a desired region where the air-gaps are formed. The air-cavities are created during the nonconformal CVD deposition of the interlevel dielectric, which pinches off the top portion of the dielectric layer,[14,15] as shown in Fig. 1c. Three lithography steps are needed for via, trench, and selective etch back of the intrametal dielectric. Four additional process steps are needed compared with the dual Damascene process, including selective etching of the intrametal dielectric and CMP of the upper interlevel dielectric layer. Recently, a manufacturing-worthy

Table I. Summary of the Different Approaches for the Integration of Air-Gaps in Terms of the Number of Lithographic and Additional Process Steps Compared with the Conventional Dual Damascene Process

Air-Gap Integration Approach	Company	Number of Lithography	Number of Additional Steps Compared with Dual Damascene
Thermal decomposition of sacrificial polymer	GeorgiaTech[8,9]	2	3
	NXP Semiconductors and DOW[10]	2	0
Removal of sacrificial materials by wet etching	STMicroelectronics, CEA, LTM/CNRS, NXP Semiconductors[11]	3	4
Nonconformal deposition of interlayer dielectric	Matsushita, Panasonic, Renesas Tech.[12]	3	4∼6
	IBM[13]	3	8

dual Damascene air-gap processes using nonconformal deposition of the SiCOH interlayer dielectric material has been disclosed by IBM.[2] In this approach, the SiCOH dielectric was used as the intrametal and interlayer dielectric materials in the dual Damascene process to fully take advantage of the low dielectric constant of SiCOH. Following the dual Damascene process, an additional lithography step was used to etch back the SiCOH intrametal dielectric material in order to incorporate air-cavities in the desired areas. After the etch back of the SiCOH intrametal dielectric, SiCOH as a top interlayer dielectric is nonconformally deposited, forming air-gaps in between the metal lines. In this approach, three lithography steps are used and eight additional process steps are needed compared with the dual Damascene process. The additional process steps include a lithography step for the etch back of the SiCOH dielectric between the Cu lines and hard mask in the desired interconnect regions, and deposition and CMP steps involving the top SiCOH interlayer dielectric.

In this study, a single-layer Cu/air-gap structure using a thermally decomposable sacrificial polymer placeholder is investigated. The study includes extending the air-gap into the interlayer dielectric region, further lowering the effective dielectric constant. The effect of moisture uptake on the Cu/air-gap structure has also been explored.

EXPERIMENTAL

Air-gap structures and structures extending the air cavity into the interlayer dielectric were fabricated, as shown in Figs. 2 and 3. The purpose of the fabrication is to demonstrate the ability to fabricate the air-gaps and extended air-gaps using the high-modulus tetracyclododecene (TD)-based sacrificial polymer and to experimentally verify the advantage of integration of air-gaps and extended air-gaps into the intrametal dielectric region on the interconnect capacitance. Thus, a lift-off Cu metallization process was used in all the processes. Patterns of polymethyl-methacrylate (PMMA) positive tone electron-beam resist were developed using a methyl isobutyl ketone and isopropyl alcohol (IPA), 1:1 volume ratio, followed by an IPA rinse for 1 min. Electron-beam exposures were performed by using a JEOL JBX-9300FS electron-beam lithography system. The accelerating voltage of the electron beam was 100 kV and the spot size was 4 nm. The beam current was 2 nA and the electron dose was 500 $\mu C/cm^2$. After development, the height and width of PMMA patterns was 540 nm and 200 nm, respectively. A 380 nm Cu layer was deposited by using a filament evaporator (PVD75, Kurt J. Lesker Company) at a deposition rate of 2 Å/s. During the removal of the PMMA electron-beam resist in *N*-methyl-2-pyrrolidone (NMP) at 70°C, the Cu lines on top of the PMMA electron-beam resist patterns were also removed, leaving the Cu lines in between the PMMA electron-beam resist patterns, as shown in Fig. 2a. The Cu lines were annealed at 450°C for 2 h in a nitrogen atmosphere. The aspect ratio of the Cu lines was 1.8:1 (H:W, 380 nm in height and 210 nm in width). The integration of air-gaps with the dual Damascene processes will be proposed in the discussion section.

Following Cu metallization, the tetracyclododecene-based sacrificial polymer (TD) was spin-coated and etched to remove the excess material (Fig. 2b). After hard bake of the TD-based sacrificial polymer at 300°C for 1 h in nitrogen, a PECVD SiO_2 dielectric layer was deposited (Fig. 2c). The sacrificial polymer was thermally decomposed in the furnace, resulting in the formation of air-gaps as shown in Fig. 2d. Before starting the decomposition heating, nitrogen gas (4 L/min) was used to purge the furnace for 30 min to remove residual oxygen. During the heating cycle, the nitrogen flow rate was decreased to 2 L/min. During thermal decomposition, the sacrificial polymer was decomposed to form gaseous by-products. The furnace ramp rate was adjusted so that the polymer decomposition rate was 0.5 wt.%/min to avoid excess pressure build-up during decomposition.[16,17] Table II shows the

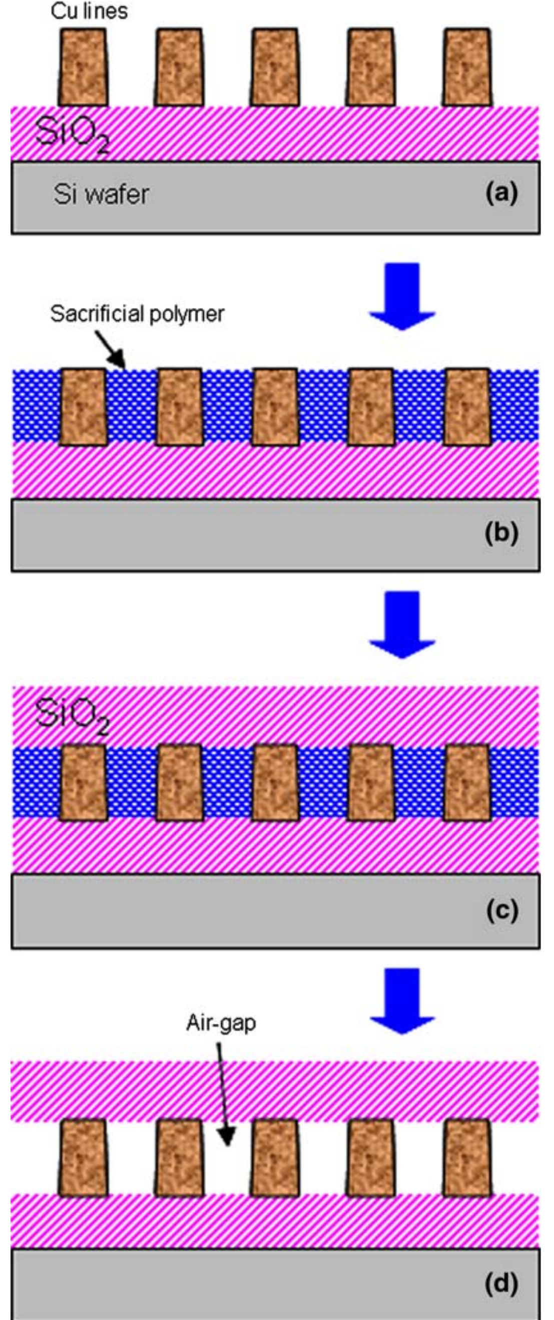


Fig. 2. The fabrication processes flow for Cu/air-gaps interconnect structures using the Cu-metallization-first process.

temperature profile during the thermal decomposition step. The half-pitch of the Cu/air-gap interconnect was 200 nm, and the height of the Cu metal lines was 380 nm. For the purpose of comparison, PECVD Cu/SiO_2 interconnect structures were also fabricated.

The fabrication process for the extended Cu/air-gap structures is shown in Fig. 3. After Cu metallization using the lift-off process (Fig. 3a), the lower SiO_2 layer was etched by reactive ion etching (RIE) to extend air-gaps into the bottom dielectric layer as shown in Fig. 3b. The Cu lines were used as a hard mask, and the etched depth of SiO_2 was 100 nm. The TD-based polymer was spin-coated on the Cu lines, and a thin PECVD SiO_2 layer was deposited (Fig. 3c) and used as a hard mask in the following dry etch step. The sacrificial polymer on top of the Cu lines was removed by electron-beam lithography, resulting in the extension of air-gaps into the upper SiO_2 layer as shown in Fig. 3d. The extension of the air-gap into the upper SiO_2 dielectric layer was approximately 80 nm, as determined by the thickness of spin-coated sacrificial polymer on top of the Cu lines. The next step was the deposition of the upper SiO_2 layer (Fig. 3e) and the TD-based polymer between Cu lines was thermally decomposed as shown in Fig. 3f. The decomposition process conditions were the same as those for the fabrication of Cu/air-gap structures.

In the fabrication of Cu/air-gap and extended Cu/air-gap structures, PECVD SiO_2 was used as the interlayer dielectric. The effective dielectric constant of Cu/air-gap and extended Cu/air-gap structure were evaluated by comparing the measured capacitances to those with SiO_2. The dielectric constant of PECVD SiO_2 was measured by making parallel-plate capacitors. The area of the Cu electrodes was 1400 μm × 1400 μm, and the thickness of the PECVD SiO_2 dielectric was 1 μm. The calculated capacitance due to the fringing field was small (0.014%) so that the parallel capacitor was considered an ideal parallel capacitor. The relative dielectric constant of PECVD SiO_2 was calculated by measuring a capacitance of the parallel capacitor and Eq. 1,

$$C = \varepsilon_0 \varepsilon_r \cdot \frac{A}{d}, \tag{1}$$

where C is the capacitance, ε_0 is the permittivity of free space, ε_r is the relative dielectric constant, A is the electrode area, and d is the distance between the two electrodes.

Comb structures of Cu/SiO_2, Cu/air-gap, and extended Cu/air-gap interconnects were fabricated, and the capacitances of each interconnect structure were measured by using a Keithley 590 CV analyzer and Cascade Microtech Alessi REL-4800 probe station at room temperature. The capacitance of the devices was measured at a frequency of 1 MHz with a voltage sweep from −1 V to 1 V.

The moisture uptake of the extended Cu/air-gap structures was investigated by changing the relative humidity within the probe station enclosure. In order to stabilize the humidity inside the probe station enclosure and to achieve a steady-state measurement, a comb structure device was exposed to each relative humidity (RH) for 1 h before the capacitance was measured. Hexamethyl disilazane (HMDS) treatment was carried out on a vacuum line to remove moisture and make the comb structure device hydrophobic. The device was evacuated using a turbomolecular pump for 1 h. In addition, a separate vessel which contained HMDS was

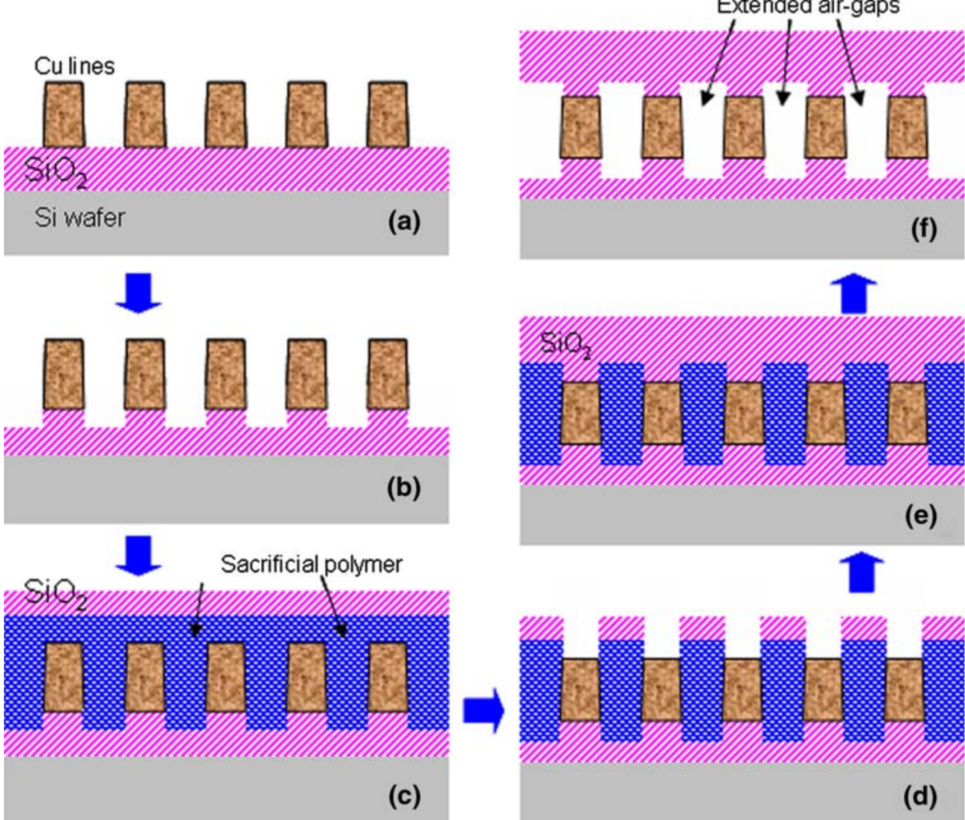


Fig. 3. The fabrication processes flow for extended Cu/air-gaps interconnect structures using the Cu-metallization-first process.

Table II. Temperature Profile for the Decomposition of Sacrificial Polymer with 0.5 wt.%/min

	Initial Temp. (°C)	Final Temp. (°C)	Time (min)	Ramp Rate (°C/min)
Step 1	20	300	150	2.0
Step 2	300	350	50	1.0
Step 3	350	385	205	0.17
Step 4	385	395	30	0.33
Step 5	395	405	20	0.50
Step 6	405	415	13	0.77
Step 7	415	430	10	1.50
Step 8	430	450	4	5.00
Step 9	450	450	120	0.00

evacuated to remove the air inside the vessel so that only HMDS gas existed in the head space. After the evacuation for 1 h, the device was exposed to HMDS vapor for 1 h.

RESULTS

The integration of air-gaps as the intrametal dielectric and extension of the air-gap into the top and bottom interlevel dielectric layer was investigated by electrostatic modeling. Figure 4 shows the geometry modeled using ANSYS software. The width and aspect ratio (H:W) of the Cu lines were fixed at 200 nm and 2.0, respectively. The modeled domain of 10 μm $\times$ 10 μm accounted for more than 99.5% of the electric fringing field. In the case of the extended air-gap, the height of the air-gap was extended by 100 nm into the top and bottom SiO_2 interlevel dielectric layers.

The contour plots of the electric flux density (D), the capacitance per unit length, and k_{eff} of Cu/SiO_2, Cu/air-gaps, and extended Cu/air-gaps interconnects are summarized in Table III. From the comparison of the electric flux density distribution in the contour plots, it can be observed that the incorporation of the air-gaps decreases the electric flux density in the intrametal dielectric region between the Cu lines compared to the case where

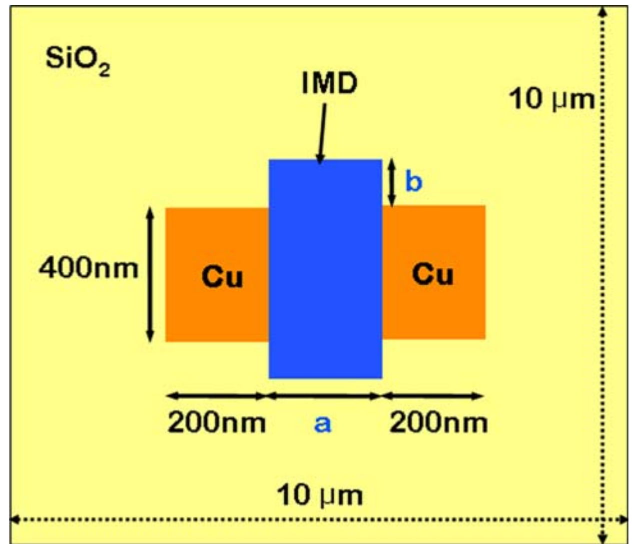
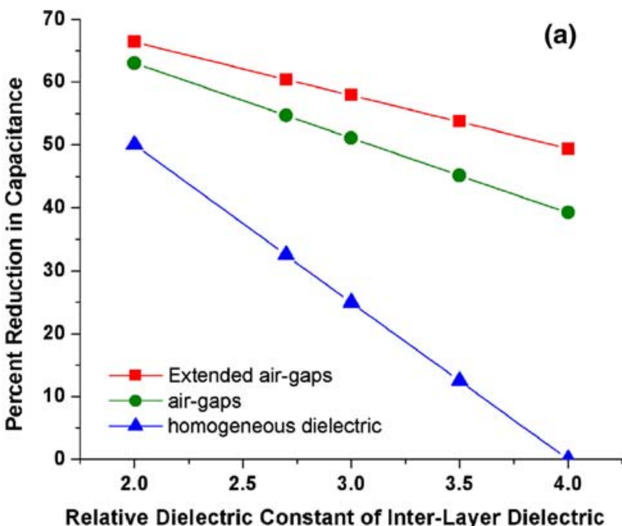


Fig. 4. The electrostatic modeling geometry of the interconnect.

SiO_2 is placed between the copper lines. However, the electric flux density is still high at the corners of the Cu lines due to the fringing field into the interlayer dielectric. The effective dielectric constant can be decreased by extending the air-gap into the interlevel dielectric layer. This is shown in the extended Cu/air-gaps interconnect structure. The air-gaps and extended air-gaps lower capacitance by 39% and 49%, respectively, compared with SiO_2. The k_{eff} of the air-gap structure was 2.45. Extending the air cavity 100 nm into the interlayer dielectric lowered k_{eff} to 2.01.

In Fig. 5, the effect of the interlayer dielectric constant on k_{eff} is shown. The geometry for the model was the same as that shown in Fig. 4. The width and aspect ratio of the Cu lines and air-gaps were 200 nm and 2.0, respectively. In the case of the extended air-gap, the height of the air cavity was



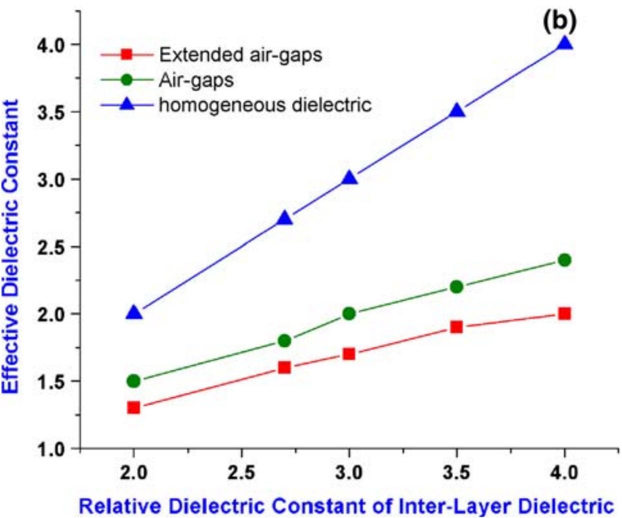
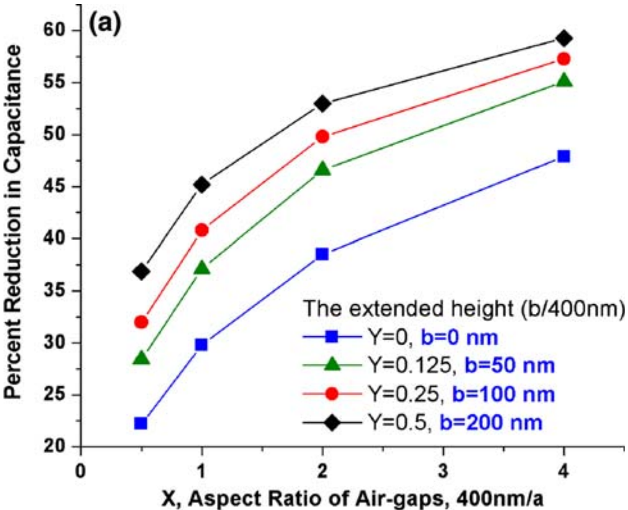


Fig. 5. The effect of the dielectric constants of the interlayer dielectric materials on (a) the percentage reduction in capacitance and (b) the effective dielectric constant, k_{eff}.

Table III. Summary of the Electric Flux Density, Capacitance, and k_{eff} of Homogeneous Cu/SiO_2, Cu/Air-Gaps, and Extended Cu/Air-Gaps Interconnects

	SiO_2 Dielectric	Air-Gaps	Extended Air-Gaps
Electric flux density (D)			
Capacitance (C) (pF/m)	138.2	84.8	69.5
Reduction in capacitance (%)	0	39	49
Effective k (k_{eff})	4.0	2.45	2.01



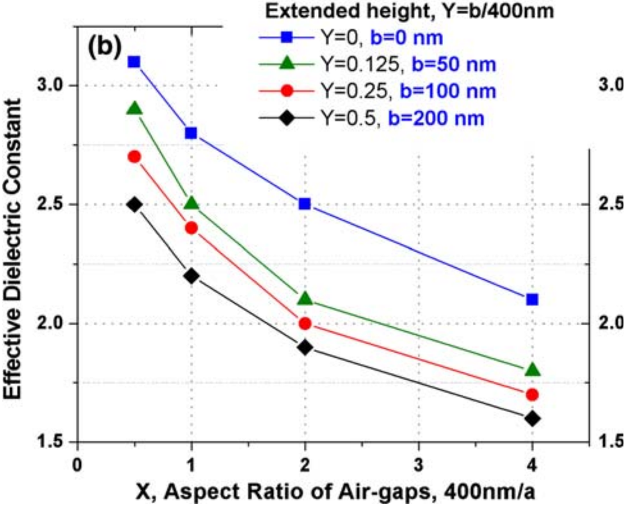


Fig. 6. The effect of the space between the metal lines and extended height of air-gaps on (a) the percentage reduction in capacitance and (b) the effective dielectric constant, k_{eff}.

extended 100 nm into the top and bottom of the interlayer dielectric. As the dielectric constant of the interlayer dielectric decreased, the effective dielectric constant of the interconnect structures decreased. For example, if a low-k dielectric were used (ε_r = 2.7) instead of SiO_2 (ε_r = 4.0), the capacitance decreased 54.7% compared with the SiO_2 case (no air-gap). The effective dielectric constant decreased from 4.0 for SiO_2 to 1.8. In the case of an extended air-gap with a very low interlayer dielectric (ε_r = 2.0), k_{eff} was reduced to 1.3, which exceeds the needs of the 22 nm technology node.[1]

The effect of extending the height of the air-gap and the space between the metal lines (the aspect ratio of the air-gap) on the interconnect capacitance and k_{eff} were evaluated, as shown in Fig. 6. As defined in Fig. 4, the parameter a is the width of an air-gap and the aspect ratio of dielectric area, X, was defined as 400 nm/a. As X becomes larger, the space between the Cu lines becomes narrower. The parameter b is the extension height of an air-gap into the top and bottom interlayer dielectric. The ratio of the extension height of the air-gap to the height of the Cu lines, Y, was defined as b/400 nm. Therefore, Y becomes larger as the air-gap extends further into the interlayer dielectric. As the space between the copper lines decreases (X becomes larger), the effective dielectric constant decreases, as shown in Fig. 6b. This is because a decrease in the space between the Cu metal lines increases the intensity of the electric field (E) and the electric flux density (D). However, the electric flux density (D) is a function of the dielectric constant of the insulator and can be further reduced by locating air-cavities in the space between the metal lines. This means that the integration of an air cavity into the intrametal dielectric region has a greater effect for higher-aspect-ratio interconnect structures. Extending the air-gap into the interlayer dielectric region reduces the fringing field, resulting in an additional reduction in the capacitance and k_{eff}. The capacitance at an aspect ratio of $X = 2.0$ (a = 200 nm) and an extension height ratio of $Y = 0.25$ (b = 100 nm) is reduced by 49% compared with a SiO_2-only dielectric.

Single-layer Cu/air-gap and extended Cu/air-gap structures using the tetracyclododecene (TD)-based thermally decomposable sacrificial polymer as a temporary placeholder between the Cu metal lines were fabricated. Figure 7 shows a cross-sectional secondary electron microscopic (SEM) image of an extended Cu/air-gap structure. The width and aspect ratio of the Cu lines were 210 nm and 1.8, respectively. The width of the air-gaps was 190 nm and the air-gap was extended into the top and bottom PECVD SiO_2 layers by 80 nm and 100 nm, respectively. The SEM image shows that the TD-based polymer was cleanly decomposed, leaving an air-cavity as the intralevel dielectric, without residual solids on the side walls of the copper.

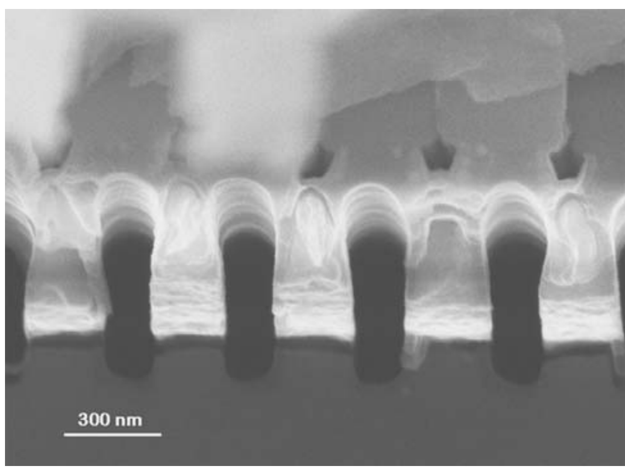
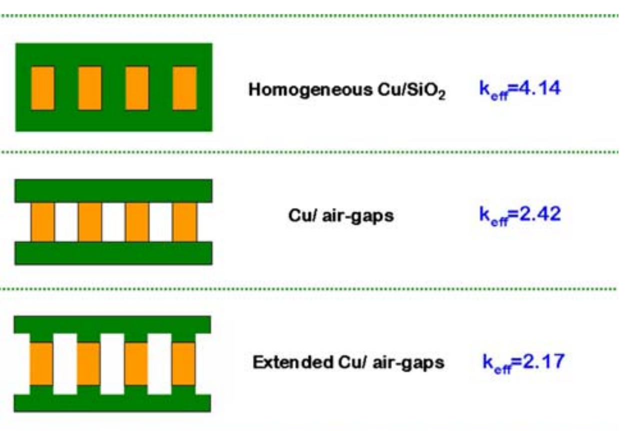


Fig. 7. Cross-sectional secondary electron microscopic image of the extended Cu/air-gaps structure.

Table IV. Summary of the Measured Effective Dielectric Constants of the Comb Structure Devices



Structure	k_{eff}
Homogeneous Cu/SiO_2	k_{eff}=4.14
Cu/ air-gaps	k_{eff}=2.42
Extended Cu/ air-gaps	k_{eff}=2.17

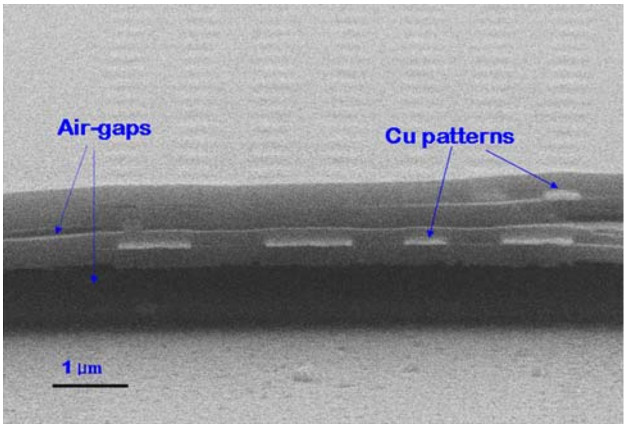


Fig. 8. Cross sectional secondary electron microscopic image of multilayer air-gaps and Cu patterns.

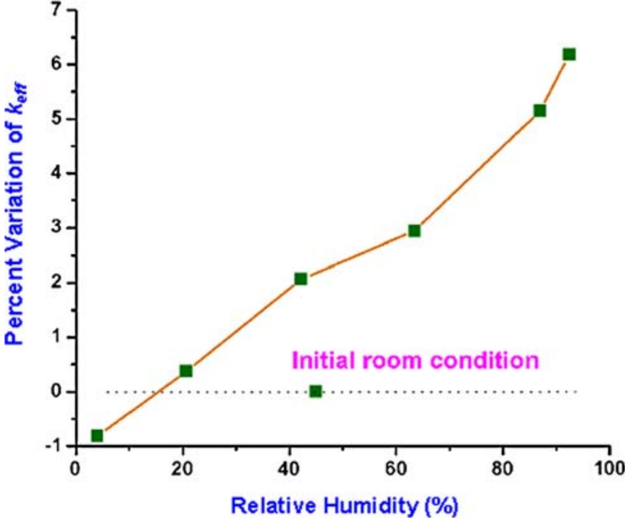


Fig. 9. The effect of moisture uptake of extended Cu/air-gaps interconnect structures on the k_{eff}.

An interdigitated comb structure was fabricated and the measured capacitance values of the Cu/SiO_2, Cu/air-gap, and extended Cu/air-gap structures are summarized in Table IV. The dielectric constant of PECVD SiO_2 measured with a parallel plate capacitor was 4.14. Thus, the k_{eff} of the homogeneous SiO_2/Cu interconnect was 4.14. The measured k_{eff} of Cu/air-gap and extended Cu/air-gap structures were 2.42 and 2.17, respectively. According to the 2006 ITRS,[1] the required k_{eff} for a 32 nm technology node in 2013 is 2.1 to 2.4. As shown in Fig. 5b, the electrostatic simulation of the dielectric constant for the low-k interlayer dielectric material (ε_r = 2.7) instead of SiO_2 would lower k_{eff} below 1.9.

The thermal decomposition of the sacrificial polymer is a critical part of the air-gap formation. A multilayered structure could have air-gaps in several layers. It is beneficial to decompose the sacrificial material at the end of the build-up sequence and not after each layer. This was demonstrated in Fig. 8 where a multilayer interconnect structure with two layers of sacrificial polymer was fabricated. Both layers of sacrificial polymer were decomposed at once. Two air-gap layers and two Cu layers are clearly shown, and the sacrificial polymer in both layers was fully decomposed.

The effect of moisture absorption on k_{eff} in the extended Cu/air-gap structures was studied. The results are shown in Fig. 9. Increasing the relative humidity (RH) in the ambient air from 40% to 92%, at constant temperature, resulted in a 6.2% increase in k_{eff} (from 2.17 to 2.32) for the as-fabricated samples. According to our previous study,[9] the walls of the cavity, after polymer decomposition, were hydrophobic. The interlayer dielectric, including SiO_2, are nonhermetic and allow air and moisture to permeate from the ambient.

Due to the high electric polarizability of water, the absorbed water significantly increases the effective dielectric constant and can lead to corrosion problems. In order to minimize the increase in capacitance with RH, the extended Cu/air-gap structure was made hydrophobic by reaction with hexamethyldisilazane (HMDS) vapor for 1 h in vacuum. After exposure to the HMDS vapor, the k_{eff} of the extended Cu/air-gap structure decreased by 1.7%. When the HMDS-treated sample was exposed to the highest RH, k_{eff} increased by only 0.3% above the initial condition.[18–20] The change in effective dielectric constant is shown in Fig. 10. The initial dielectric constant at ambient humidity is shown in Fig. 10. During the HMDS process, surface hydroxides react with HMDS, resulting in an alkyl-terminated surface which is hydrophobic. In a similar way, HMDS has been used to repair damage within porous low-k materials and terminating the surface with a trimethyl siloxane moiety.[21,22] The reduction in dielectric constant is shown in Fig. 10.

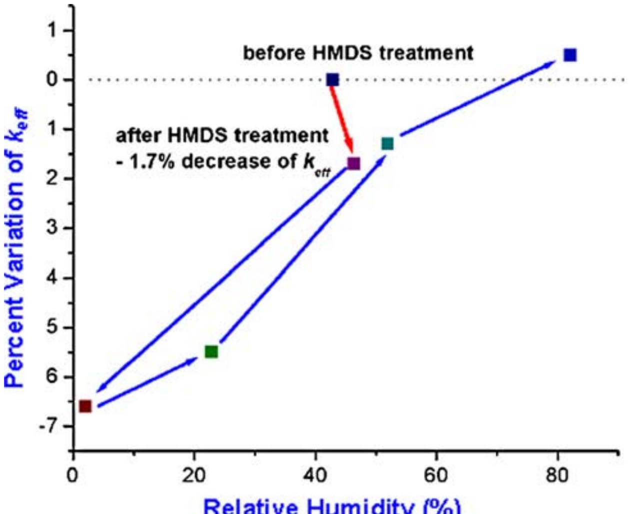


Fig. 10. The effect of HMDS vapor treatment on the k_{eff} of extended Cu/air-gaps interconnect structures.

The arrows trace the sequence of events in treating the sample with HMDS, and then follow the changes in relative humidity. The equivalent thickness of water responsible for the change in k_{eff} can be estimated by the electrostatic simulation. One would need 3.1 Å of water to account for a 1.7% reduction of the k_{eff}. This is about 1.5 monolayers of water, assuming the bulk value of k for water.

DISCUSSION

The insulator-first process is preferred in the Damascene fabrication process, versus the copper-first process used here. Figure 11 shows a via-first dual Damascene fabrication process for Cu/air-gap structures using the thermally decomposable sacrificial polymer process used in this study. The dual Damascene, via-first process using the sacrificial polymer placeholder process for air-gap formation developed here will be compared with the published approaches for via-first dual Damascene processing.

The dual Damascene air-gap process using a sacrificial polymer starts with completing the lower interconnect layer (Fig. 11a). An interlayer dielectric (the via hole layer) is deposited followed by spin-coating the sacrificial polymer. A low-k dielectric such as SiCOH (ε_r = 2.7) is preferred for the interlayer dielectric. The inorganic nature of SiCOH also provides a convenient etch-stop for the patterning of the lines (above the via level). A thin SiO_2 or SiCOH hard mask is deposited on the spin-coated sacrificial

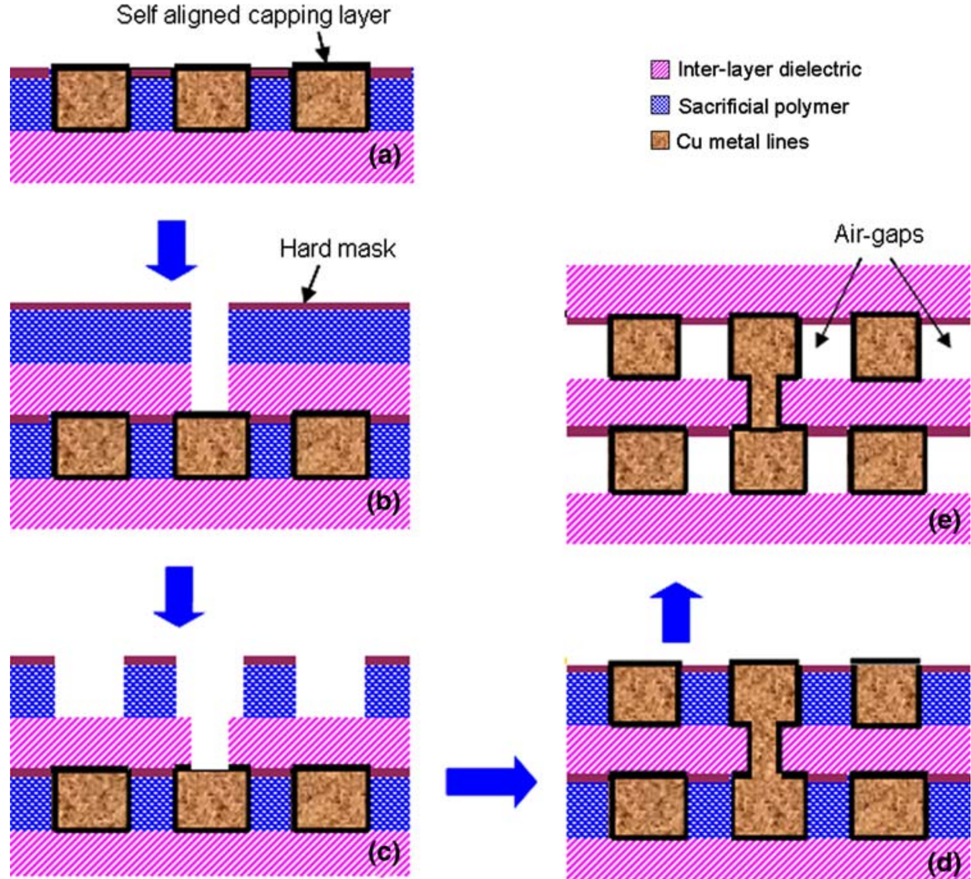


Fig. 11. Proposed fabrication process flow for the Cu/air-gaps interconnect structure using dual Damascene processes.

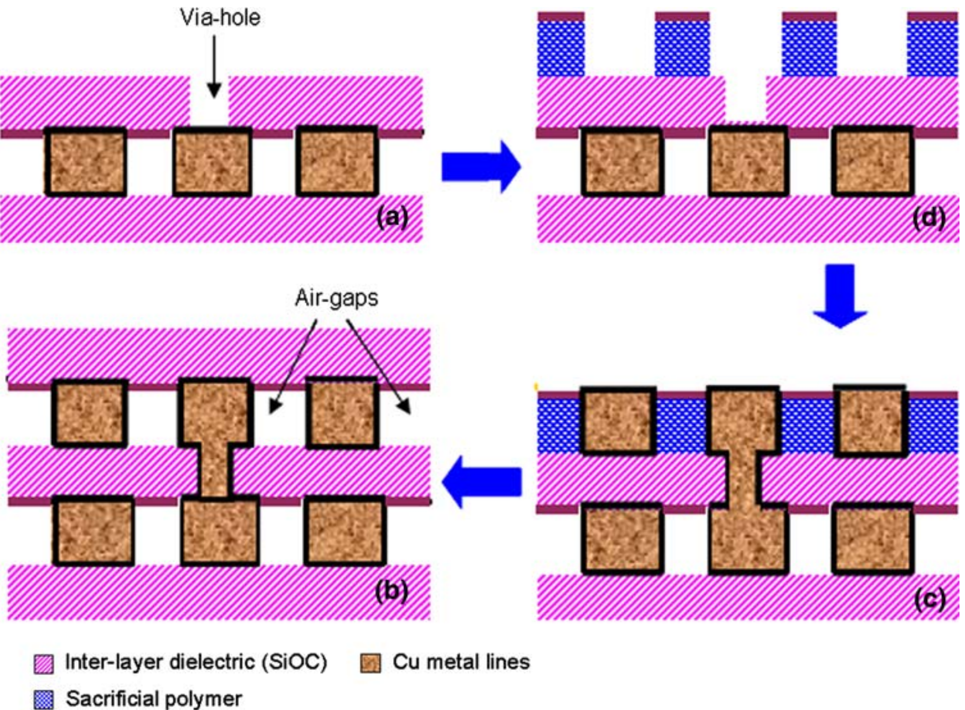


Fig. 12. The process flow of an embedded via-first dual Damascene air-gap using a spin-on thermally degradable sacrificial polymer.[10]

polymer, and SiCOH is preferred due to its low dielectric constant versus SiO_2. This is followed by via-hole lithography and etching as shown in Fig. 11b. A self-aligned capping layer such as CoWP or CuSiN on top of the lower copper lines is used as an etch stop for dry etching the interlayer dielectric material for the via holes. After stripping the resist, a bottom antireflection coating (BARC) material is spin-coated to fill the via holes and protect them from the trench etch process. After trench patterning in Fig. 11c, the metal barrier layer and Cu seed layer are deposited, followed by copper superfilling. The excess Cu is removed by CMP and the hard mask on top of the sacrificial polymer is used as a CMP stop-layer as shown in Fig. 11d. After deposition of the self-aligned capping layer on top of the Cu lines, the last two steps are the deposition of the top interlayer dielectric and thermal decomposition of the sacrificial polymer (Fig. 11e), forming the Cu/air-gap structures. In the fabrication processes, high aspect ratio and anisotropic sacrificial polymer patterns are required. The sacrificial polymer needs to hold its spatial dimensions during the CMP step. Thus, a hard, sacrificial polymer is preferred. It was shown that the TD-based sacrificial polymer is harder than the norbornene-based sacrificial polymer, while the thermal properties of the two materials are the same.[9]

Minimizing the residual material within the air-gap is important because it can degrade k_{eff}. If a large amount of residue remains, it can increase the leakage current and capacitance, and decrease the time-dependent dielectric breakdown. According to a previous study,[9] the decomposition residue of the TD-based sacrificial polymer is less than 1% of the original polymer thickness. In addition, decreasing the background oxygen concentration in the thermal decomposition furnace reduces the residue.[23] Thus, it is expected that the effect of the decomposition residues on the interconnect performance should be small.

Other via-first dual Damascene air-gap processes using a spin-on thermal degradable sacrificial polymer as a placeholder and SiOC as an interlayer dielectric have been published.[10] A simplified process flow for these is shown in Fig. 12 for comparison with the sacrificial polymer approach. Before spin-coating of the sacrificial polymer, a via hole is formed in the SiOC interlayer dielectric as shown in Fig. 12a. Then, the sacrificial polymer is spin-coated and fills in the via holes. The sacrificial polymer filling the via hole is removed following the trench lithography step (Fig. 12b). This requires extra dry-etching time due to the thickness of the material being removed. The extra dry-etching time may change the critical dimensions of the polymer trench pattern in the via-hole region due to undercutting and damage the SiOC interlayer dielectric.[24] The next process steps are Cu metallization (Fig. 12c) and thermal decomposition of the sacrificial polymer (Fig. 12d). Compared to the conventional dual Damascene, no additional lithography step and processes are required because the via holes are formed before spin-coating of the sacrificial polymer. This results in a decrease in the number of process steps. The additional layers required are a

hard mask on the sacrificial polymer for trench patterning, and a SiCN capping layer to protect Cu lines from the top dielectric layer. The challenges in this approach are the effect of decomposition residue and misalignment of via holes.

The integration of air-gaps in an intrametal layer using wet etching of a SiO_2 intrametal dielectric material has been demonstrated in a via-first dual Damascene process.[11] The organic interlayer dielectric is SiLK (Dow Chem. Co.). The dilute hydrofluoric acid solution penetrates into the interconnect structure and dissolves the SiO_2 intrametal dielectric, while the organic SiLK interlayer dielectric remains, as shown in Fig. 1b. The additional layers in this approach include a SiC capping layer and a CuSiN self-aligned barrier on the top of the Cu lines. The SiC ($\varepsilon_r = 5.8$) capping layer on the top of the dual Damascene structure is essential to preventing the diffusion of dilute HF etching solution into regions where it would damage the structure. The SiC raises the k_{eff} of the interconnect structures because of its high dielectric constant. An additional lithography step is necessary to localize the air-gaps to specific regions. The complete removal of the HF etching solution from the interconnect structure can also be a challenge.

The integration approach of air-gaps using nonconformal deposition of an interlevel dielectric material in a via-first dual Damascene process has been demonstrated.[12,13] After finishing the via-first dual Damascene process, the intrametal dielectric in the dense region is etched back using an additional lithography step as shown in Fig. 1c. Air-gaps are then formed during the nonconformal plasma deposition of an interlayer dielectric. The plasma etching of the lines for the trench does not use an etch-stop layer. In addition, there is no etch-stop layer in the etch-back process of the intrametal dielectric. Thus, etch damage in the interlayer dielectric may occur.[21] A process to repair the damaged low-k may be required.[19–21] An additional CMP step is required for the planarization of the nonconformal interlayer dielectric. The air cavity occupies only a portion of the intralayer dielectric region. The additional layers in this approach are a hard mask, a SiC dielectric liner, and a capping layer. The challenges in the integration of air-gaps by nonconformal deposition of an interlayer dielectric are breakthrough of the air-cavities during trench etch into the via-level dielectric, and mislanded vias due to misalignment,[23,24] as shown in Fig. 13. In order to avoid the breakthrough of air-cavities into the via-level dielectric during the process, the height of the air-gap is controlled using a hard mask and an additional lithography step. This controls the width of the etched-back area in the intrametal dielectric region, as shown in Fig. 13a.[24] In order to address the problem of mislanded via shown in Fig. 13b, a hard mask and an additional lithography step are used to exclude air-gaps from underneath the via holes.[23] In the etch-back process

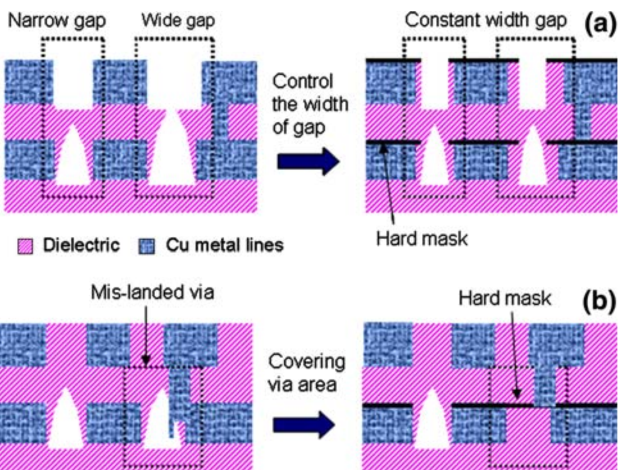


Fig. 13. The challenges in the air-gap formation during nonconformal deposition of the interlayer dielectric: (a) breakthrough of air-gaps and (b) mislanded via due to misalignment.

of the intrametal dielectric, the hard mask covers the via area and prevents the formation of air-gaps, resulting in the localization of the air-gaps in the desired area.

IBM has recently integrated air cavities into dielectrics.[2] After completing the dual Damascene process, the SiCOH intrametal dielectric in a desired region is selectively etched back using a thin oxide hard mask and an additional noncritical lithography step at the first metal layer and a nanoporous polymer are used. During the lithography step, the width of the etched area in between the Cu lines is kept constant, controlling the width and aspect ratio (H:W) of the air-gap trench. The air-gaps are formed by the nonconformal deposition of the upper SiCOH dielectric layer. Compared to the conventional dual Damascene process, eight additional process steps are required. These include the deposition and removal of the hard mask, a noncritical lithography step, etch back of the intrametal dielectric, and an additional CMP for planarization of the surface of the nonconformal SiCOH dielectric. The advantage of this approach is that no new materials are introduced and air-cavities can be inserted at any level. However, the dry etch damage in the SiCOH may increase the dielectric constant due to carbon depletion.[21]

The via-first dual Damascene process to extend the air-cavity into the interlayer dielectric regions is shown in Fig. 14. After formation of a via hole (Fig. 14a), the trench pattern in the sacrificial polymer is developed by use of an additional lithography step. Then, a metal barrier and copper seed layer are deposited. The wafer is then planarized, and a self-aligned capping layer is deposited as shown in Fig. 14b. After the deposition of the self-aligned capping layer on the top of the copper lines, the sacrificial polymer is stripped by dry or wet etching and the copper lines remain. The remaining Cu lines are used as a hard mask during

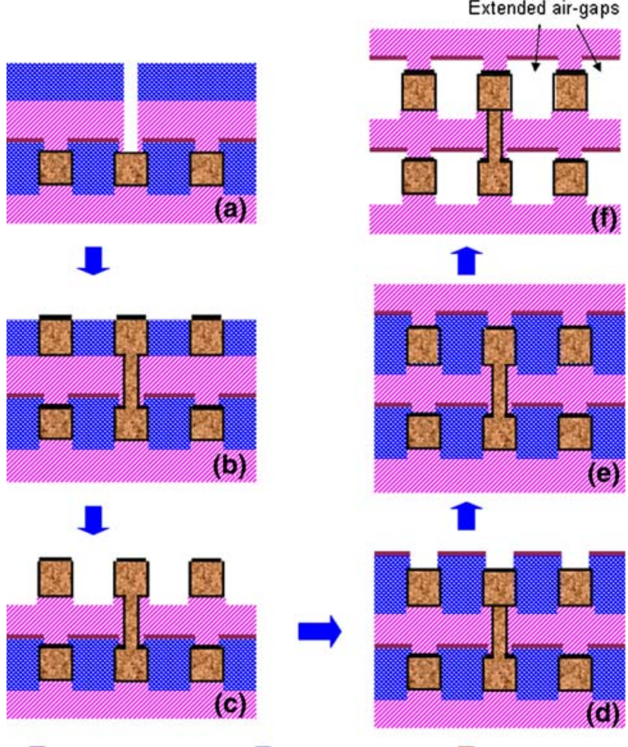


Fig. 14. The proposed fabrication process flow for the extended Cu/air-gaps interconnect structure using dual Damascene processes.

the etching of the lower interlayer dielectric to extend the air-gaps into the dielectric layer, as shown in Fig. 14c. Then, a sacrificial polymer is spin-coated and a thin, hard-mask layer is deposited. Gap fill between the copper lines is not likely to be an issue for the sacrificial polymer because it will be removed in the final thermal decomposition step. In the fabrication of extended air-gaps in Fig. 3c, the surface of the spin-coated sacrificial polymer layer was planarized and no additional CMP step was needed. The thickness of the sacrificial polymer on top of the Cu lines determines the extension height of the air-cavity into the top interlayer dielectric. After deposition of the thin hard mask, a lithography step is needed to remove the sacrificial polymer from on top of the copper lines, resulting in the extension of the air-cavity into the top interlayer dielectric, as shown in Fig. 14d. In this step, the width of the etched sacrificial polymer pattern above the Cu lines should be smaller than the width of the Cu lines in order to avoid overetching of the sacrificial polymer. The final process step is the thermal decomposition of the sacrificial polymer in the intrametal dielectric region (Fig. 14f). Compared with the dual Damascene air-gap process in Fig. 11, the additional process steps are etched back at the bottom of the interlevel dielectric layer in Fig. 14c. The sacrificial polymer, on the top of the Cu lines, is removed (Fig. 14d) to extend the air-gap into the interlayer dielectric region.

CONCLUSION

The advantages of the air-gaps as an ultralow-k dielectric and methods of fabrication are presented. The integration of air-gaps or extended air-gaps with low-k interlevel dielectrics could satisfy the requirement for 32 nm technology node and beyond.

The measured effective dielectric constants of Cu/air-gap (200 nm half pitch and aspect ratio of 1.8) and extended air-gap (extended height of 80 nm on top and 100 nm on the bottom) was 2.42 and 2.17, respectively. Adsorbed moisture increased the capacitance by 7%. However, exposure to HMDS vapor removed the moisture and made the interconnect hydrophobic, resulting in only 0.3% increase at the highest RH. Fabrication processes for the Cu/air-gap structures and extended air-gap using TD-based thermally decomposable polymers with a dual Damascene processes were proposed and compared to other integration approaches.

ACKNOWLEDGEMENT

The authors gratefully acknowledge the support of Promerus LLC.

REFERENCES

1. *The International Technology Roadmap for Semiconductors* (2006). http://www.itrs.net/.
2. D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig et al., *Technical Digest, IEEE International Electron Devices Meeting* (2007), p. 773.
3. D.C. Edelstein, G.A. Sai-Halasz, and Y.-J. Mii, *IBM J. Res. Dev.* 39, 383 (1995).
4. D.C. Edelstein, *Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference* (1995), p. 301.
5. N.P. Hacker, G. Davis, L. Figge, and T. Krajewski, *Proc. MRS Symp. Low Dielectric Constant Materials III*, Vol. 476, eds. C. Case, P. Kohl, T. Kikkawa, and W. Lee (1997), p. 25.
6. Y. Ohoka, Y. Ohba, A. Isobayashi, N. Komai, S. Arakawa, R. Kanamura, and S. Kadomura, *IITC* (San Francisco, CA, 2007), pp. 67–69.
7. M. Aimadeddine, V. Jousseaume, V. Arnal, L. Favennec, A. Farcy, A. Zenasni, M. Assous, M. Vilmay, S. Jullian, P. Maury, V. Delaye, N. Jourdan, T. Vanypre, P. Brun, G. Imbert, Y. LeFriec, M. Mellier, H. Chaabouni, L.L. Chapelon, K. Hamioud, F. Volpi, D. Louis, G. Passemard, and J. Torres, *IITC* (San Francisco, CA, 2007), p. 175.
8. P.A. Kohl, D.M. Bhusari, M. Wedlake, F.P. Klemens, J. Miner, B.C. Lee, and R.J. Gutmann, *Electron. Dev. Lett.* 21, 557 (2000).
9. S. Park, J. Krotine, S. Allen, and P. Kohl, *VMIC* (Fremont, CA, 2007).
10. R. Daamen, P.H.L. Bancken, D. Ernur Badaroglu, J. Michelon, V.H. Nguyen, G.J.A.M. Verheijden, A. Humbert, J. Waterloos, A. Yang, J.K. Cheng, L. Chen, T. Martens, and R.J.O.M. Hoofman, *IITC* (San Francisco, CA, 2007), p. 61.
11. L.G. Gosset, F. Gaillard, D. Bouchu, R. Gras, J. de Pontcharra, S. Orain, O. Cueto, Ph. Lyan, O. Louveau, G. Passemard, and J. Torres, *IITC* (San Francisco, CA, 2007), p. 58.
12. T. Harada, A. Ueki, K. Tomita, K. Hashimoto, J. Shibata, H. Okamura, K. Yoshikawa, T. Iseki, M. Higashi, S. Maejima, K. Nomura, K. Goto, T. Shono, S. Muranka, N. Torazawa, S. Hirao, M. Matsumoto, T. Sasaki, S. Matsumoto, O. Ogawa, M. Fujisawa, A. Ishii, M. Matsuura, and T. Ueda, *IITC* (San Francisco, CA, 2007), p. 141.
13. R.H. Havemann and S.-P. Jeng, U.S. patent No. 5,461,003 (1995).

14. B. Shieh, K.C.. Saraswat, J.P. McVittie, S. List, S. Nag, M. Islamraja, and R.H. Havemann, *Electron. Dev. Lett.* 19, 16 (1998).
15. L.G. Gosset, V. Arnal, C. Prindle, R. Hoofman, G. Verheijden, R. Daamen, L. Broussous, F. Fusalba, M. Assous, R. Chatterjee, J. Torres, D. Gravesteijn, and K.C. Yu, *IITC* (2003), p. 65.
16. M.D. Wedlake and P.A. Kohl, *J. Mater. Res.* 17, 632 (2002).
17. X. Wu, H. Reed, Y. Wang, L. Rhodes, E. Elce, R. Ravikiran, R. Shick, C. Henderson, S. Allen, and P. Kohl, *J. Electrochem. Soc.* 150, H205 (2003).
18. Y. Uchida, S. Hishiya, N. Fujii, K. Kohmura, T. Nakayama, H. Tanaka, and T. Kikkawa, *Microelectron. Eng.* 83, 2126 (2006).
19. T. Rajagopalan, B. Lahlouh, J.A. Lubguban, N. Biswas, S. Gangopadhyay, J. Sun, D.H. Huang, S.L. Simon, D. Toma, and R. Butler, *Appl. Surf. Sci.* 252, 6323 (2006).
20. T.C. Chang, Y.S. Mor, P.T. Liu, T.M. Tsai, C.W. Chen, Y.J. Mei, and S.M. Sze, *J. Electrochem. Soc.* 149, F81 (2002).
21. O. Richard, F. Iacopi, H. Bender, and G. Beyer, *Microelectron. Eng.* 84, 517 (2007).
22. N. Grove, Characterization of functionalized polynorbornenes as interlevel dielectrics (Ph.D. dissertation, Georgia Institute of Technology, 1997).
23. J. Noguchi, T. Oshima, T. Matsumoto, S. Uno, K. Sato, N. Konishi, T. Saito, M. Miyauchi, S. Hotta, H. Aoki, T. Kikuchi, K. Watanabe, and K. Kikushima, *IITC* (2006), p. 167.
24. R. Daamen, P.H.L. Bancken, V.H. Nguyen, A. Humbert, G.J.A.M. Verheijden, and R.J.O.M. Hoofman, *Microelectron. Eng.* 84, 2177 (2007).