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Some Critical Materials and Processing Issues in SiC Power Devices

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There has been a rapid improvement in SiC materials and power devices during the last few years. However, the materials community has overlooked some critical issues, which may threaten the emergence of SiC power devices in the coming years. Some of these pressing materials and processing issues will be presented in this paper. The first issue deals with the possibility of process-induced bulk traps in SiC immediately under the SiC/SiO_2 interface, which may be involved in the reduction of effective inversion layer electron mobility in SiC metal–oxide–semiconductor field-effect transistor (MOSFETs). The second issue addresses the effect of recombination-induced stacking faults (SFs) in majority carrier devices such as MOSFETs, Schottky diodes, and junction field-effect transistors (JFETs). In the past it was assumed that the SFs only affect the bipolar devices such as PiN diodes and thyristors. However, most majority carrier devices have built-in *p*–*n* junction diodes, which can become forward biased during operation in a circuit. Thus, all high-voltage SiC devices are susceptible to this phenomenon.

Key words: SiC, SiC power devices, SiC/SiO_2 interface, interface traps, bulk traps, recombination-induced stacking faults, effective inversion layer electron mobility

INTRODUCTION

Some of the most important issues limiting the commercialization of SiC power MOSFETs are high positive fixed charge in the gate oxide, low threshold voltage, low effective inversion layer electron mobility, and poor reproducibility of these very important parameters. All these problems are interrelated. The conventional understanding is that the high fixed positive charge in the gate dielectric is balanced by an equally high negative charge in the acceptor-like states near the conduction band edge resulting in low and poorly reproducible threshold voltage. The high density of interface states not only removes the inversion layer electrons from the conduction band but also reduce the effective electron mobility by scattering. It is speculated, for the first time, that an important third component of this problem, which has been overlooked thus far, may also significantly affect the threshold voltage and effective inversion layer electron mobility. This third component is due to the bulk traps in SiC, which may already be present in high numbers and are significantly increased by processing such as thermal oxidation itself and ion implantation followed by high-temperature anneals. If this conjecture is correct then the focus of research should shift from efforts to reduce the interface state density at the SiC/SiO_2 interface using various pre- and postoxidation anneals (POA) to the reduction of process-induced bulk traps in SiC. The process of fabrication of MOSFETs may shift toward utilizing epitaxial layers as opposed to the implanted *p*-wells and subsequent activation at temperatures as high as 1700°C. More importantly, if the process of oxidation itself is responsible for the generation of defects immediately below the SiC/SiO_2 interface, then the deposited oxides with no subsequent thermal oxidation should be considered followed by N_2 and H_2 treatments. Annealing in NO

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or N_2O ambient results in significant oxidation and therefore other means of delivering nitrogen to the SiC/SiO_2 interface should be considered such as annealing in ammonia or ion implantation of nitrogen with subsequent drive-in.

The phenomenon of recombination-induced stacking faults (SFs) in high-voltage p–n diodes in SiC has previously been shown to increase the forward voltage drop due to a reduction of the carrier lifetime in the conductivity-modulated drift region. We have recently discovered that this effect is equally important in unipolar devices such as high-voltage MOSFETs and merged PiN Schottky (MPS) diodes. If the internal body diode is allowed to be forward biased during the operation of these devices, then the recombination-induced SFs not only reduce the majority carrier conduction current but also significantly increase the leakage current in blocking mode.[1–2] The effect is more noticeable in high-voltage devices where the drift layer is thick. It is not expected to impact 600 to 1200 V devices, which have a drift layer thickness of 6 to 12 μm. There are important consequences of this finding, which will change the way in which majority carrier devices in SiC are designed and used. Furthermore, the traditional understanding that this phenomenon of SF formation in SiC affects only the bipolar devices has been proven wrong.

Finally, issues affecting the current gain and on-resistance degradation of bipolar junction transistors (BJTs) will be addressed. There is a need to decouple various issues in these devices such as increase in surface states, lifetime reduction due to the recombination-induced stacking faults in the base and collector layers, and the effect of SFs on majority carrier conduction.

SiC MOS ISSUES

Since 1990, numerous papers have been written on the factors limiting the performance of SiC MOSFETs. All the papers addressing the low effective inversion layer mobility, μ_{eff}, of n-channel MOSFETs have focused on the role of the interface state density, D_{it}. In this paper, it is proposed that bulk traps in SiC also play a role similar to the interface traps in reducing μ_{eff}. This new model will encourage a paradigm shift in the methods and techniques used to solve the problem of low μ_{eff} in SiC MOSFETs. In 1999, both Emil Arnold[3] and Reinhold Schörner and colleagues[4] independently advanced the concept of rapidly increasing D_{it} near the conduction band edge and its deleterious effect on μ_{eff}. The current understanding is explained as follows. A large fraction of the electrons in the inversion layer of n-channel SiC MOSFETs are trapped by the interface traps below the equilibrium position of the Fermi level at the $Si–SiO_2$ interface. As the device is driven into stronger inversion by the application of a positive gate bias, an increasingly large fraction of inversion layer electrons get trapped. This is due to the increasing density of interface traps as the equilibrium Fermi level moves closer to the conduction band edge. This removes mobile electrons from the inversion layer and therefore μ_{eff} calculated from the charge sheet model is drastically reduced. In addition to the reduced electron density in the inversion layer, the remaining electrons in the inversion layer suffer from coulomb scattering by the negatively charged acceptor like states resulting in a further reduction of μ_{eff}. This model is schematically shown in Fig. 1 (adapted from Ref. 4). It successfully explained the experimental data corresponding to μ_{eff} being largest in 15R-SiC, intermediate in 6H-SiC, and lowest in 4H-SiC due to the different positions of the conduction band edge in the three polytypes with respect to a rapidly increasing D_{it} profile.

After publication of the papers by Emil Arnold and Reinhold Schörner, work began in earnest to try to reduce D_{it} near the conduction band edge of 6H- and 4H-SiC MOS devices. Prior to this, most of the experimental work had been focused on reducing D_{it} near the mid gap and in the lower-half band-gap as measured on p-MOS capacitors. For example the pioneering work by Lori Lipkin and John Palmour on the so-called "wet reox" anneal at 950°C, which reduced D_{it} near the mid-gap and towards the valence band edge by almost an order of magnitude but had no effect on μ_{eff}.[5] Success was soon achieved by Jamet and Dimitrijev[6] who demonstrated that direct oxidation in NO ambient could reduce D_{it} near the conduction band edge by an order of magnitude. This notion was extended by Chung et al., who showed that μ_{eff} could indeed be improved by reducing D_{it} through POA in NO ambient.[7] Since then, no other major breakthrough has taken place in our understanding of the problem as it relates to the role of rapidly increasing D_{it} toward the conduction band edge in the reduction of μ_{eff}.

The SiC MOSFETs have been demonstrated with a breakdown voltage in the range of 1200 V to

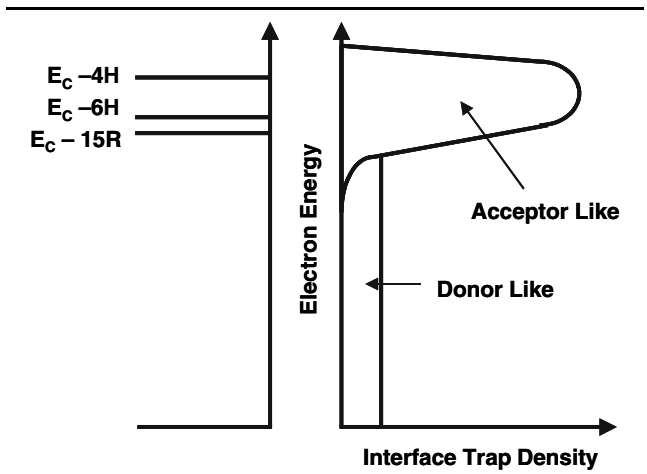

Fig. 1. Assumed distribution of interface states at the $SiC–SiO_2$ interface for different polytypes of SiC (adapted from Ref. 4).

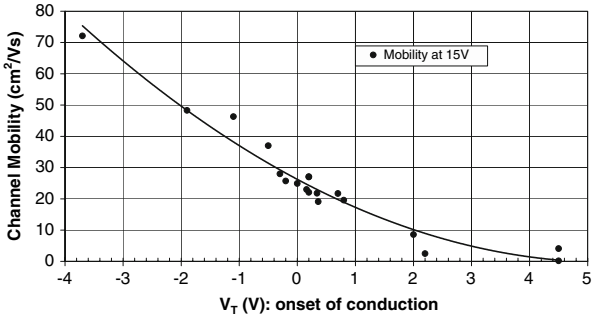

Fig. 2. Inversion layer mobility versus threshold voltage in the 4H-SiC MOS system.

10 kV. The most difficult issue has been the control of threshold voltage from run to run. This difficulty arises due to the fact that the threshold voltage is determined by a difference of two large numbers, namely, a large fixed oxide charge and a large negative charge in the interface traps and possibly the bulk traps. Therefore, we are forced to contend with a certain effective inversion layer mobility that is largely determined by interface traps and possibly bulk traps in SiC for a given threshold voltage (Fig. 2). The curve shown in Fig. 2 is fairly universal and applies to all SiC MOSFETs regardless of the blocking voltage. If we improve the effective inversion layer mobility by reducing interface trap density by means of a postoxidation anneal in NO then the threshold voltage reduces. The resulting negative temperature coefficient of on resistance, due to the interdependence of the threshold voltage and inversion layer mobility, is a serious concern for parallel operation of MOSFETs.

The New Model

The proposed model is shown in Fig. 3. It is speculated that, in addition to interface traps, bulk traps on either side of the interface are being generated during the high-temperature oxidation process and/or due to the ion implantation and subsequent anneal at high temperatures. It considers the role of bulk traps, N_{it}, in SiC on μ_{eff} and threshold voltage in addition to the role of D_{it}. This represents a radical departure from the exclusive focus on interface states over the last 15 years. The bulk traps in SiC should affect μ_{eff} in the same manner as the interface traps do, by trapping electrons from the inversion layer and via Coulomb scattering. The traps located within the depletion width of SiC, below the equilibrium Fermi level, will be negatively charged and will contribute negative charge to the overall charge balance in equilibrium. The net effect will be to reduce the amount of inversion charge for a given gate voltage, an increase in threshold voltage, V_T, and a reduction in μ_{eff}. Those bulk traps, which are within the inversion layer, will also contribute to the Coulomb scattering of mobile electrons in the inversion layer.

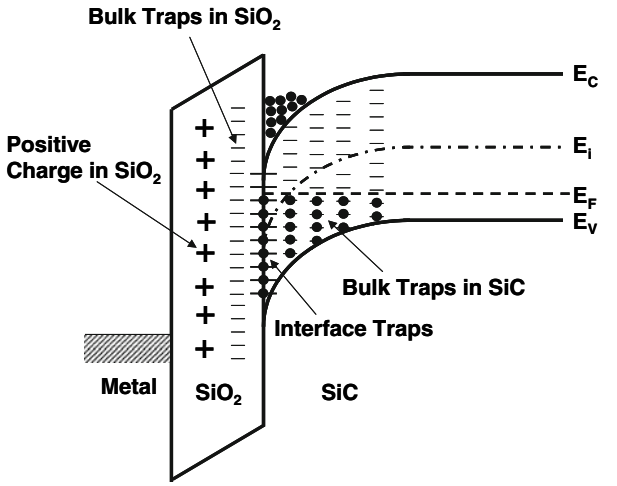

Fig. 3. Depiction of the charge balance in an SiC MOS system with Q_{ox}, D_{it}, and bulk traps under a positive gate bias.

The presence of numerous bulk traps in SiC has been well documented and researched.[8–11] The bulk traps can arise from point defects such as carbon and silicon vacancies, interstitials, complexes, etc., as well as extrinsic defects such as impurities. In addition, new defects are created by simply annealing SiC at high temperatures with and without ion implantation of impurities. Any processes such as ion implantation or high-temperature implant activation anneal, which increase the density of bulk traps in SiC, will tend to increase V_T and reduce μ_{eff} in n-channel SiC MOS systems. Furthermore, the thermal oxidation itself may result in defects immediately below the SiC/SiO_2 interface. Needless to say, there is an ample supply of bulk traps (intrinsic and process induced) in SiC material.

The following experiment was done to understand the effect of bulk traps on μ_{eff} created by ion implantation. As shown in Fig. 4, 5 μm of lightly doped p-epilayer was grown on a p-type 4H-SiC substrate. A heavy dose of p^+ impurity (Al) with a surface concentration of 5×10^{18} cm^{-3} was then implanted at an elevated temperature of 650°C. This implant was activated at 1650°C in an Ar ambient with a graphite cap on the surface to maintain surface morphology. After carrying out a sacrificial oxidation to remove approximately 20 nm of the SiC surface, a lightly doped (1×10^{16} cm^{-3}) p-epilayer was regrown with three different thicknesses: (1) 0.15 μm, (2) 0.5 μm and (3) 2.0 μm. In addition, a control sample with no regrown epilayer was also included. Lateral MOSFETs were made using phosphorous implants activated at 1200°C in a furnace and a 50 nm gate oxide grown in a dry O_2 ambient at 1200°C followed by a 2 h anneal in NO at 1175°C. The field-effect mobility data measured on the lateral MOSFETs for various samples are shown in Fig. 5. As expected, the sample with no

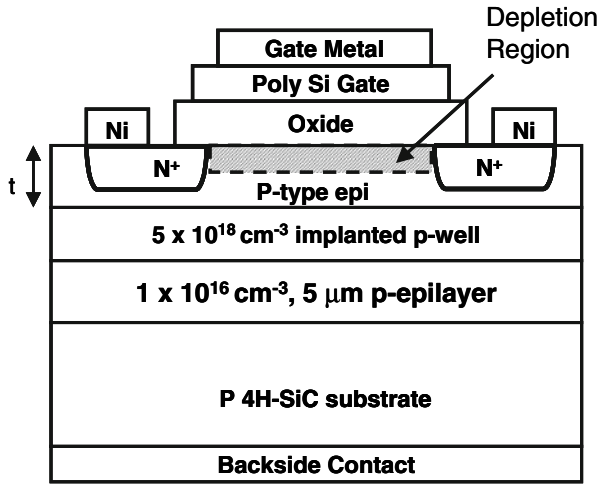

Fig. 4. Cross-section of the lateral 4H-SiC MOSFET with a regrown *p*-epilayer on a heavily implanted *p*-region. The regrown *p*-epilayer was lightly doped and its thickness was varied between 0 μm and 2 μm.

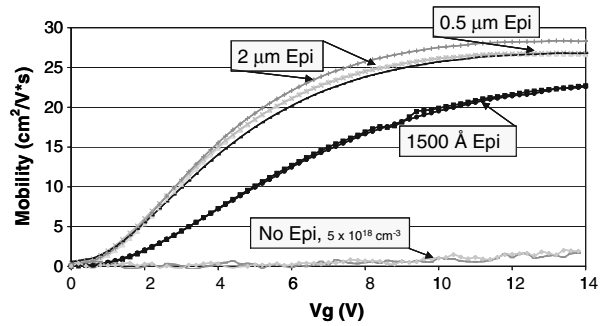

Fig. 5. The measured effective inversion layer mobility versus gate voltage graphs for various thicknesses of regrown *p*-epilayer in the MOSFET structure shown in Fig. 4.

regrown epilayer showed extremely poor mobility due to the high doping concentration and implant damage. The sample with only a 0.15 μm regrown epilayer typically showed a much lower mobility of inversion layer electrons compared to all the other samples with ≥0.5 μm regrown epilayer thickness. Furthermore, all the samples with ≥0.5 μm regrown epilayer thickness showed very similar mobility data. These results can be understood in two ways. First, the sample with 0.15 μm of epilayer thickness may have a high concentration of defects originating from the underlying heavily implanted layer, which tend to lower the inversion layer electron mobility. In contrast, the samples with thicker regrown epilayers may have very few remaining defects. Another way to look at this is to consider the maximum depletion width in strong inversion, which can be calculated to be about 0.6 μm for a 1×10^{16} cm^{-3} doping density. Thus, the depletion width extends well past the 0.15 μm regrown epilayer into the heavily implanted *p*-well, whereas it stays almost within the 0.5 μm regrown *p*-layer and certainly well within the 2 μm regrown *p*-layer. Therefore, the bulk defects in the thin regrown epilayer case do affect the inversion layer electron mobility and threshold voltage of the MOSFET according to our new model.

DISCUSSION

The question of how many traps are needed to affect the inversion layer mobility needs to be addressed. For a 50 nm gate oxide, the gate voltage is typically limited to about 15 V. Assuming the threshold voltage to be about 3 V, we can calculate the inversion charge as $Q_n = (V_G - V_T) * C_{ox}/q = 5 \times 10^{12}$ cm^{-2}. In order to alter the effective mobility, the trapped charge, Q_t, should be at least 10% of the inversion charge, say about $Q_t \sim 5 \times 10^{11}$ cm^{-2}. If it is distributed over the depletion width of about 0.6 μm, corresponding to the onset of strong inversion with a doping of 1×10^{16} cm^{-3}, then we get a trap density of $N_t \sim 1 \times 10^{16}$ cm^{-3}, which is very high. The traps located within the width of the inversion layer will, in addition to trapping electrons, further reduce the effective mobility via Coulomb scattering.

A large number of studies on defects in the SiC material have been carried out.[8–11] The defects can be point defects, impurity related, stress-related, or implant-induced. The large body of literature indicates that the trap density of the order of 10^{16}–10^{17} cm^{-3} is easily possible in implanted and subsequently annealed samples. For example, Mitra et al., have measured a trap density of 10^{15}–10^{16} cm^{-3} located at E_V + 0.51 eV in an N/Al implanted n^+–p diode.[11] The trap density increased towards the metallurgical junction. Some defects such as D_I, D_{II} centers, and the E_A spectra are created after ion implantation and persist after anneals up to 1700°C.[8]

In future work, it will be important to distinguish between the interface traps and bulk traps. Most of the work during the past 15 years has focused on improving the oxidation conditions to reduce the interface trap density. However, very little attention has been devoted to the reduction of bulk traps. If the proposed model is indeed correct, it will compel researchers to optimize implantation conditions and implant activation anneals to reduce the bulk trap density and thereby improve the effective inversion layer electron mobility in MOS structures. The process of fabrication of MOSFETs may shift toward utilizing epitaxial layers as opposed to implanted *p*-wells and subsequent activation at temperatures as high as 1700°C. Furthermore, if the process of oxidation itself is responsible for the generation of defects immediately below the SiC/SiO_2 interface, then the deposited oxides with no subsequent thermal oxidation should be considered followed by N_2 and H_2 treatments. The key point

here is to completely eliminate thermal oxidation of the SiC surface and find other means of stabilizing the SiC/deposited oxide interface with nitrogen and hydrogen etc.

THE EFFECT OF RECOMBINATION-INDUCED STACKING FAULTS ON MAJORITY CARRIER CONDUCTION

SiC PiN diodes have previously suffered from an increase in the forward drop (V_F drift) under forward conduction stress.[12] It was discovered that the basal plane dislocations (BPDs) in the thick epilayers result in the formation of stacking faults (SFs) whenever the PiN diode is forward biased.[13] The size of these SFs depends on the thickness of the epilayer. The SFs represent regions of poor lifetime and therefore, the V_F of the diodes increases, presumably due to the poor conductivity modulation in the regions occupied by the SFs. Skowronski and Ha have argued that the increase in V_F is due to the formation of the potential barrier at the stacking fault rather than due to a decrease in the carrier lifetime.[14] It was shown that the formation of the SFs can be suppressed if an epilayer with a relatively low density of BPDs (LBPD) is grown by using substrates with pre-etched patterns or using repetitive use of epilayer growth and KOH etch to prepare the substrates.[15] The effect of SFs on majority carrier conduction was first demonstrated in 2006 using a SiC merged PiN Schottky (MPS) diode.[1] In this paper, we show that the recombination-induced SFs also affect the majority carrier conduction and the reverse leakage currents in high-voltage (10 kV) SiC MOSFETs. There are important consequences of this finding, which will change the way the majority carrier devices in SiC are designed and used. Furthermore, the traditional understanding that this phenomenon of SF formation in SiC affects only the bipolar devices has been proven wrong.

Experiments

The 10 kV, 4H-SiC DMOSFET structure is shown in Fig. 6. The details of the design, fabrication, and results have been previously reported.[16] Features pertinent to this discussion are reiterated as follows. The MOS channel length, defined by the p-well and n^+ implants, is approximately 0.5 μm. When the MOS channel is turned on by the application of a positive gate bias, electrons flow laterally from the n^+ source, through the MOS channel on the implanted p-well. They then flow through the JFET region formed by two adjacent p-well regions, and finally through the lightly doped n^- drift region into the backside drain. When the MOS channel is turned off by grounding the gate, and a large drain voltage (up to 10 kV) is applied to the drain with the source grounded, the device blocks the high voltage by virtue of the reverse biased p–n junction formed by the p-well and the thick n^- drift layer. The drift

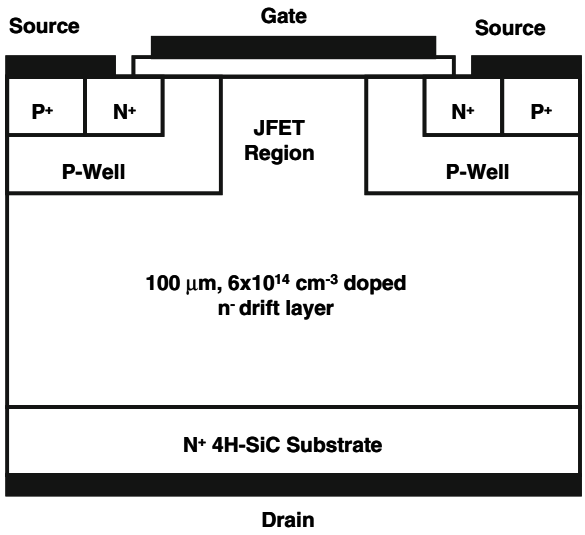

Fig. 6. Simplified cross-sectional view of a 10 kV 4H-SiC DMOSFET.

layer was designed to be 100 μm thick with a doping concentration of 6×10^{14} cm^{-3} to block 10 kV.

The following tests were performed on the device. First, the I–V characteristics of the MOSFET, and the p–n junction body diodes (formed by the p-well and the thick n^- drift layer) were measured at room temperature. The leakage current of the device was also measured up to 6 kV at room temperature. To forward bias the built-in diode, a bias of –10 V was applied on the gate to ensure the complete shut-off of the MOS channel, and a negative bias was applied to the drain. The body diode was stressed at 5 A, which is the current rating of the power DMOSFET, in forward conduction for 1 h. Following the initial stress, all the measurements were repeated. Next, the forward bias stress on the diode was repeated for two additional hours and again the electrical tests were conducted. During the forward bias stress on the body diode, the device was mounted on a heat sink with a fan running to keep the case temperature of the MOSFET package below 50°C. After the stress, the device was allowed to cool to room temperature before making the electrical measurements.

RESULTS AND DISCUSSION

The forward bias characteristics of the body diode are shown in Fig. 7. Since the diode is formed by a heavy dose of aluminum implants, the body diode shows soft turn-on characteristics. It is clear from Fig. 7 that the forward voltage of the body diode increases with forward stress. This is a well-understood phenomenon in SiC, caused by BPDs.[12–14,17] The MOSFET drift layer did not receive a BPD reduction treatment. Hence, the lightly doped n-drift layer of the 4H-SiC DMOSFET

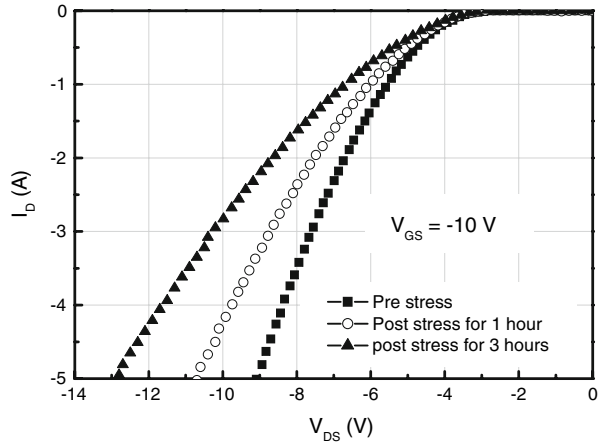

Fig. 7. Degradation of the forward *I–V* characteristics of the built-in body diode before after stress at 5 A. The gate voltage was kept at –10 V to ensure that the MOS channel was completely off.

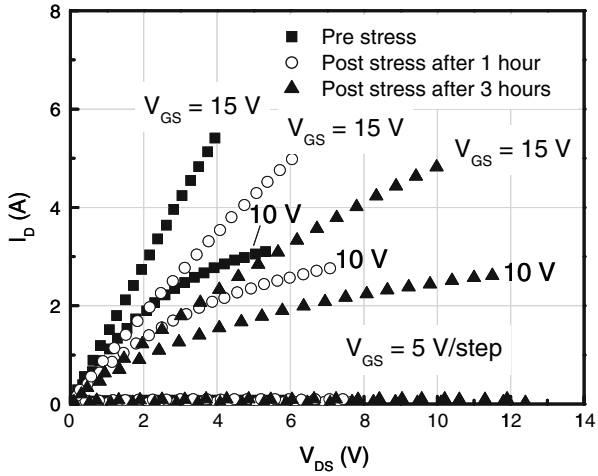

Fig. 8. Forward *I–V* characteristics of the 10 kV DMOSFET before and after stressing the body diode at 5 A. The curves with gate voltage of 0, 5, 10, and 15 V are shown. The curves with gate voltage of 0 V and 5 V are the overlapping curves near $I_D = 0$.

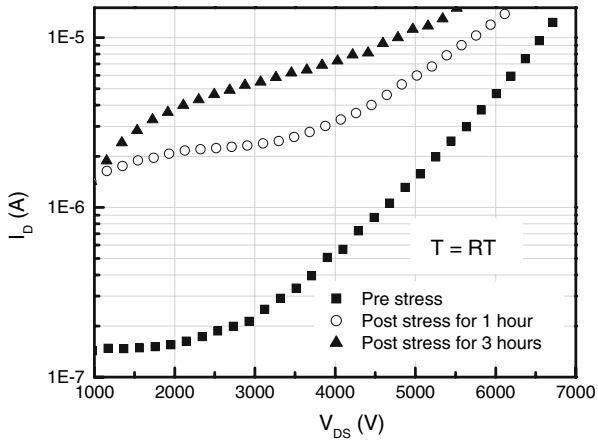

Fig. 9. Forward leakage current of the 10 kV DMOSFET at room temperature before and after stress of the body diode at 5 A.

had a high density of BPDs. These dislocations travel the thickness of the epilayer from substrate to the surface of the wafer where the device is made. When the *p–n* junction body diode is forward biased, the electrons and holes recombine in the drift layer. The recombination locally provides the energy to activate dislocation glide, which gives rise to SFs.[17] The SFs show up as triangular defects looking down at the surface of the device. The spatial size of the SFs depends upon the thickness of the drift layer. In this case, the drift layer is 100 μm thick grown on an 8° off-cut substrate. Therefore a SF's projection along the offcut direction on the wafer surface will be about 100/tan(8°) = 711 μm. The extent of the SF perpendicular to the offcut direction is comparable. Thus the area covered by these SFs may be substantial.

The forward *I–V* characteristics of the MOSFET as a function of the forward stress on body diode are shown in Fig. 8.[2] The on resistance is the slope of the *I–V* curve near the origin at V_{GS} = 15 V. The degradation in the on resistance of the MOSFET, which is completely dominated by the majority carrier conduction in the drift region, was observed. The tests were repeated on multiple devices, all of which showed similar results. It appears that the SFs induced by the forward-biased body diode not only act as recombination centers but also impede the flow of majority carriers. This may happen either by increased scattering of carriers, which reduces the effective mobility of the carriers, or by simply reduced free electron concentration through a compensation site. The actual mechanism is not yet understood at this time.

The leakage current in the forward blocking mode is shown in Fig. 9 at room temperature. The leakage current shows a marked increase with increasing stress on the body diode. The increase in leakage current as a result of recombination-induced SFs has never been reported before, although fully expected. Indeed if the SF reduces lifetime then it must be introducing electronic states in the band gap of SiC, which also act as generation centers in a reverse-biased *p–n* junction diode.

These results have important consequences for the design and use of SiC high-voltage unipolar devices such as MOSFETs, JFETs, and MPS diodes. Minority carrier injections should be avoided at all times in these devices. In typical applications of switches, the internal body diode is used as a freewheeling diode that conducts in the forward direction during some part of a switching cycle. The internal body diode in SiC switches should be bypassed by using an external SiC junction barrier Schottky (JBS) diode, which has a turn-on voltage of 1 V whereas the turn-on voltage of the internal body diode is about 3 V. This will effectively bypass the internal body diode and prevent minority carriers

from being injected. SiC MPS diodes have been used for their surge capability by utilizing the injection from the internal p–n diode at >3 V forward bias.[18] This is not recommended in high-voltage devices to prevent the formation of SFs. The high-voltage SiC MPS diodes should be bypassed by a silicon p–n diode for surge capability. Alternatively, these devices should be made on a low basal plane dislocation (LBPD) epilayer, which significantly reduces the possibility of formation of SFs. This type of epilayers are currently being perfected for use in SiC bipolar devices.

Finally, it should be emphasized that the effect of recombination-induced SFs on majority carrier conduction and leakage current has only been verified in a high-voltage structure such as the 10 kV MOSFET described in this paper. The SFs take up a large volume in a thick epilayer. As the epilayer thickness reduces for lower-voltage structures, the SFs for a given density of BPDs take up a progressively lower percentage of the volume of the drift layer and hence their effect becomes less pronounced. This effect is present, but is not expected to have a significant impact on the terminal characteristics of 600 to 1200 V class 4H-SiC unipolar devices.

DEGRADATION IN SiC BJTs

In order to study the effect of stacking faults in the collector region of SiC BJTs, measurements were performed on 4 kV SiC BJTs. The collector region of the BJTs was 40 μm thick doped at $N_D = 1.4 \times 10^{15}\,cm^{-3}$ (Fig. 10). The details of the structure can be found in Ref. 19. It is well known that there is very little conductivity modulation in the collector region of the SiC BJTs while operating in the saturation region. This implies that the on resistance of the BJT is primarily determined by the majority carrier (electron) conduction in the collector region. As shown in Fig. 10, the current is mostly concentrated near the edges of the emitter and the stacking faults can form in the base region or/and in the collector region provided there is electron-hole recombination in these regions.

The base-collector diode was stressed in the forward direction at a current of 5 A for 30 min. The emitter was not connected during the stress. The I–V characteristics of the base-collector diode were measured at room temperature before and after stress. As shown in Fig. 11, there is a significant forward voltage drift in the base-collector diode, indicating formation of recombination-induced stacking faults in the collector region. The output characteristics and the forward leakage currents were also measured, at room temperature, before and after the stress as shown in Figs. 12 and 13. It is clear from Fig. 12 that there is a significant

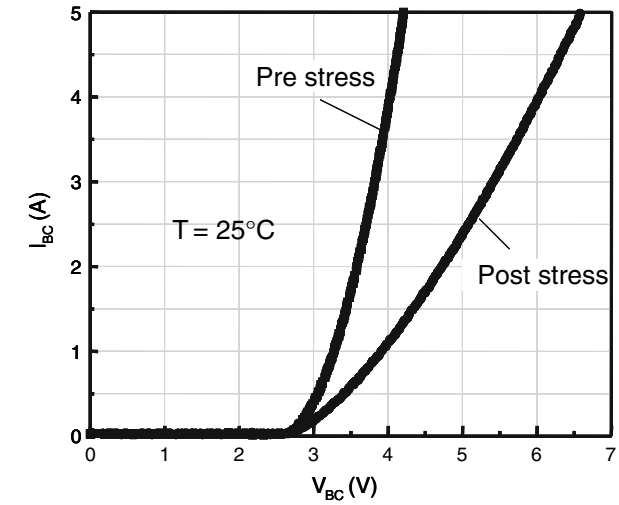

Fig. 11. Forward voltage drift of a base-collector diode due to stacking fault generation in the collector and base regions. The base collector junction was stressed at 5 A for 30 min in the forward direction.

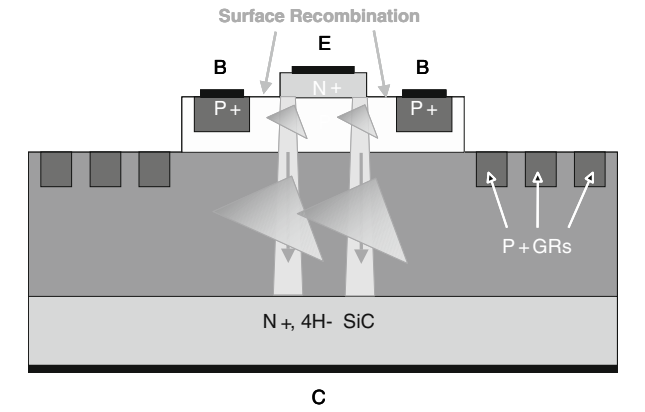

Fig. 10. Schematic cross-section of the SiC BJT showing a cartoon of recombination-induced stacking fault formation in the base and collector regions.

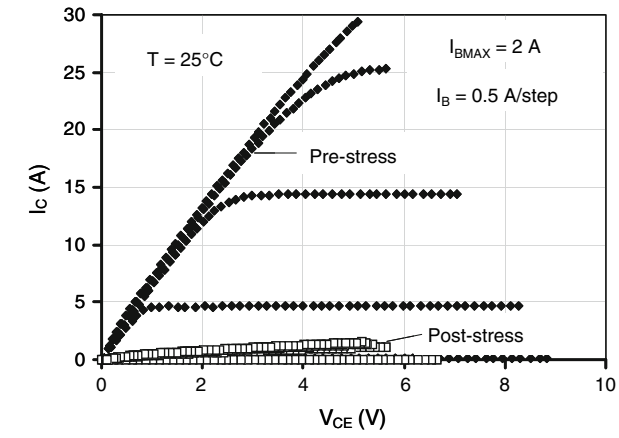

Fig. 12. The output characteristics of the SiC BJT before and after stress of the base-collector junction. The on resistance of the BJT increases drastically.

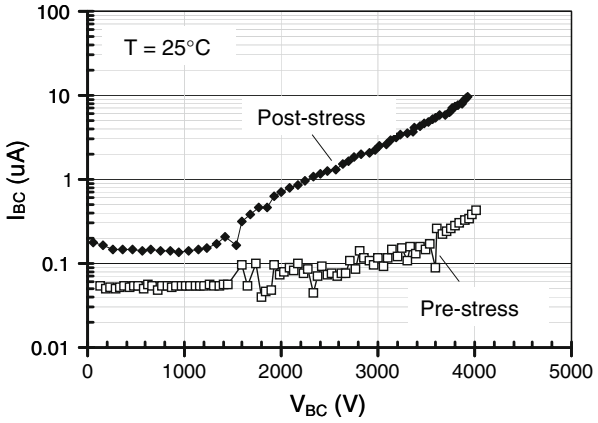

Fig. 13. The leakage current of the base-collector junction of the 4 kV SiC BJT before and after the stress of the base-collector junction.

increase in the on resistance after the stress since the on resistance of SiC BJT is primarily determined by the majority carrier conduction. This is very similar to the effect on majority carrier conduction that was described for 10 kV MOSFETs. Furthermore, the leakage current in the base-collector diode increases after degradation as seen in the 10 kV MOSFETs. These results on 4 kV SiC BJT provide further support to our findings on the effect of recombination-induced stacking faults on the conduction of majority carriers in 4H-SiC along the *c*-axis.

CONCLUSIONS

We have introduced a novel concept of bulk traps affecting the inversion layer mobility in 4H-SiC MOSFETs. These bulk traps may be created as a result of the oxidation process or ion implantation and subsequent activation at >1500°C or may already be present in the epilayer. These bulk traps can affect the inversion layer electron mobility in *n*-channel SiC MOSFETs, much the same way as the interface traps at the SiC–SiO_2 interface. This concept is speculative and is offered with no concrete evidence at the present time. Several experiments are under way at the present time to corroborate this theory. If it is indeed true that the traps on either side of the interface are being created by the high temperature oxidation process then one should consider either thermal oxides grown at <1100°C or minimizing the thickness of thermal oxide to 1–5 nm and depositing the rest of the required thickness at lower temperature. As annealing in NO or N_2O results in significant oxidation, other means of delivering nitrogen such as ion implantation should be considered. Furthermore, if the bulk traps created by high-dose implantation of *p*-wells prove to be detrimental to the effective inversion layer electron mobility then structures in which the *p*-wells are grown by epitaxy should be considered.

We have demonstrated the adverse effect of recombination-induced SFs on majority carrier conduction as well as leakage currents in a 10 kV SiC MOSFETs and 4 kV SiC BJTs. This effect was considered to be critical for bipolar devices but now for the first time, it has been shown to be equally important for unipolar devices such as MOSFETs, Schottky diodes, and JFETs. This new information will necessitate the users of these devices to bypass the internal body diode by an external Schottky diode or never allow the injection of minority carriers into the drift layer. Alternatively, unipolar devices should be made on an LBPD epilayer being developed to address this issue in bipolar devices. Finally, this effect may not be important for lower-voltage devices in the 600 to 1200 V range.

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