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Top-gated graphene field-effect transistors on SiC substrates

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We report on a demonstration of top-gated graphene field-effect transistors (FETs) fabricated on epitaxial SiC substrate. Composite stacks, benzocyclobutene and atomic layer deposition Al_2O_3, are used as the gate dielectrics to maintain intrinsic carrier mobility of graphene. All graphene FETs exhibit n-type transistor characteristics and the drain current is nearly linear dependence on gate and drain voltages. Despite a low field-effect mobility of 40 $cm^2/(V\ s)$, a maximum cutoff frequency of 4.6 GHz and a maximum oscillation frequency of 1.5 GHz were obtained for the graphene devices with a gate length of 1 μm.

graphene, radio frequency (RF), field-effect transistor (FET), SiC

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Graphene, consisting of one or a few carbon atomic layers packed into a two dimensional (2D) hexagonal lattice, has attracted enormous attention over the last few years [1]. Graphene exhibits impressive transport properties, including high carrier mobility and saturation velocity [2]. As a result, it is a good candidate for radio-frequency (RF) field-effect transistor (FET) applications. So far, high quality graphene device with a maximum cutoff frequency (f_T) of 300 GHz has been obtained on thin exfoliated films of graphite [3]. Although an excellent method to obtain single devices for scientific research, exfoliation is impractical for large-scale manufacturing of graphene sheets. However, mass production can be solved by epitaxial growth on SiC or metal-catalyzed chemical vapor deposition (CVD) [4,5]. To date, graphene FETs with f_T beyond 100 GHz have also been achieved using graphene films synthesized by both methods [6,7]. Graphene by epitaxy on SiC is directly obtained on semi-insulating SiC substrates, so that no transfer is required before processing devices, as compared with the CVD method. Recently, graphene integrated circuits have been realized on SiC wafers [8], showing potential in practical applications. Nevertheless, the graphene on SiC substrates is still cost ineffective and not compatible with Si technologies.

In this work, we present DC and RF performance of graphene FETs developed on SiC substrates. The graphene transistors are fabricated by the conventional top-down approach, holding the potential of compatibility with other semiconductor materials. An organic polymer film is introduced between graphene and regular gate dielectrics to minimize mobility degradation in top-gated graphene FETs. The output characteristics are nearly linear without clear current saturation before device breakdown. With a gate length of 1 μm and a low field-effect mobility of 40 $cm^2/(V\ s)$, a maximum cutoff frequency of 4.6 GHz and a maximum oscillation frequency (f_{MAX}) of 1.5 GHz were measured.

The graphene was epitaxially grown on SiC. From the intensity ratio of the G peak to SiC substrate peaks and the shape of the 2D peak in the measured Raman spectrum of the graphene [9,10], it can be determined that most of the surface was covered by monolayer graphene, and only in few regions associated with pits bilayers started forming;

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thus, we can consider these graphene sheets to be quasi-monolayer films. Arrays of graphene RF FETs on SiC substrate are fabricated using conventional top-down lithography and processing techniques. The schematic view of the graphene device is shown in Figure 1. The source and drain contacts are formed by optical lithography and lift-off and consist of 10 nm Ti and 50 nm Au. To define the graphene channel and isolate individual devices, regions of graphene are etched in an oxygen plasma using photoresist as the etch mask. The gate dielectric film consists of first 10 nm of an organic seed layer made of benzocyclobutene, followed by an 8 nm film of Al_2O_3 deposited by atomic layer deposition (ALD). Details of the fabrication processes are presented in [11]. Finally, the gate electrodes consisting of Ti/Au metals (10 nm/50 nm) are formed by optical lithography and lift-off. Figure 2 shows an optical image of a dual-channel graphene FET with a gate length of L_G=1 μm. The width of each channel is 20 μm and the spacing between the source and drain electrodes is 2 μm. Electrical measurements of the graphene transistors were performed at room temperature in ambient environments.

It is essential to adopt a proper gate dielectric that does not significantly degrade carrier mobility, allowing for high carrier motilities to be retained in top-gated operation. The composite stacks have been proven to meet the requirements on gate dielectric [11]. Briefly, the gate dielectric layers are deposited on graphene prepared by mechanical exfoliation on SiO_2/Si substrates. Electrical measurements are taken using the Si substrate as the back gate, and no evidence of damage to the graphene in the form of a resistance increase or transconductance decrease is observed with the deposition of the composite dielectrics. Therefore, the introduction of the organic seed layer before Al_2O_3 ALD not only facilitates the high-κ gate Al_2O_3 deposition through

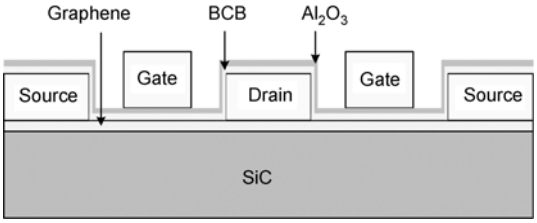

Figure 1 Schematic view of the dual-gate graphene transistor.

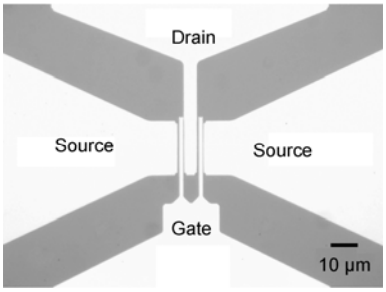

Figure 2 Optical microscope image of a graphene FET.

methyl groups contained within the polymer on the otherwise inert graphene surface but also preserves the intrinsic carrier mobility of the active graphene layer. In addition, the gate leakage current is in the range of ~1 nA/μm^2 or less, which is negligible in the device characterization presented here.

The drain current I_D, measured as a function of gate voltage V_G, as shown in Figure 3, exhibits dominant n-type characteristics, differing from the ambipolar characteristics typically observed in exfoliated and CVD graphene [11]. For all of our graphene FETs, the Dirac point (the current minimum) always occurs at V_G<−6 V. The device transconductance g_m, defined by dI_D/dV_G, is nearly constant over a wide V_G range in the on-state (right axis in Figure 3). The peak extrinsic g_m of 17 mS/mm is measured at drain voltage (V_D) of 3.5 V. The field-effect mobility μ_{FE} defined by $\mu_{FE} = \frac{L \times g_m}{WC_G V_D}$, where C_G is the gate capacitance, is obtained from g_m. With a reasonable value of C_G=1.83×10^{-3} F/m^2 [11], the low-field μ_{FE} is estimated to be ~40 cm^2/(V s) at V_D=0.1 V. One should notice that mobility extracted by this method is inevitably underestimated, because the influences of contact resistance are not excluded [7,11]. The contact resistance plays a dominant role in graphene devices and has an exponentially detrimental impact on the transconductance [12]. However, unlike the case of Si FET devices, there is currently no proven way to reduce the contact resistance of graphene transistors; a greater undertaking is required to reduce this resistance.

The output characteristics of graphene FET are different from those of conventional Si transistors because of the absence of a band gap in graphene [1]. A nearly linear I_D-V_D dependence for all gate voltages is observed up to a drain voltage of 3.5 V as shown in Figure 4, so the device transconductance increases with rising drain voltage for these graphene FETs.

High-frequency scattering parameters (S) of the graphene FETs are measured up to 5 GHz by an Agilent E8363B network analyzer using ground-signal-ground probes. Short and open structures are used to de-embed the signals of the parasitic capacitance and the series resistance associated

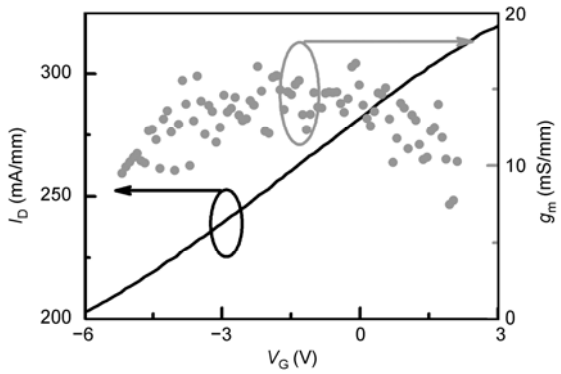

Figure 3 Transfer characteristics of the graphene FET at V_D=3.5 V.

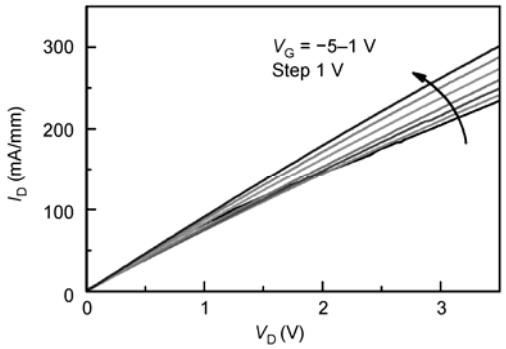

Figure 4 Output characteristics of the graphene FET at different V_G, from −5 to 1 V in steps of 1 V.

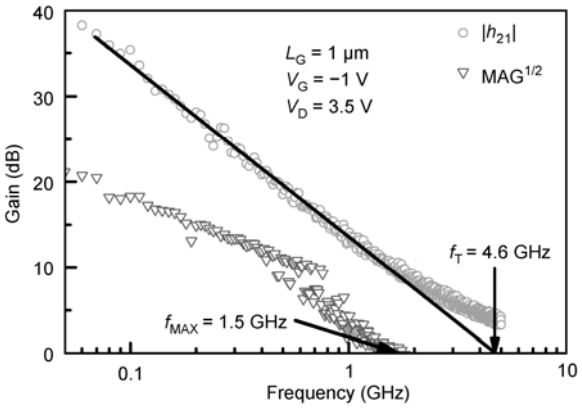

Figure 5 Plot of short circuit current gain (circle) and power gain (triangle) versus frequency. The f_T is 4.6 GHz and the f_{MAX} is 1.5 GHz for the graphene device.

with the pads and connections. This de-embedding procedure is a well-established standard method and is performed using an "open" test structure without graphene and a "short" test device where the gate, source, and drain electrodes are all connected by metals. The layouts of these open and short structures are strictly identical to that of the active device.

Figure 5 shows the measured current gain $|h_{21}|$, after the de-embedding, as a function of frequency for graphene FET. The current gain $|h_{21}|$ is obtained from the measured S parameters using the following formula: $h_{21} = -S_{21}/[(1-S_{11}) \times (1+S_{22}) + S_{12} \cdot S_{21}]$. $|h_{21}|^2$ can be converted into dB by 20log $|h_{21}|$. The current is then plotted against the frequency in log scale, following a 1/f dependence, which is equivalent to −20 dB/decade dependence. This −20 dB/decade frequency dependence suggests a conventional FET-like behavior for graphene transistors. The cutoff frequency f_T, defined as the frequency at which the current gain becomes unity, is one of the most important figures-of-merit for characterizing RF transistors. For our graphene FETs with L_G=1 μm, a maximum f_T of 4.6 GHz is measured at V_D= 3.5 V.

In addition to the current gain, the graphene FETs also possess power gain at gigahertz frequencies, as shown in Figure 5. The maximum frequency f_{MAX} [11] defined as the frequency at which the power gain is equal to one, is measured to be 1.5 GHz for the graphene FET with f_T =4.6 GHz. It is noted that f_{MAX}, unlike f_T, is highly dependent on the device layout and interconnects, including the metal thickness that affects the gate and source/drain resistance. Therefore, f_{MAX} can be further enhanced by optimizing the gate structure, such as decreasing the gate resistance with a thicker metal stack or with a multi-finger gate layout.

In summary, graphene FETs were fabricated on semi-insulating SiC substrates with composite stacks as gate dielectric. Typical n-type characteristics without clear current saturation were observed. Even though only a low field-effect mobility was acquired, epitaxial graphene transistors have already shown decent performance in the GHz frequency range. With further improvement of the quality of the graphene material and optimization of the device structure, graphene RF FETs could achieve more superior performance.

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