

Effect of dummy vias on interconnect temperature variation

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The number of the dummy via can significantly affect the interconnect average temperature. This paper explores the modeling of the interconnect average temperature in the presence of multiple dummy vias. The proposed model incorporates the multi-via effect into the effective thermal conductivity of the interlayer dielectric (ILD) to obtain accurate results. Using different ILDs, the multi-via effect is analyzed and discussed. Also, the extended applications of the multi-via effect are presented in this paper to obtain the minimum interconnect average temperature increase with a given via separation or number. This study suggests that the multi-via effect should be accounted for in integrated circuits design to optimize the performance and design accuracy of integrated circuits.

interconnect modeling, interconnect average temperature increase, multi-via effect, dummy via, interlayer dielectric

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As feature sizes have decreased, a continuous increase in integration density has resulted in higher overall chip temperature, which makes power dissipation and thermal issues a major impediment in the design of ultra large scale integrated circuits (ULSI) [1–3]. Research has shown that on-chip global interconnect self-heating contributes about 34% of the total chip power dissipation in an Intel microprocessor with 130-nm features [4]. Moreover, because of the reduction of the distance between the substrate and the top-most metal layers [5], the substrate temperature variations have an increased effect on interconnect temperature profile. In high-performance integrated circuits (ICs), the peak chip temperature can reach 210°C and the thermal gradients can rise above 50°C when in the GHz frequency regime [6,7]. The temperature distribution can strongly affect the interconnect resistance, and, consequently, the signal integrity of circuits can be degraded.

Furthermore, low-k materials are generally used to reduce the effect on interconnect time delay, crosstalk and dynamic power consumption [8,9]. However, because of the poor thermal conductivity of such materials, most of the

Joule heating produced by the interconnects on every level cannot be transmitted to the heat sink. Therefore it accumulates which leads to a larger interconnect temperature rise. However, vias can effectively reduce interconnect temperature increase. Hence the interconnect temperature will not be not as high would be estimated or the previous circumstance [10–13]. Because of the reasonable thermal conductivity of vias, dummy vias can be introduced to reduce the interconnect temperature in IC design. A dummy via is a kind of via which that used to conduct heat but is not electrically connected [12–15]. The interconnect temperature profile can be strongly affected by the presence of dummy vias. Over-estimation of the interconnect temperature can lead to design failure or unnecessarily conservative design. Therefore, an accurate prediction of interconnect temperature is a necessary precondition for interconnect characterization.

1 Interconnect temperature model with multiple dummy vias

For our model, we assumed that an interconnect exchanges heat with the environment only through the substrate [5]. In

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addition, as shown in Figure 1, for a global interconnect, the temperature in the length direction varies more quickly than in the directions of thickness and width. Therefore, we take only the temperature variation in the length direction into account when solving the equation.

Also, we assume the temperature at interconnect terminals connected by vias is the same as the constant underlying layer temperature, T_{ref} . Therefore, the temperature distribution along an interconnect with thickness t_m , width w_m and length L can be formulated by the following heat diffusion equation [12]:

$$k_m \frac{d^2 T(x)}{dx^2} + j_{rms}^2 \rho_0 [1 + \beta(T(x) - T_{ref})] - j_{rms} \varepsilon \frac{dT(x)}{dx} - \frac{k_{ins} w^*}{t_{ins} t_m w_m} (T(x) - T_{ref}) = 0, \quad (1)$$

where $T(x)$ represents the temperature profile of the interconnect. k_m and k_{ins} are the thermal conductivity of the interconnect and the underlying interlayer dielectric (ILD), respectively. j_{rms} is the uniform root-mean-square current density flowing in the interconnect. ρ_0 is the resistivity of the interconnect at the reference temperature, T_{ref} . β is the temperature coefficient of resistance ($^{\circ}C^{-1}$). ε is the Thomson coefficient. The third term represents the heat loss resulting from the Thomson effect, which is very small and is neglected here. The fourth term is the energy loss due to the heat transmission between the adjacent interconnects through the insulator. t_{ins} is the thickness of the ILDs. w^* is the effective interconnect width for thermal diffusion. By solving eq. (1), we can obtain:

$$T(x) = T_{ref} + \frac{j_{rms}^2 \rho_0}{k_m \alpha^2} \left[1 - \frac{\cosh(\alpha x)}{\cosh(\alpha L/2)} \right], \quad -L/2 \leq x \leq L/2, \quad (2)$$

where

$$\alpha = \sqrt{\frac{k_{ins} w^*}{t_{ins} t_m w_m k_m} - \frac{j_{rms}^2 \rho_0 \beta}{k_m}}, \quad (3)$$

because the fluctuation of the resistivity due to the tem-

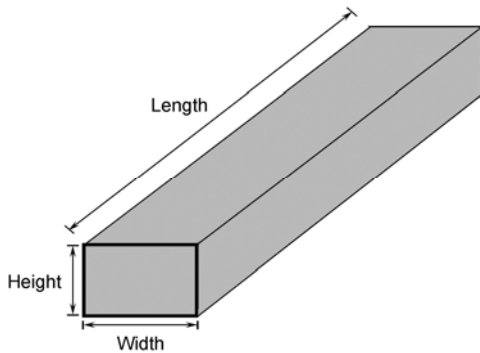


Figure 1 A global interconnect schematic diagram.

perature fluctuation is small enough to be ignored [12], α

$$\text{can be simplified to } \alpha = \sqrt{\frac{k_{ins} w^*}{t_{ins} t_m w_m k_m}}.$$

It is assumed that the number of the vias in the interconnect of interest is n . Because of the via effect, the interconnect average temperature increase T_{avg} can be expressed as the total temperature increase divided by the interconnect length, L :

$$T_{avg} = \frac{1}{L} \sum_{i=2}^n \int_{l_i} [T_n(x) - T_{ref}] dx, \quad (4)$$

where $T_n(x)$ is the temperature profile between via $n-1$ and via n . L is the total interconnect length, l_i is the distance between via $i-1$ and via i . Let the number of the vias be even (eight vias for example) and the vias in the cooling area are equidistantly arranged. The detailed temperature increment with multiple dummy vias is shown in Figure 2.

Let T_l be the average temperature increase of the main interconnect, and let T_v be the average temperature increase of the interconnect of length l between adjacent vias in the cooling area. The average temperature increase T_l and T_v can be expressed as

$$T_l = \frac{j_{rms}^2 \rho_0}{k_m \alpha^2} \int_{-\frac{L-n-2l}{2}}^{\frac{L-n-2l}{2}} \left[1 - \frac{\cosh(\alpha x)}{\cosh\left(\frac{1}{2} \alpha (L - nl + 2l)\right)} \right] dx \\ = \frac{j_{rms}^2 \rho_0 [L - (n-2)l]}{k_m \alpha^2} \left[1 - \frac{\tanh\left(\frac{1}{2} \alpha (L - nl + 2l)\right)}{\frac{1}{2} \alpha (L - nl + 2l)} \right], \quad (5)$$

$$T_v = \frac{j_{rms}^2 \rho_0}{k_m \alpha^2} \int_{-\frac{l}{2}}^{\frac{l}{2}} \left[1 - \frac{\cosh(\alpha x)}{\cosh\left(\frac{1}{2} \alpha l\right)} \right] dx \\ = \frac{j_{rms}^2 \rho_0 l}{k_m \alpha^2} \left[1 - \frac{\tanh\left(\frac{1}{2} \alpha l\right)}{\frac{1}{2} \alpha l} \right]. \quad (6)$$

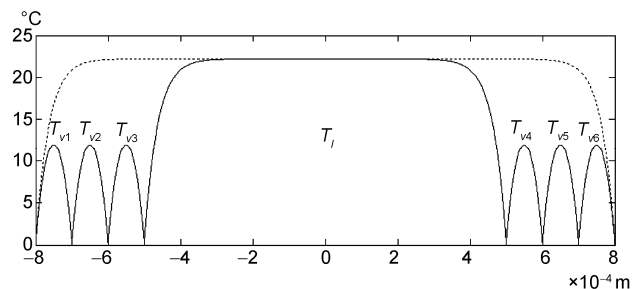


Figure 2 Temperature profile for an interconnect with multiple vias. The solid line represents the temperature profile of an interconnect that has multiple dummy vias, and the dotted line represents the thermal distribution of the same interconnect with only two vias.

temperature increase, T_{avg} , can be expressed as

$$T_{avg} = \frac{1}{L} [T_l + (n-2)T_v]$$

$$= \frac{j_{rms}^2 \rho_0}{k_m \alpha^2 L} \left\{ \begin{array}{l} L - \frac{\tanh\left[\frac{1}{2}\alpha(L-(n-2)l)\right]}{\frac{1}{2}\alpha} \\ -(n-2) \frac{\tanh\left(\frac{1}{2}\alpha l\right)}{\frac{1}{2}\alpha} \end{array} \right\}. \quad (7)$$

2 Effect of multiple dummy vias on thermal conductivity of the ILDs

Dummy vias have different effects on the average temperature increase for different ILDs [12]. To obtain the correct interconnect temperature increase, the effect of multiple dummy vias can be incorporated into the effective thermal conductivity during the analysis of interconnect characteristics. The average interconnect temperature increase can be expressed as

$$T_{avg}^* = j_{thermal} R_{thermal} = \frac{j_{rms}^2 \rho_0 t_m t_{ins} W}{k_{ins}^* W^*}, \quad (8)$$

where $R_{thermal}$ represents the thermal resistance of the interconnect. $j_{thermal}$ is the heat transfer rate. k_{ins}^* is the effective thermal conductivity of ILD. If we set eqs. (7) and (8) to be equal:

$$T_{avg} = T_{avg}^*, \quad (9)$$

and solving eq. (9), we obtain:

$$k_{ins}^* = k_{ins} \left\{ \begin{array}{l} \tanh\left[\frac{1}{2}\alpha(L-nl+2l)\right] \\ -(n-2) \tanh\left(\frac{1}{2}\alpha l\right) \\ 1 - \frac{\tanh\left(\frac{1}{2}\alpha l\right)}{\frac{1}{2}\alpha L} \end{array} \right\}^{-1}. \quad (10)$$

We define ξ as the dummy via correction coefficient, and it is expressed as

$$\xi = \left\{ \begin{array}{l} \tanh\left[\frac{1}{2}\alpha(L-nl+2l)\right] \\ -(n-2) \tanh\left(\frac{1}{2}\alpha l\right) \\ 1 - \frac{\tanh\left(\frac{1}{2}\alpha l\right)}{\frac{1}{2}\alpha L} \end{array} \right\}^{-1}. \quad (11)$$

Therefore,

$$k_{ins}^* = k_{ins} \xi. \quad (12)$$

Using eq. (11) we find that the value of ξ is larger than 1, and it increases as n becomes larger. Accordingly, the low-k dielectrics become more thermally conductive, because of the presence of the dummy via. Table 1 shows the effect of the dummy via number on the effective thermal conductivity for different ILDs.

Table 1 shows the multi-via effect on the conductivity for three kinds of dielectrics, SiO₂, Orion and air. From the table it can be seen that the lower the nominal thermal conductivity, the more the via number effects the effective thermal conductivity of a low-k dielectric. When $n = 10$, the effective thermal conductivity of the air becomes 0.064 W/m K, which is almost twice its nominal thermal conductivity. Also, the effective thermal conductivity is doubled when $n = 30$ for Orion and when $n = 78$ for SiO₂.

The relationship between the interconnect average temperature increase (°C) and the via number for different ILDs is shown in Table 2, where

$$\eta = \frac{T_{avg}(n=2) - T_{avg}(n>2)}{T_{avg}(n=2)} \times 100\%. \quad (13)$$

From Table 2, it can be seen that the interconnect average temperature increase for ILDs with low thermal conductivities are larger than those for ILDs with high thermal conductivities. However, the via effect is more sensitive to n for low-k dielectrics. For example, with air as the ILD, the interconnect average temperature increase is 105.13°C when $n = 2$, and it is 43.60°C when $n = 12$, which is less than 50% of the original temperature increment. This is the reason why the interconnect average temperature increase is not as high as commonly estimated when low- k materials are used in advanced interconnect structures. As a result, increasing the number of dummy vias is a simple and effective way to decrease the interconnect average temperature

Table 1 Influence of the dummy via number on the effective thermal conductivity for different ILDs^{a)}

	$n=2$	Change rate (%)	$n=4$	Change rate (%)	$n=6$	Change rate (%)	$n=8$	Change rate (%)	$n=10$	Change rate (%)	$n=12$	Change rate (%)
k_{SiO_2}	1.055	1.44	1.069	2.79	1.083	4.13	1.098	5.58	1.113	7.02	1.129	8.56
k_{Orion}	0.166	3.75	0.173	8.13	0.179	11.86	0.186	16.25	0.194	21.25	0.202	26.25
k_{Air}	0.034	13.33	0.038	26.67	0.044	46.67	0.052	73.33	0.064	113.33	0.081	170.00

a) The unit of thermal conductivity is $W m^{-1} K^{-1}$; the nominal thermal conductivities of SiO₂, Orion and air are 1.04, 0.16 and 0.03 $W m^{-1} K^{-1}$, respectively [13].

increase.

3 Extension of the application of the multi-via effect

When n is constant and $l = L/(n-1)$, the interconnect average temperature increase is minimized. The minimum interconnect average temperature increase is given as follows:

$$T_{\text{avg_min}} = \frac{j_{\text{rms}}^2 \rho_0}{k_m \alpha^2} \left[1 - (4n-8) \frac{\tanh\left(\frac{\alpha L}{2n-2}\right)}{\alpha L} \right]. \quad (14)$$

Interconnect average temperature increase is dependent on the separation of the dummy vias. Figure 3 shows the relationship between the interconnect average temperature increase and via separations for 65-nm technology [16].

Let n be 11, and let the interconnect length be 2000 μm . We used seven different via separations, namely, 50, 80, 100, 150, 200, 210 and 220 μm , to analyze the effect of via separation on interconnect average temperature increase. From Figure 3, it can be seen that the minimum interconnect average temperature increase happens at $l = 200 \mu\text{m}$. It can also be seen that the change of interconnect average temperature increase varies smoothly over the range $l = 80\text{--}210 \mu\text{m}$ for an SiO_2 ILD. However, the interconnect average temperature increase changes significantly for different via separations as the thermal conductivity is reduced, which is shown in Figure 3(b) and (c). As a result, for a constant number of the dummy vias, we can adjust the via separation to reduce the interconnect temperature increase and decrease the power dissipation.

For a given l , using eq. (7), the interconnect average temperature increase is minimized when

$$n = \left\lceil \frac{\alpha L + 2\alpha l + 2 \tanh^{-1} \left[\frac{\sqrt{\alpha l (e^{\alpha l} + 1) (-2e^{\alpha l} + 2 + \alpha l e^{\alpha l} + \alpha l)}}{\alpha l (e^{\alpha l} + 1)} \right]}{\alpha l} \right\rceil. \quad (15)$$

For a constant interconnect length ($l = 200 \mu\text{m}$), the number of the dummy vias vs. the interconnect average temperature increase is shown in Figure 4.

In Figure 4, it can be seen that the average interconnect temperature increase has an approximately linear relationship with via number. The increased the thermal conductivity of the ILD is, the more linear the relation is. Therefore, the via number can be estimated by the calculated temperature increase for a constant via separation.

4 Conclusion

A novel analytical model for analyzing the interconnect average temperature increase in the presence of multiple vias is developed in this paper. The proposed model incorporates the multi-via effect into the thermal conductivity of the ILD to obtain a more accurate calculation of the interconnect average temperature increase. For a number of different ILDs, this paper discusses the interconnect average temperature increase in terms of the multi-via effect. We concluded that the multi-via effect has a significant effect on the effective thermal conductivity of the ILD. Moreover, two extended applications of the proposed model are presented. Using these applications, we can minimize the interconnect average temperature increase to decrease the power dissipation of the interconnect. The proposed model can help IC designers estimate the interconnect average temperature increase, modify the interconnect arrangement and obtain the expected interconnect average temperature increase. Likewise, the proposed model with the multi-via

Table 2 Multi-via effect on the interconnect temperature increase for different ILDs

	$n=2$	$n=4$	η (%)	$n=6$	η (%)	$n=8$	η (%)	$n=10$	η (%)	$n=12$	η (%)
ΔT_{SiO_2}	3.37	3.32	1.48	3.28	2.67	3.24	3.86	3.19	5.34	3.15	6.53
ΔT_{Orion}	21.38	20.62	3.55	19.85	7.16	19.09	10.71	18.32	14.31	17.56	17.87
ΔT_{Air}	105.13	92.82	11.71	80.51	23.42	68.21	35.12	55.91	46.82	43.60	58.53

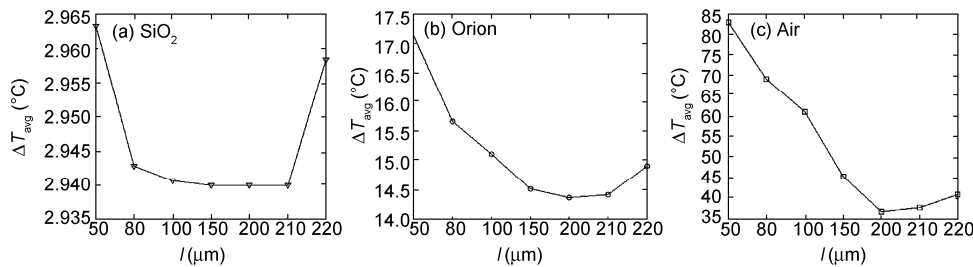


Figure 3 Interconnect average temperature increase for different via separations at constant n .

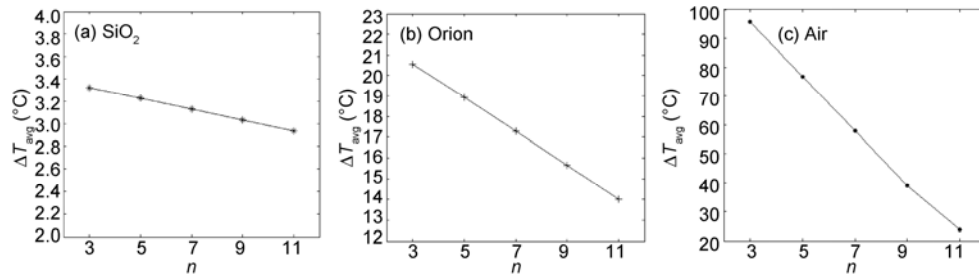


Figure 4 Relationship between the interconnect average temperature increase and via number for a constant l .

effect can also be used to research and improve models of interconnect delay, crosstalk and power dissipation.

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