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EDITORIAL

Guest Editors' Introduction

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This special issue contains a selection of papers on design and implementation of signal processing systems. The papers span a broad range of topics including hardware, software, reconfigurable architecture, and algorithm-architecture co-design techniques for signal processing systems.

In *A Bit-rate Aware Scalable H.264/AVC Deblocking Filter using Dynamic Partial Reconfiguration*, Khraisha and Lee develop a dynamically reconfigurable FPGA architecture for deblocking filter computation, which accounts for a significant portion of decoder complexity in H.264/AVC. The architecture is designed for flexible adaptation to diverse operating requirements including those involving resolution, frame rates, and bit rates. The architecture is demonstrated through implementation on a Xilinx Virtex-4 device.

In *Flexible and Expandable Speech Recognition Hardware with Weighted Finite State Transducers*, You, Choi, and Sung demonstrate and compare two alternative system architectures for real-time continuous speech recognition based on weighted finite state transducer (WFST) networks. The first architecture employs SRAM storage to manage the working set during processing, while the second employs DRAM as working set storage to promote expandibility. As part of the second architecture, a split DRAM hash table organization is proposed to help hide the longer memory latencies. A detailed experimental study of the two architectures is presented based on FPGA implementation.

In *Efficient Generalized Minimum-distance Decoders of Reed-Solomon Codes*, Zhu and Zhang propose an interpolation-based one-pass scheme to be used in decoding Reed-Solomon codes. The objective of the work is low-complexity and the implementation studies on 180 nm ASIC technology show significant improvement in throughput with negligible increase in area compared to previous solutions. The savings in complexity are obtained with the aid of a novel polynomial selection scheme and a search architecture used to implement the scheme.

In *Design of Sparse Filters for Channel Shortening*, Chopra and Evans propose methods for designing filters containing a small number of non-contiguous non-zero coefficients. The paper evaluates the impulse response energy compaction and analyses the computational complexity of these sparse filters. The proposed filters are applied to ADSL channels and underwater acoustic communication channels and simulations show the same energy compaction with half the number of coefficients compared to dense filters.

In *Hardware Emulation of Wideband Correlated Multiple-Input Multiple-Output Fading Channels*, Ren and Zheng develop a low-complexity FPGA based

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emulator for wideband, correlated, multiple-input multiple-output (MIMO) fading channels. The Kronecker products employed for modeling channel functions are implemented by a mixed parallel-serial (mixed P-S) method for reducing memory storage while meeting the real-time requirement.

In *Mapping Parameterized Cyclo-static Dataflow Graphs onto Configurable Hardware*, Kee, Shen, Bhattacharyya, Wong, Rao, and Kornerup develop a scheduling technique for efficient FPGA-based implementation of dataflow that supports dynamic parameter change. The developed scheduling technique is integrated with an existing formal scheduling model, and also demonstrated with a subset of the long-term evolution (LTE) communication standard.

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