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Guest Editorial

Special Issue on Signal Processing Circuits and Systems for Broadband Communications

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Over the past 10 years, broadband communications have become the major focus for industry for offering rich multimedia services. As new video-rich and bandwidth-hungry services are developed, the challenge to deliver the next generation broadband services is becoming more profound. In addition, energy-efficient circuits and systems for broadband communications require systematic optimization at all levels of design abstraction ranging from process technology and logic design to architectures and algorithms.

However, the straightforward VLSI implementation of broadband communication systems is associated with considerable silicon area and high power consumption. These issues pose unprecedented challenges for the design and implementation of highly practical and reliable circuits and systems for broadband communications. The signal processing research for broadband communications needs to address a plurality of issues ranging from the development of high-speed signal processing techniques to the implementation of compact transceiver architectures with low power consumption. In addition, the signal processing technology for broadband communications requires more studies not only from the perspective of wireless systems, but also in the area of high-speed optical and satellite communication systems.

This special issue intends to present the latest state-of-the-art research results in the area of signal processing circuits and systems for broadband communications. The topics included range from algorithm development to implementation and system design. All papers were thoroughly reviewed according to the standard peer review process of the *Journal of Signal Processing Systems*.

The first two papers provide interesting insights into Reed-Solomon (RS) Decoders. "Modified Low-Complexity Chase Soft-Decision Decoder of Reed-Solomon Codes," by Xinmiao Zhang, et al. exploits the low-complexity Chase (LCC) algorithm, which can achieve better performance-complexity tradeoff compared to other decoding algorithms of RS codes. Through adding common erasures to the test vectors, a modified LCC (MLCC) decoding is proposed to combat inter-symbol interference. It leads to significant reductions on both silicon area and average decoding latency without incurring any performance loss. The second paper, "Three-Parallel Reed-Solomon Decoder using S-DCME for High-Speed Communications," by Jae Do Lee et al. proposes a high-speed and area-efficient three-parallel RS decoder. The high throughput and efficiency are achieved through computing the inner signals in parallel and solving the key equation using the simplified degree computationless modified Euclid (S-DCME) algorithm.

The next two papers focus on the design of a Turbo decoder for multi-standards and a BCH decoder for 100Gb/s optical communications. "Implementation of a Radix-4, Parallel Turbo Decoder and Enabling the Multi-Standard Support," by Rizwan Asghar et al. offers a unified architecture supporting radix-4 turbo decoders for multiple standards such as DVB, WiMAX, 3GPP-LTE and HSPA Evolution. The support of multi-standards is mainly achieved through modifying the schemes for Turbo code interleavers used in different standards. The proposed architecture achieves smaller silicon area, lower power consumption and higher throughput, while maintaining reconfigurablity on-the-fly. The paper "A High-Speed Low-Complexity Concatenated BCH Decoder Architecture for 100Gb/s Optical Communications," by Kihoon Lee et al. presents a two-iteration concatenated Bose-Chaudhuri-Hocquenghem (BCH) code and its high-speed low-complexity two-parallel decoder architecture for 100 Gb/s optical communications. The proposed architecture features a very high data processing rate as well as excellent error correction capability.

The fifth paper presents a time-division multiplexing (TDM) switch integrated circuit (IC). It is "An 8×8 20Gbps Reconfigurable Load Balanced TDM Switch IC for High-

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Speed Networking" by Ching-Te Chiu, et al. In this paper, the authors fold the two-stage switch to reduce 50% hardware complexity, and then implement a prototype switch fabric IC, including a digital 8×8 switch core, eight SERDES ports with I/O interfaces and a phase-lock loop, in 0.18 μm CMOS technology. Measurements show that the 8×8 switch fabric IC can achieve 20Gbps switching rate and consumes only about 690 mW power.

The last paper, "On the Achievable Rate for Wideband Channels with Estimated CSI," by Jinho Choi et al. attempts to find the achievable rate for frequency-selective fading channels when the channels are to be estimated. Since some portion of the radio resources is consumed to estimate the channel state information (CSI), it should be taken into account in finding the achievable rate. This work is useful in designing flexible radio systems such as software defined radio.

We would like to thank the authors for their work in submitting and revising the manuscripts. It has been gratifying to learn more about the advances of signal processing circuits and systems for broadband communications. We also wish to express our deepest gratitude for the efforts of the reviewers. This special issue is only possible with their expert help.

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Guest Editor

Myung H. Sunwoo received the B.S. degree in Electronic Engineering from the Sogang University in 1980, the M.S. degree in Electrical and Electronics from the Korea Advanced Institute of Science and Technology in 1982, and the Ph.D. degree in Electrical and Computer Engineering from the University of Texas at Austin in 1990.

He worked for Electronics and Telecommunications Research Institute (ETRI) in Daejeon, Korea from 1982 to 1985, and Digital Signal Processor Operations, Motorola, Austin, TX from 1990 to 1992. Since 1992, he has been a Professor with the School of Electrical and Computer Engineering, Ajou University in Suwon, Korea. In 2000, he was a Visiting Professor at the University of California, Davis, CA.

He has authored over 370 papers and also holds 50 patents. He received 28 research awards including the Best Student Paper Award from the IEEE Workshop on Signal Processing Systems (SiPS) 2005, International SoC Conference (ISOCC) in 2003, 2005, 2008, 2009, and IEEE Seoul Section in 2004, the Ministry of Commerce, Industry and Energy, Samsung Electronics, and the Institute of Electronics Engineers of Korea (IEEK). His research interests include low power SOC architectures, design for multimedia and communications, and application-specific design.

He will serve as General Chair of International Symposium on Circuits and Systems (ISCAS) 2012, Korea. He served as Technical Program Chairs of the IEEE Workshop on SiPS in 2003, General Co-Chair of ISOCC and General Chair of the IEEK SOC Conference in 2008. He has been a TPC for numerous conferences and societies including IEEE SiPS, Cool Chips, Design, Automation and Test in Europe (DATE), Asian-Pacific Conference on CAS (APC-CAS), Asian-Solid State Circuits Conference (A-SSCC), ISOCC, Asia Symposium on Quality Electronic Design (ASQED), IEEE BioCAS, International Symposium on VLSI Design, Automation and Test (VLSI-DAT), etc, Associate Editor for the IEEE Transactions on Very Large Scale Integration (VLSI) Systems (2002–2003), Guest Editor for the Journal of VLSI Signal Processing (Kluwer, 2004) and will serve on the Guest Editor for the Journal of Signal Processing Systems (Springer, 2011). He is listed in MARQUIS Who's Who in the world, in Science and Engineering, in Asia and International Biographical Centre.

He is the IEEE Circuits and Systems Society (CASS) Board of Governor (BoG) since 2011 and was a Distinguished Lecturer of the IEEE CASS until 2010. He was a Director of the National Research Laboratory sponsored by the Ministry of Science and Technology, a Director of the New Growth Engine Semiconductor Center, and an Executive Director of IEEK. He is a Vice President of the IEEK Semiconductor Society and he was a Chair of the IEEK SOC Design Technical Committee. He was an honorary ambassador of Korean Tourism Organization. He is a Chair of the IEEE CASS, Seoul Chapter and a Fellow of IEEE.