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EDITORIAL

Special Issue on Signal Processing for Software Defined Radio Handsets

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The ultimate objective of Software Defined Radio (SDR) is to replace the entire analog signal processing in the wireless transceivers with digital signal processing. This will provide the flexibility, through reconfiguration or reprogramming, to enable the transceivers to work with different air-interfaces standards using a single generic hardware platform. Most of the research in SDR to date has been focused on base stations, which do not have as tight constraints in size and power consumption as handsets. However, in order to realize the promise of integrated services and global roaming capabilities, the design and development of a multi-standard SDR handset with dynamic reconfigurability is crucial. The size and power constraints imposed by handsets with limited resources pose a major design challenge. This special issue brings together 11 papers that address various aspects of this challenge from the perspectives of wireless systems, computing architectures, embedded systems and signal processing.

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The most important part of an SDR transceiver is the wideband analog-to-digital converter (ADC) that converts the radio frequency signal received by the antenna into digital form for further processing. The first paper, "A multi-mode sigma-delta ADC for GSM/WCDMA/WLAN applications" by Jose et. al. proposed a cascaded reconfigurable sigma-delta modulator that is able to work with three different communication standards. This design, implemented in 0.18 μm CMOS technology, exhibits excellent signal-to-noise plus distortion ratios and has reduced power consumption compared to conventional designs.

After ADC, the digitized received signal will need to be separated into signals within the various bands specified by the communication standard. This is performed by the channelizer which has the highest computational requirements of the whole SDR system. The second paper, by Panicker et al., reviews the state-of-the-art filter bank channelizer techniques with low power and dynamic reconfigurability properties.

The design of reconfigurable devices can be optimized using the methodology of parametrization which bring together the common aspects of a myriad number of wireless standards into a single processing procedure. In this way, the implementation of the multi-standard SDR will be greatly simplified. "Promising technique of parametrisation for reconfigurable radio, the Common Operators Technique: fundamentals and examples" by Alaus et al. presents the common operator technique for parametrization which is less standards dependent than the more conventional Common Function technique.

The direct digitization of the radio frequency (RF) signal requires very high speed ADCs which is not readily available using current technology. Therefore, current SDR implementations typically down-converts the RF

signal to an intermediate frequency (IF) which is then sampled. Zero IF is one popular technique being deployed. In the fourth paper, Ramasamy and Venkataramani proposed a new analog baseband processing block, consisting of a variable gain amplifier anda low-pass filter which can be digitally tuned between 100 kHz and 20 MHz which a maximum power consumption of 5 mW.

This special issue continues with three papers that propose new digital signal processing architectures useful for SDR. Smitha and Vinod described a low complexity, low power, reconfigurable channel filter architecture based on a multi-stage frequency response masking technique. The high-speed computation of discrete Fourier transforms of arbitrary lengths is discussed by Meher et al. in "Efficient systolic design for 1 and 2-dimensional DFT of general transform lengths for high-speed wireless communication applications" previously published in Volume 60, Issue 1, 2010, pages 1–14, under doi:10.1007/s11265-008-0328-x. Amiri et. al. address the issue of multi-user detection for multiple-input multiple-output (MIMO) wireless communications. A high throughput configurable detector is proposed and implemented in FPGA that supports 4, 16, 64 QAM with up to 4 antennas/users.

For SDRs operating within a system with multiple antennas with multiple modulation carriers, the paper by Kurniawan et al. addresses the operational issue of optimal antenna selection. They proposed a sub-optimal low complexity scheme with acceptable performance.

SDR is the enabling technology for cognitive radio (CR). CR technology allows wireless communication systems to use those portions of the scarce radio spectrum for transmission when it is not in use by the primary users. Some aspects of CR is covered by the remaining three papers in this special issue. Eghbali et al. proposed two solutions that supports different bandwidths and centre frequencies for a large set of users. These solutions only require a small modification to current hardware platforms. The problem of spectrum sensing using filter banks is addressed in the paper by Lin et al. They proposed a multi-stage coefficient decimation filter bank that features significantly reduced hardware complexity compared to the conventional discrete Fourier transform filter banks. Finally, "Spectrum occupancy statistics and time series models for cognitive radio" by Wang and Salous proposed a model of spectrum occupancy using time series analysis that will help cognitive radios better predict and detect spectrum holes.

It is our hope that this issue adequately summarizes the state-of-the-art in SDR-based handset technology and provides useful insights for further research in this area. We sincerely thank the authors and the reviewers for their contributions.

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