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EDITORIAL

Guest Editorial: Special Issue on Reconfigurable Video Coding

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More than 20 years of active research on multimedia coding technology have generated a rich variety of successful and complex coding algorithms such as MPEG-2, MPEG-4 AVC. However, besides these monolithic codecs, by selecting only components of these algorithms codec designers could be able to generate new codec profiles achieving useful tradeoffs between compression performances and implementation complexity. Currently, interoperability demands that such selection process is "hard-wired" into the normative description of the codec and their profiles. A significant research effort, called Reconfigurable Video Coding (RVC), is currently undertaken by the ISO/IEC MPEG committee in order to increase the flexibility by which the variety of algorithmic options can be included or excluded from codecs keeping them standard and thus guarantying interoperability. The MPEG Reconfigurable Video Coding (RVC) framework is a new ISO/IEC standard, currently under its final stage of development aiming at providing video codec specifications at the level of coding tool libraries of monolithic descriptions.

The final objective of the RVC approach is to enable building arbitrary combinations of video coding algorithms taken from a unified standard library, without additional standardization steps. This is done by defining an infrastructure that provides the information enabling to specify the decoding process associated to a specific content. The information consists essentially of the description of the decoder configuration. Decoder configuration information is constituted by the description of the interconnections between algorithmic components. The approach is based on new specification formalism for describing all these algorithmic components in the form of dataflow components based on the programming paradigm of the dataflow-oriented CAL language and of an XML dialect for the description of the codec configurations. This language has been found to be appropriate for describing complex signal processing applications. The programming paradigm is based on a processing entity called actor or Functional Unit (FU) in MPEG terminology that represents the lower granularity of each algorithmic components in the standard library.

The special issue intends to summarize and divulgate the status of the RVC standardization process, the scientific problem addressed so far, the open issues, the tools needed to support video reconfiguration capabilities on reconfigurable platforms and the methodologies for codec reconfiguration and deployment.

This special issue begins with a paper that provides an overview of the MPEG RVC framework, authored by Bhattacharyya et al., from the capture of an RVC

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application within the RVC framework to its final implementation on a platform. The RVC framework is supported by the opensource Open Dataflow initiative composed of a simulator, code analysis and code generators.

The features of the Open Dataflow platform is highlighted by three papers describing code analysis and direct software and hardware synthesis of an MPEG RVC description over different platforms. They are

- "Software Code Generation for the RVC-CAL Language" authored by Wipliez et al., that describes the direct synthesis exemplified by the design case of an MPEG-4 Simple Profile decoder. The different translation steps from the CAL description to the C implementation are carefully detailed and discussed.
- "Synthesizing Hardware from Dataflow Programs" authored by Janneck et al, that describes how direct synthesis of an MPEG-4 SP decoder dataflow description can outperform a hand written VHDL version in terms of both throughput, silicon area and design resources.
- "Quasi-Static Scheduling of CAL Actor Networks for Reconfigurable Video Coding" from Boutellier et al. proposes a Parametrized Synchronous Data Flow approach supporting an efficient scheduling of MPEG RVC applications.

The possibility of selecting a subset of standard video coding algorithms within the MPEG RVC formalism to specify a decoder that satisfies application specific constraints is a very attractive option. However, such possibility to reconfigure codecs requires systematic procedures and tools capable of describing the new bitstream syntaxes generated by such new codecs. Moreover, it becomes also necessary to generate the associated parsers, capable of parsing the new bitstreams.

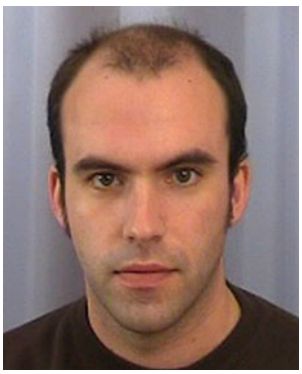
The next paper will describe the technologies needed for the automatic synthesis of a parser from the standard XML representation namely Bistream Syntax Description Language (BSDL): "Automatic Synthesis of Parsers and Validation of Bitstreams Within the MPEG Reconfigurable Video Coding Framework" from Lucarz et al..

The paper "Reconfigurable Architecture for Deinterlacer based on Algorithm/Architecture Co-Design" from Lee and al. will reflect that concurrency can be explored by an algorithm/architecture co-design methodology based on the CAL modeling of a deinterlacer dataflow application. The proposed algorithm and architecture design of deinterlacer with such methodology is more cost-efficient than other works.

The main goal of the last paper "CAL Dataflow Components for an MPEG RVC AVC Baseline Encoder" from Aman-Allah et al. is twofold:

- to demonstrate the flexibility and ease that is provided by RVC-CAL, which allows for efficient implementation of the presented encoder,
- to shed light on the advantages that can be brought into the RVC framework by including such encoding tools.

We hope this special issue provides enlightening information on the MPEG RVC framework and all supporting tools that can provide simulation and direct synthesis of high level description of MPEG RVC codecs. We would like to thank all the authors for their valuable contributions to the content of this special issue.



Mickaël Raulet received his postgraduate certificate in signal, telecommunications, images, and radar sciences from Rennes University in 2002, and his Engineering degree in electronic and computer engineering from National Institute of Applied Sciences (INSA), Rennes Scientific and Technical University. Next in 2006, he received a Ph.D. degree from INSA in electronic and signal processing in collaboration with the software radio team of Mitsubishi Electric ITE (Rennes – France). He is currently in the Institute of Electronics and Telecommunications of Rennes (IETR) where he is a research engineer in rapid prototyping of standard video compression on embedded architectures (multi DSP architecture). Since 2007, he is involved in the ISO/IEC JTC1/SC29/WG11 standardization activities (better known as MPEG) such as a Reconfigurable Video Coding Expert.

Marco Mattavelli started his research activity at the "Philips Research Laboratories" of Eindhoven in 1988 on channel and source coding for optical recording, electronic photography and signal processing of HDTV. In 1991 he joined the "Swiss Federal Institute of Technology" (EPFL) where he got his PhD in 1996. He has been a chairman of a sub group of MPEG ISO/IEC standardization committee. For his work he received the ISO/IEC Award in 1997 and 2003. He is currently leading the "Multimedia Architectures Research Group" at EPFL. His current major research activities include methodologies for specification and modeling of complex systems, architectures for video coding, high speed image acquisition and video processing systems, applications of combinatorial optimization to signal processing. He is the author of more than 100 publications and has served as invited editor for several conferences and scientific journals.

Jörn W. Janneck graduated from the University of Bremen in 1995, worked for the Fraunhofer Institute for Material Flow and Logistics in 1996, and then pursued graduate studies at the ETH Zurich, where he received his Dr. sc. techn. in 2000. From 2000 to 2003 he worked as a visiting scholar at the University of California at Berkeley as a member of the Ptolemy group. In 2003 he joined the Xilinx Research Labs, where he focuses on highlevel programming methodologies for FPGAs, and in particular on dataflow. His research interests include concurrency, programming languages, compilers, and the engineering of parallel computing systems. He has worked in a variety of application areas, including material flow modeling and simulation, image and video coding and processing, wireless communications, distributed algorithms and simulation, and discrete-event modeling of complex electro-mechanical systems.