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Editorial

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This special issue contains a selection of the best papers from the 2007 IEEE ESTIMedia workshop, which is part of the Embedded Systems Week. ESTIMedia is intended to be a forum for specialists from academia and industry for defining design methodologies, architectures and circuits for future embedded multimedia systems. Today, the design process for high-end multimedia systems has become a crucial bottleneck due to the increasing complexity of both the software and the underlying hardware, coupled with shortened time-to-market pressures. While there has been a notable growth in the use and applications of multimedia systems and in the evolution of system-on-chip design technology, there are still enormous opportunities for improving design productivity in this domain. Given this backdrop, the aim of ESTIMedia is to bring together people from different multimedia-related research communities (e.g., software, architectures, real-time systems, DSP, compilers, multimedia applications) who have worked separately, but did not interact sufficiently to address the challenges facing the design of hardware and software for multimedia systems.

In the 2007 edition of ESTIMedia, the workshop featured 19 high-quality technical papers, which have been selected after a thorough review process in which each submitted paper received on average 4.2 reviews. From these 19 papers, we selected seven papers for this special issue, which were again subjected to a rigorous review process. The selected papers cover a wide range of topics in the scope of embedded multimedia systems.

In "Energy-Efficient Streaming Using Non-Volatile Memory", Mohammed G. Khatib et al. show that energy can be saved for predominantly streaming workloads by connecting the system's disk to the DRAM via a large non-volatile memory (NVM). In their approach, the NVM acts as a traffic reshaper from the disk to the DRAM.

In "Run-time Task Overlapping on Multiprocessor Platforms", Zhe Ma et al. address dynamic Pareto-optimal scheduling on multiprocessor systems. They propose a simple yet powerful on-line technique that performs task overlapping by run-time subtask re-scheduling. By doing so, a multiprocessor system with concurrent tasks can achieve better performance without extra energy consumption.

In "Optimizing the H.264/AVC Video Encoder Application Structure for Reconfigurable and Application-Specific Platforms", Muhammad Shafique et al. propose an optimized application structure for the H.264 encoder which is suitable for application-specific and reconfigurable hardware platforms. The proposed application structural optimization for the computational reduction of the Motion Compensated Interpolation is independent of the actual hardware platform that is used for execution.

In "Code and Data Placement for Embedded Processors with Scratchpad and Cache Memories", Yuriko Ishitobi et al. propose a code placement problem, its Integer Linear Programming formulation, and a heuristic algorithm for reducing the total energy consumption of embedded processor systems including a CPU core, on-chip and off-chip memories. The approach exploits a non-cacheable memory region for an effective use of cache memory and, as a result, reduces the number of off-chip accesses.

In "Still Image Processing on Coarse-Grained Reconfigurable Array Architectures", Matthias Hartmann et al.

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investigate the mapping of two typical image processing algorithms, wavelet encoding and decoding, and TIFF compression, on a novel type of coarse-grained reconfigurable array architectures (ADRES) and its corresponding DRESC compiler in a systematic way.

In "A High-level Microprocessor Power Modeling Technique based on Event Signatures", Peter van Stralen et al. present a technique for high-level power estimation of microprocessors. The technique operates at a higher level of abstraction than commonly-used instruction-set simulator based power estimation methods, thus achieving good evaluation performance. As a consequence, the technique can be useful in the context of early system-level design space exploration of multimedia systems.

In "A Safari Through the MPSoC Run-Time Management Jungle", Vincent Nollet et al. provide a detailed survey on MPSoC run-time management functionality and its design space trade-offs. They substantiate the run-time components and the implementation trade-offs with academic state-of-the-art solutions and give a brief overview of some industrial multiprocessor run-time management examples.

We would like to thank all the authors who submitted manuscripts for this special issue. Special thanks go to all the reviewers for their valuable comments, criticism, and suggestions. The investment of their time and insight is very much appreciated and helped to generate this selection of high quality technical papers.

We also appreciate the support from the ESTIMedia organization as well as the editor-in-chief and publisher of the Journal of Signal Processing Systems for organizing this special issue.

Mladen Berekovic has received the Dipl.-Ing. and Dr.-Ing degrees both from the University of Hannover, Germany, in electrical and computer engineering. He has been Research Assistant with the Institute for Microelectronic Systems at the University of Hanover where he worked on several programmable video processor chips for MPEG-4 and image processing. After his PhD he worked at IBM on processor development and at IMEC as a senior researcher for advanced architectures. At IMEC he was leading teams on reconfigurable architectures and ultra-low-power DSPs. Prof. Berekovic was part-time assistant professor at the computer engineering department of Delft University of Technology, the Netherlands. Since 2007 he is professor at Technische Universität Braunschweig, Germany. His present research interests include low-power VLSI implementations for signal processing, DSP and processor architectures for multimedia and wireless applications, reconfigurable and dependable computing systems. Prof. Berekovic is a member of the IEEE and ACM, and served as a reviewer for several IEEE conferences and journal publications including DAC, IEEE Trans. CSVT, ETRI Journal and the Kluwer Journal of VLSI Signal Processing Systems. He is member of the Editorial Board of Elsevier's Journal on Microprocessors and Microsystems, and in the program committees of FPL, RAW, ARC, ARCS, SAMOS, Estimedia and VLSi-SOC.

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