



# Microring resonator-based all-optical parallel pseudo random binary sequence generator for rate multiplication

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## Abstract

In this paper, we design an all-optical Pseudo Random Binary Sequence (PRBS) generator in parallel configuration for operating rate multiplication purposes. The sequential circuit comprises of several clocked D flip-flops, XOR gates and multiplexers implemented using microring resonator (MRR)-based switches. The proposed design is demonstrated and validated through simulations for 500 Gb/s and 400 Gb/s rate doubling and quadrupling, respectively, of a 5-bit degree PRBS. The MRR critical operating parameters are also optimized against performance metrics through numerical investigation.

**Keywords** Microring resonator · Optical D flip-flop · Optical XOR gate · Optical multiplexer · Pseudo random binary sequence · Rate multiplication

## 1 Introduction

In recent years, the rapid convergence of interdisciplinary technologies, such as optical and RF, together with the intensive demand for broadband services fuelled by the emergence of applications such as cloud computing, online gaming, social media, etc., or trends such as distance working, training, etc., forced by factors like the COVID-19 pandemic, has made more imperative than ever the need for providing information that can be readily scaled to higher data speeds. In modern communication networks and systems, such information is carried in structured form by Pseudo Random Binary Sequences (PRBS), which are deterministic in nature, include all possible combinations of data up to a given length, have useful statistical properties, and can be generated in a straightforward and reproducible manner (MacWilliams and Sloane 1976). PRBS are also used in the optical domain, where different approaches have been adopted to generate them exclusively by means of light (Zoiros et al. 2011; Ma et al. 2009; Wu et al. 2010; Rakshit et al. 2021; Thapa et al. 2019; Kouloumentas et al. 2009), i.e. all-optically (AO), and employ them in applications with

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better performance and higher operating speed than the corresponding electronic, such as bit error rate testing (Zoiros et al. 2004), binary pattern recognition (Webb et al. 2009), error detection/correction (Aikawa et al. 2011), parity generation and checking (Dimitriadou et al. 2013), encryption/decryption (Zhang et al. 2015) and optical code division multiple access (CDMA) (Glesk et al. 2017).

In order to efficiently cope with single channel data rates dramatic increase mandated by the need to manage the growing traffic demand, it is necessary to enhance the speed of PRBS generators (Zhu and Saxena 2018). Recently (Hossain et al. 2021a), we showed how the rate of a PRBS can be doubled to 500 Gb/s without increasing the synchronization frequency of the PRBS generator. For this purpose, microring resonator (MRR)-based clocked D flip-flops, exclusive-or (XOR) logic gates and a 2:1 multiplexer were used, thus benefiting from the MRR attractive properties of compact size, high-Q, ultrafast and controllable nonlinearity, ultra low power consumption and compatibility with microelectronic fabrication methods and material systems (Rakshit and Roy 2014, 2017). The core AO circuit employed the series PRBS configuration, which is a linear feedback shift register (LFSR) that produces an  $r$ -bit degree PRBS of maximum length  $p=2^r-1$ , provided that certain memory units, or flip-flops, of total number  $r$ , are tapped and their contents are modulo-2 added in an XOR gate so that the output of the latter is fed back as the new input to the register (Golomb 1967). In general, for increasing the original bit rate of the PRBS by  $q$  times,  $q$  original sequences spaced apart by  $(p-1)/q$  bits in phase are required (Sinesbichler et al. 1996). These delayed replicas of the initial PRBS can be obtained through modulo-2 addition of existing sequences from the LFSR based on PRBS shift-and-add property (MacWilliams and Sloane 1976). Although the connections and combinations of the additional XORs can be found by means of devised algorithms (Latawiec 1974; Miller et al. 1977; Luyn 1978), still the number of the XOR gates required to implement the phase shifts grows exponentially with  $q$ , which hence cancels the benefit of generating the reference PRBS at a lower speed.

Unlike the conventional series PRBS generator, a more hardware- and cost-effective PRBS rate multiplication scheme is that of a parallel PRBS generator, which can produce at the output of each  $r$ -th flip-flop  $q \leq r$  shifted sequences simultaneously (Laskin and Voiginescu 2006). Thus the necessary and appropriately phase-shifted sequences are available from the generator itself and can be multiplexed to higher bit rates directly, without the need for extra phase shifting circuitry, as in the case of series PRBS generator. The parallel PRBS generator can be designed by constructing a transition matrix of order  $q$  and translating its binary contents into the PRBS circuit with parallel outputs, as described in O'Reilly (1975). In this paper, for the first time to our knowledge, we design this modified PRBS architecture and apply the associated method to AO PRBS speed enhancement using MRR-based clocked D flip-flops and XOR logic gates, as well as a 2:1 multiplexer and a 4:1 multiplexer to double and quadruple, respectively, the repetition rate of a 5-bit degree PRBS.

This paper is organized as follows: Sect. 1 puts the conducted work in the proper context by referring to the prior art in the field of AO PRBS generation and rate acceleration. It also explains the motivation for PRBS speed enhancement based on the parallel PRBS generator architecture. Section 2 describes the PRBS rate enhancement principle in parallel configuration. Section 3 describes the fundamental structure and operation of the MRR-based all-optical switch. Section 4 describes the working principle of the MRR-based clocked D flip-flop, XOR gate, multiplexer and how these modules are assembled to set up a parallel PRBS generator for speed doubling and quadrupling. It also considers some practical implementation issues. Section 5 considers and investigates the effect of MRR critical

parameters on the performance of the parallel PRBS generator. Section 6 presents the simulation results for the outcomes of the parallel PRBS generator. Finally, Sect. 7 includes the conclusion.

## 2 Principle of PRBS speed enhancement in parallel configuration

PRBS speed can be enhanced, i.e. doubled, tripled, quadrupled, etc., without changing the synchronization frequency of the LFSR (Murashko 2007), by multiplexing suitable number of properly shifted PRBS replicas at the original bit rate (Laskin 2006). This mechanism has been thoroughly established in Hossain et al. 2021a for doubling the PRBS speed at a rate of 500 Gb/s in series PRBS configuration. In this case, however, the output sequence bits are generated sequentially and hence are not amenable to multiplexing, unless using extra phase-shifting circuitry. In the parallel PRBS generator, in contrast, a number of properly shifted PRBS can be generated in parallel and be directly multiplexed to enhance the PRBS speed (Laskin 2006).

A parallel PRBS generator of  $k$  parallel outputs can be constructed from a series PRBS generator of  $r$  memory elements (O’Reilly 1975). The mathematical tool exploited for this purpose is the so-called ‘transition’ (or sometimes ‘companion’)—‘ $T$ ’ matrix. This is an  $r \times r$  matrix that corresponds to the LFSR physical realization, as it describes how data is transferred between the memory elements of the LFSR that implements the PRBS by linking the next to the current LFSR state according to the relationship

$$D(i + 1) = T \cdot D(i) \tag{1}$$

where  $D$  is a  $r \times 1$  vector of 1’s and 0’s that represents the state of the  $r$ -stage PRBS at the  $i$ -th clock cycle. In a  $T$  matrix, assuming that the LFSR stages are numbered in the same direction as that of data shifting, the column number represents the corresponding stage of the generator, while the row number indicates the connection between stages. The column number containing a 1 indicates the corresponding stage to be connected to the input of the stage represented by the row number containing 1, when there is only one 1 in a row. If there is more than one 1 in a row, the outputs of the stages corresponding to column number containing 1 are added (modulo-2) and connected to the stage represented by the row number containing 1’s. All other entries of the matrix are 0. The  $T$  matrix whose content is formed according to the aforementioned guidelines is related in a straightforward manner to the PRBS characteristic polynomial (O’Reilly 1975; Laskin 2006), which is the reciprocal of the primitive feedback polynomial of order  $r$  used to generate the PRBS of maximum possible length  $p$  (Dimitriadou et al. 2013), or  $m$ -sequence. For example, for the 5-th order feedback polynomial  $\varphi(x) = x^5 \oplus x^3 \oplus 1$ , or equivalently for the characteristic polynomial  $\psi(x) = x^4\varphi(1/x) = x^5 \oplus x^2 \oplus 1$ , the  $T$  matrix is written as

$$T = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{2}$$

and satisfies (Murashko 2007)  $\psi(x) = \det(T \oplus I \cdot x)$ , where  $\det(\cdot)$  stands for the matrix determinant and  $I$  is a unitary diagonal matrix of rank  $r$ , so that (Sarwate and Pursley 1980)  $T^p = I$ , or equivalently  $T^p D = D$ . The first row of this matrix contains 1’s, which

define the feedback taps combined modulo-2 to form the new input to the LFSR, while all other rows contain only a single 1 and occur in the sub-diagonal below the main diagonal.

The corresponding PRBS block diagram with 5 D flip-flops, DFF-1, DFF-2, DFF-3, DFF-4, DFF-5 and a single output is presented in Fig. 1 (Laskin 2006).

The generated bits are described by the following formulas:

$$D1(i + 1) = D3(i) \oplus D5(i), D2(i + 1) = D1(i), D3(i + 1) = D2(i), D4(i + 1) = D3(i), D5(i + 1) = D4(i)$$

The disadvantage of this realization is that only one new bit is produced per clock cycle. In order to be able to obtain multiple new bits, (1) is modified by inserting the desired cycles number,  $q$ , in the power of matrix  $T$ :

$$D(i + q) = T^q \cdot D(i) \tag{3}$$

For  $q=2$  and  $q=4$ , or equivalently for 2- and 4-parallel outputs, the transitions matrices  $T^2$  and  $T^4$  are given by Eq. 4 and Eq. 5, respectively:

$$T^2 = \begin{bmatrix} 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{4}$$

$$T^4 = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5}$$

From these matrices, it can be noted that the 2nd row of  $T^2$  and the 4th row of  $T^4$  is the same as the 1st row of  $T$ , that a diagonal array of three (3) 1's appears displaced 2 rows below the main diagonal of  $T^2$ , or equivalently from the 3rd row of this matrix and downwards, which is simplified to '10000' in the 5th row of  $T^4$ , and that the 1st row of  $T^2$  as well as the 1st, 2nd and 3rd rows of  $T^4$  are the same as the 1st row of  $T$  but shifted left by 1 or 3, 2 and 1 column positions, respectively, with 0's shifted in from the right-hand side, provided 1's are not shifted from the left-hand side of each matrix (O'Reilly 1975).

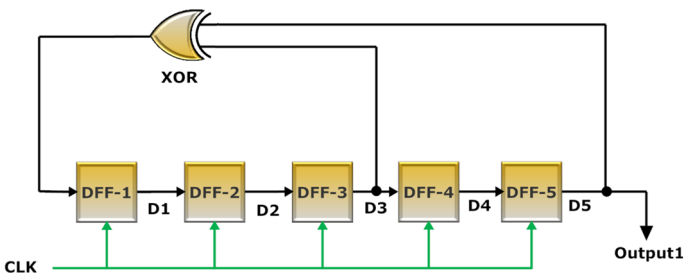
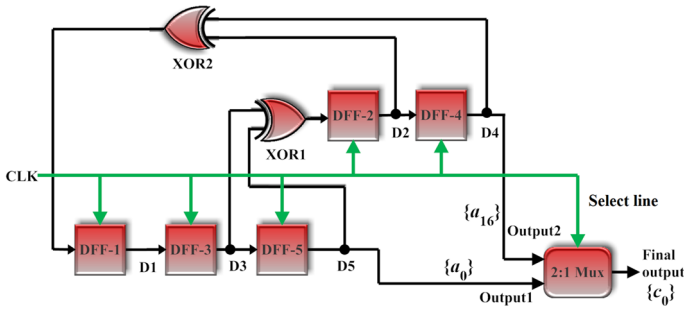
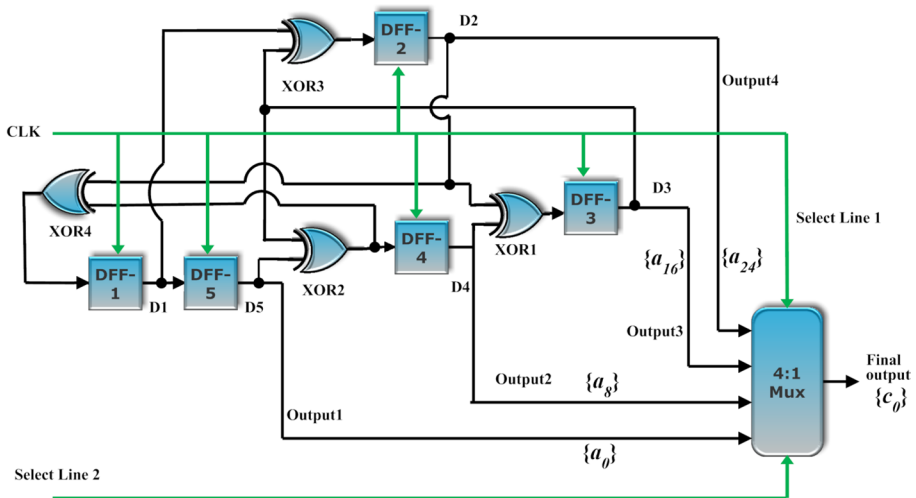


Fig. 1 5-stage PRBS with single output



**Fig. 2** Realization of 5-stage parallel PRBS generator with 2-outputs and feedback polynomial  $\varphi(x) = 1 \oplus x^3 \oplus x^5$



**Fig. 3** Realization of 5-stage parallel PRBS generator with 4-outputs and feedback polynomial  $\varphi(x) = 1 \oplus x^3 \oplus x^5$

After constructing matrices  $T^2$  and  $T^4$  as described above, they can then be converted into a sequential circuit form and a parallel PRBS generator of  $q$  ( $=2$  or  $4$ ) outputs based on the fact that rows 1 to  $q$  ( $=2$  or  $4$ ) define the excitation of the  $q$ -th (2nd or 4th) storage element or flip-flop (O'Reilly 1975). Thus Eq. 4 describes the generation of two new bits and Eq. 5 of four new bits per one clock cycle, according to the following set of logical equations, respectively

$$D1(i + 1) = D2(i) \oplus D4(i), D2(i + 1) = D3(i) \oplus D5(i), D3(i + 1) = D1(i), D4(i + 1) = D2(i), D5(i + 1) = D3(i),$$

$$D1(i + 1) = D2(i) \oplus D3(i) \oplus D5(i), D2(i + 1) = D1(i) \oplus D3(i), D3(i + 1) = D2(i) \oplus D4(i), D4(i + 1) = D3(i) \oplus D5(i), D5(i + 1) = D1(i),$$

which can be then realized with the block diagrams shown in Figs. 2 and 3, respectively.

These setups can be exploited for PRBS acceleration by a factor of 2 or 4, respectively. For this purpose, it is necessary to specify (a) which 2 or 4 phase-shifted  $m$ -sequences must be multiplexed, and (b) how these delayed replicas can be produced using the configurations of Figs. 2 and 3, respectively. To address a), we follow the guidelines for designing a PRBS generator that creates several characters of an  $m$ -sequence in a single synchronization cycle (Murashko 2007). More specifically, for PRBS rate doubling we must interleave sequences  $\{a_0\}$  and  $\{a_{16}\}$ , while for PRBS rate quadrupling we must serialize sequences  $\{a_0\}$ ,  $\{a_8\}$ ,  $\{a_{16}\}$  and  $\{a_{24}\}$ . Of these sequences,  $\{a_0\}$  is the reference PRBS taken in each case from the output of the last (right-most) flip-flop, DFF-5.  $\{a_0\}$ , which begins with the 0-th character and repeats itself every 31 bits, i.e.  $\{a_0\} = a_0, a_1, a_2, \dots, a_{30}, a_0, a_1, \dots$ , satisfies  $a_i = a_{2i}$ , i.e. the digit in the  $2i$ -th position is the same as the one in the  $i$ -th position, and it is termed as ‘characteristic’. This property is critical in order to obtain at the end of the rate multiplication process the same but faster initial  $m$ -sequence. The subsequent sequences,  $\{a_{16}\}$  and  $\{a_8\}$ , are deduced according to  $2x = 1 \pmod{31}$  and  $4x = 1 \pmod{31}$ , which results in  $x = 16$  and  $x = 8$ , respectively. These indices denote that  $\{a_{16}\}$  and  $\{a_8\}$  are produced by selecting, i.e. sampling or decimating, every 16th and 8th bit of  $\{a_0\}$ , or powers of 2 which are mutually prime relative to the PRBS period, and hence also are  $m$ -sequences. The remaining sequences required for four-fold rate increase are formed by the successive sampling of 2 and 3 copies of  $\{a_0\}$  shifted by 8 cycles, and so their phase shifts are  $2 \cdot 8 \pmod{31} = 16$  and  $3 \cdot 8 \pmod{31} = 24$ , or  $\{a_{16}\}$  and  $\{a_{24}\}$ , respectively (Murashko 2007). To tackle b), we take the outputs of flip-flops DFF-4 and DFF-5 in Fig. 2 and DFF-2 to DFF-5 in Fig. 3 (O’Reilly 1975). Thus in Fig. 2,  $\{a_0\}$  is available at the output of DFF-5, i.e. D5, while  $\{a_{16}\}$  is available at the output of DFF-4, i.e. D4, and is shifted by one-half the bit period of  $\{a_0\}$  (Murashko 2007). If sequences  $\{a_0\}$  and  $\{a_{16}\}$  are then applied to the input of a 2:1 multiplexer, an  $m$ -sequence  $\{c_0\}$  with double frequency than the original one will be generated, as 2 characters are available at the multiplexer output in the course of a single operating cycle. In Fig. 3,  $\{a_0\}$  is available at the output of DFF-5,  $\{a_8\}$  is available at the output of DFF-4,  $\{a_{16}\}$  is available at the output of DFF-3 and  $\{a_{24}\}$  is available at the output of DFF-2, while each sequence is shifted relative to each other by one-quarter of the bit period of  $\{a_0\}$ . If sequences  $\{a_0\}$ ,  $\{a_8\}$ ,  $\{a_{16}\}$  and  $\{a_{24}\}$  are applied to the input of a 4:1 multiplexer, an  $m$ -sequence  $\{c_0\}$  with quadruple frequency than the original one will be generated as 4 characters are available at the multiplexer output in the course of a clock pulse period. In each case, the faster sequence,  $\{c_0\}$ , which is obtained after multiplexing, will be exactly the same as the prototype one,  $\{a_0\}$ , given that the latter is ‘characteristic’ while its period and the acceleration factor, 2 or 4, are mutually prime (Murashko 2007).

The generation of  $\{a_0\}$  and  $\{a_{16}\}$  sequences required for doubling the PRBS speed is shown LFSR state-by-state step in Table 1, while that of  $\{a_0\}$ ,  $\{a_8\}$ ,  $\{a_{16}\}$  and  $\{a_{24}\}$  sequences for quadrupling the PRBS speed in Table 2. In both cases the same initial condition ‘01001’ has been used to ensure that  $\{a_0\}$  is ‘characteristic’ (Willett 1976).

### 3 Working principle of microring resonator-based optical switch

A MRR that works as an optical switch is constructed with a circle-shaped waveguide, two input–output bus waveguides and two input–output couplers. The basic MRR configuration comprises of four ports, as depicted in Fig. 4 (Rakshit and Roy 2016a; Laleh and Razaghi 2020). When an optical signal enters the MRR and spectrally coincides with its resonant

**Table 1** Figure 2 Parallel PRBS generator 5-stages connection and state succession to produce half-period phase-shifted *m*-sequences  $\{a_0\}$  and  $\{a_{16}\}$  that are multiplexed into  $\{c_0\}$  of same binary content but two times as fast as  $\{a_0\}$

Clock instant <i>i</i>	D1 = (D2 ⊕ D4)	D2 = (D3 ⊕ D5)	D <sub>3</sub> =(D <sub>1</sub> )	D <sub>4</sub> =(D <sub>2</sub> ) { <i>a</i> <sub>16</sub> }	D <sub>5</sub> =(D <sub>3</sub> ) { <i>a</i> <sub>0</sub> }
0 (Initial Condition)	0	1	0	0	1
1	1	1	0	1	0
2	0	0	1	1	0
3	1	1	0	0	1
4	1	1	1	1	0
5	0	1	1	1	1
6	0	0	0	1	1
7	1	1	0	0	0
8	1	0	1	1	0
9	1	1	1	0	1
10	1	0	1	1	1
11	1	0	1	0	1
12	0	0	1	0	1
13	0	0	0	0	1
14	0	1	0	0	0
15	1	0	0	1	0
16	1	0	1	0	0
17	0	1	1	0	1
18	1	0	0	1	1
19	1	1	1	0	0
20	1	1	1	1	1
21	0	0	1	1	1
22	1	0	0	0	1
23	0	1	1	0	0
24	1	1	0	1	1
25	0	1	1	1	0
26	0	1	0	1	1
27	0	1	0	1	0
28	0	0	0	1	0
29	1	0	0	0	0
30	0	0	1	0	0
31 (Repeat)	0	1	0	0	1

wavelength,  $\lambda_{res}$ , the optical intensity accumulates and is enhanced over several round trips. The condition for resonance can be controlled and satisfied by applying a suitable optical pump beam to the ring. The optical pump beam changes the refractive index of the MRR non-linear material due to two-photon absorption (TPA), according to  $n_{eff} = n_0 + n_2 \cdot I = n_0 + n_2 \cdot \frac{P}{A_{eff}}$ , where  $n_0$  and  $n_2$  are the linear and nonlinear refractive indices, respectively,  $I$  is the intensity and  $P$  is the power of the injected optical pump beam, and  $A_{eff}$  is the MRR

**Table 2** Parallel PRBS generator 5-stages connection and state succession to produce quarter-period phase-shifted *m*-sequences  $\{a_0\}$ ,  $\{a_8\}$ ,  $\{a_{16}\}$  and  $\{a_{24}\}$  that are multiplexed into  $\{c_0\}$  of same binary content but four times as fast as  $\{a_0\}$

Clock instant <i>i</i>	D1 = (D2 ⊕ D3 ⊕ D5)	D2 = (D1 ⊕ D3) { <i>a</i> <sub>24</sub> }	D3 = (D2 ⊕ D4) { <i>a</i> <sub>16</sub> }	D4 = (D3 ⊕ D5) { <i>a</i> <sub>8</sub> }	D5 = (D1) { <i>a</i> <sub>0</sub> }
0 (Initial Condition)	0	1	0	0	1
1	0	0	1	1	0
2	1	1	1	1	0
3	0	0	0	1	1
4	1	0	1	1	0
5	1	0	1	1	1
6	0	0	1	0	1
7	0	1	0	0	0
8	1	0	1	0	0
9	1	0	0	1	1
10	1	1	1	1	1
11	1	0	0	0	1
12	1	1	0	1	1
13	0	1	0	1	1
14	0	0	0	1	0
15	0	0	1	0	0
16	1	1	0	1	0
17	1	1	0	0	1
18	0	1	1	1	1
19	1	1	0	0	0
20	1	1	1	0	1
21	1	0	1	0	1
22	0	0	0	0	1
23	1	0	0	1	0
24	0	1	1	0	1
25	1	1	1	0	0
26	0	0	1	1	1
27	0	1	1	0	0
28	0	1	1	1	0
29	0	1	0	1	0
30	1	0	0	0	0
31 (Repeat)	0	1	0	0	1

effective cross-sectional area. The refractive index change induces a phase shift, which if made equal to  $\pi$  makes through constructive interference the input signal available at the MRR through port, while the drop port will get nothing. In contrast, when no optical pump signal is applied, the input signal becomes available at the MRR drop port and the through port gets nothing. The through port and the drop port output electric fields can be expressed, respectively, as (Rakshit and Roy 2014):



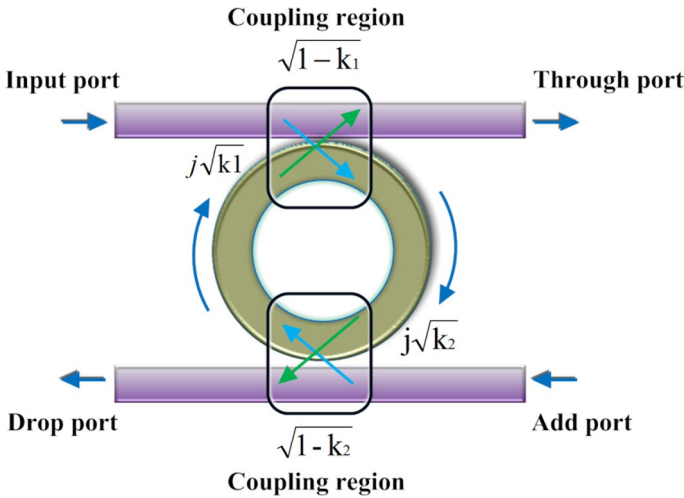


Fig. 4 MRR basic configuration

$$E_t = \frac{D\sqrt{1-k_1} - D\sqrt{1-k_2}x^2 \exp^2(j\varphi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\varphi)} E_{i1} + \frac{-D\sqrt{k_1}\sqrt{k_2}x \exp(j\varphi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\varphi)} E_{i2} \quad (6)$$

$$E_d = \frac{-D\sqrt{k_1}\sqrt{k_2}x \exp(j\varphi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\varphi)} E_{i1} + \frac{D\sqrt{1-k_2} - D\sqrt{1-k_1}x^2 \exp^2(j\varphi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\varphi)} E_{i2} \quad (7)$$

where  $D = (1 - \gamma)^{1/2}$ ,  $x = D \cdot \exp\left(-\frac{\alpha L}{4}\right)$ ,  $\varphi = \frac{k_n L}{2}$ . The parameters involved in these formulas are the coupling coefficient of the input and output couplers,  $k_1$  and  $k_2$ , respectively; the wave propagation constant,  $k_n = \frac{2\pi}{\lambda} \cdot n_{eff}$ ; the MRR resonant wavelength,  $\lambda_{res}$ ; the intensity attenuation coefficient of the ring,  $\alpha$ ; the intensity insertion loss coefficient of the directional couplers,  $\gamma$ ; and the length of the ring,  $L$ ; while  $E_{i1}$  and  $E_{i2}$  are the input and add port fields, respectively.

When an optical pump beam is applied to the MRR, the relation between the phase shift,  $\varphi$ , induced by the refractive index change,  $\Delta n$ , is described by the following equations (Rakshit and Roy 2017):

$$\varphi = \frac{2\pi}{\lambda} \Delta n L \quad (8)$$

$$\Delta n = - \left[ 8.8 \times 10^{-22} \frac{\beta t_p^2}{2h\nu\sqrt{\pi}\tau S^2} P_{avg}^2 + 8.5 \times 10^{-22} \left( \frac{\beta t_p^2}{2h\nu\sqrt{\pi}\tau S^2} P_{avg}^2 \right)^{0.8} \right] \quad (9)$$

where  $h\nu$  is the photon energy,  $\beta$  is the TPA coefficient and  $P_{avg}$  is the average power of the optical pump signal with pulse repetition interval  $t_p$  and pulse width (full-width at half-maximum)  $\tau$ . By replacing (9) in (8), the phase shift variation against the average pump

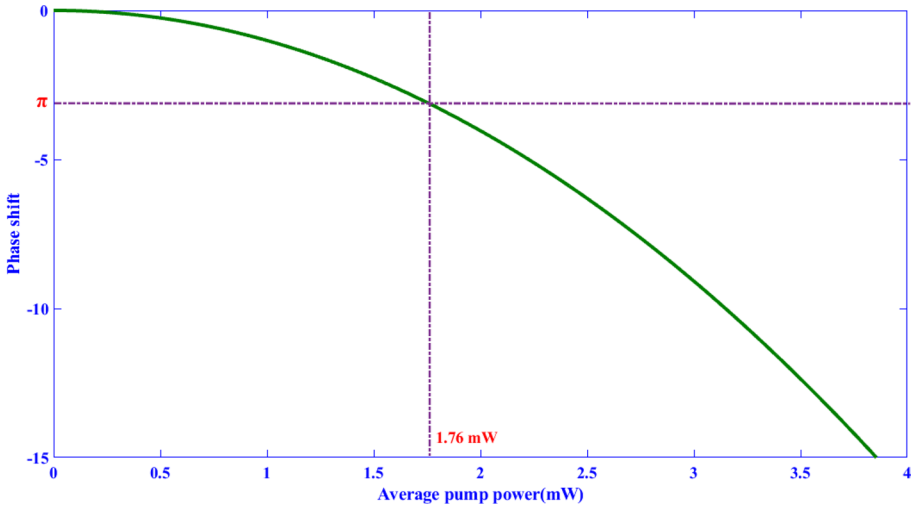


Fig. 5 Induced phase shift against average pump power

power is plotted in Fig. 5. From this figure, it can be seen that an average switching pump power of 1.76 mW is required to induce a phase shift of  $\pi$ .

#### 4 Proposed design of all-optical parallel PRBS generator for PRBS speed enhancement

The proposed design of the parallel PRBS generator for speed enhancement requires using AO clocked D flip-flops, 2-input XOR gates and 2:1 multiplexer or 4:1 multiplexer. These necessary constituents are implemented by exploiting the MRR-based technology as follows.

##### A. MRR-based clocked D flip-flop

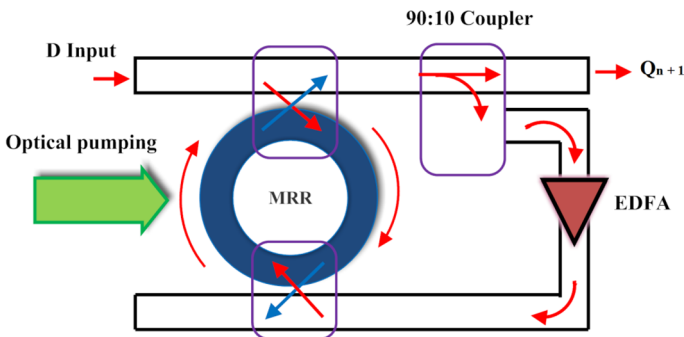
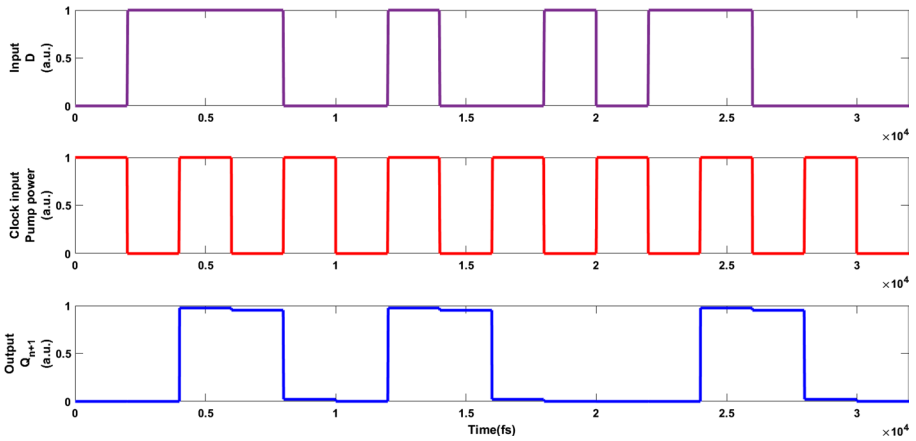


Fig. 6 Implementation of MRR-based clocked D flip-flop

**Table 3** Truth table of clocked D flip-flop

D input	CLK	$Q_n$	$Q_{n+1}$	Remarks
0	0	0	0	Unchanged
0	0	1	1	Unchanged
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	0	Unchanged
1	0	1	1	Unchanged
1	1	0	1	Set
1	1	1	1	Set



**Fig. 7** Simulation results of MRR-based clocked D flip-flop

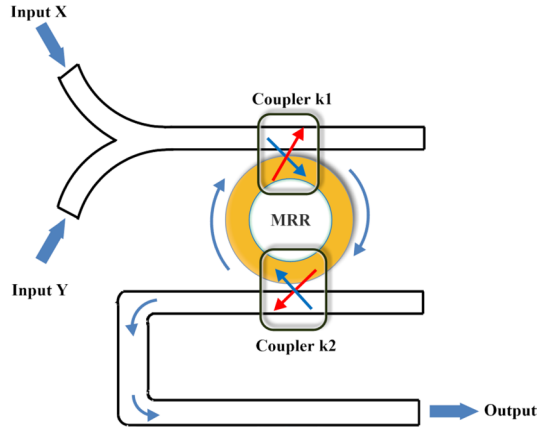
Microring resonator-based clocked D flip-flop is an essential unit of AO parallel PRBS generator employed for speed enhancement. Figure 6 shows the construction of the clocked D flip-flop in the optical domain using MRR. The output ( $Q_{n+1}$ ) of the clocked D flip-flop equals the MRR input D when the clock signal (CLK) is HIGH (logic 1), else  $Q_{n+1}$  holds the information of the previous state,  $Q_n$ . The possible clocked D flip-flop outputs are displayed in Table 3. A feedback path is formed through a 90:10 coupler from the MRR add port to maintain the previous output of the flip-flop when no clock signal is applied. An Erbium Doped Fiber Amplifier (EDFA) is used in this path to provide the necessary extra gain (Rakshit et al. 2021).

The operation of the AO clocked D flip-flop is simulated using MATLAB software and the outcome, which complies with Table 3, is shown in Fig. 7.

**B. MRR-based XOR gate**

The XOR gate is also an important logic block for designing the parallel PRBS generator. The output of the XOR gate will be LOW (logic 0) if both inputs are LOW or HIGH (logic 1), and will be HIGH if, and only if, one of the inputs is HIGH. Figure 8 shows the XOR gate configuration using single MRR. A Y-shaped coupler is used to provide two inputs to the MRR. The input signals act as pseudo-pump signals to the MRR. If

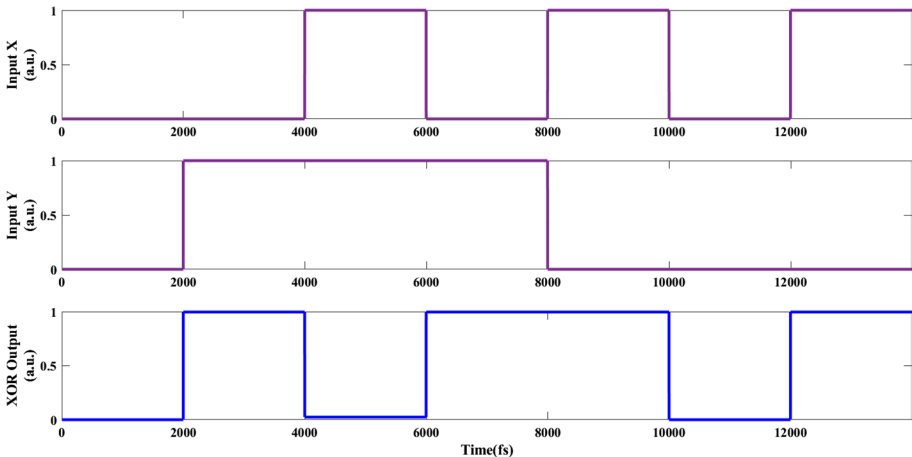
**Fig. 8** Implementation of MRR-based XOR gate



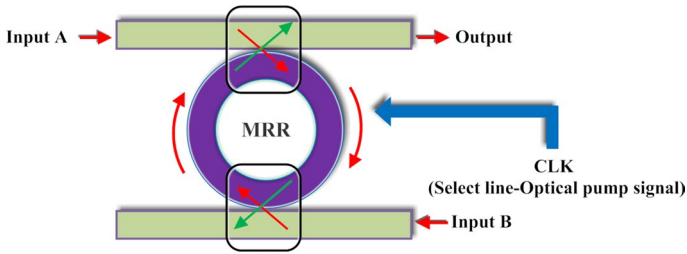
any of the input is HIGH (logic 1), the power corresponding to this input is not adequate to shift the MRR resonance, and as a consequence the MRR drop port will be HIGH. If both inputs are HIGH, the input power is doubled and capable of shifting the MRR resonance, so the MRR drop port will be LOW. Therefore, the 2-input XOR operation that is summarized in Table 4 is obtained from the drop port of the MRR, according to the simulated results shown in Fig. 9.

**Table 4** Truth table of XOR gate

Input X	Input Y	Output at drop port
0	0	0
0	1	1
1	0	1
1	1	0



**Fig. 9** Simulation results of MRR-based XOR gate



**Fig. 10** Implementation of MRR-based 2:1 Multiplexer

**Table 5** Truth table of 2:1 Multiplexer (X = don't care)

Select (control) line	Data inputs		Output
	A	B	
1	D <sub>0</sub>	X	D <sub>0</sub>
0	X	D <sub>1</sub>	D <sub>1</sub>

**C. MRR-based 2:1 multiplexer**

A multiplexer is a combinational logic circuit that accepts multiple data as inputs and allows only one of them at a time to be available at the output (Rakshit and Roy 2014, 2016b). A 2:1 MUX accepts two data inputs and outputs only one at a time depending on the control signal that is termed as ‘Select’- ‘S’ line. In this work, the Select line has two states, i.e. logic ‘1’ or logic ‘0’, which are determined by an ON or OFF pump signal, respectively, applied externally to the MRR. The 2:1 MUX is required to double the PRBS speed in parallel configuration. For this purpose, input A and input B are applied to the MRR input port and add port, respectively, as shown in Fig. 10. The output at the MRR through port is such that input A is transferred therein when the optical pump signal is ON, whereas input B becomes available therein when the optical pump signal is OFF. Thus for a single clock (optical pump signal) pulse, input A is selected for half clock period and input B is selected for the next half clock period at the 2:1 MUX output. This operation is described by the Boolean expression  $Output = SA + \bar{S}B$ , and its truth table is shown in Table 5. Figure 11 depicts the simulation results of the MRR-based 2:1 MUX operation when the repetition rate of the applied optical pump signal is 250 Gb/s.

**D. MRR-based 4:1 multiplexer**

A 4:1 MUX accepts four data inputs and outputs only one at a time depending on the applied control signal. In this work, the two select lines S1 and S2 are two different optical pump signals that are applied externally to MRR and define the logic ‘0’ and ‘1’ states when they are OFF or ON, respectively. The 4:1 MUX is required for quadrupling the PRBS speed in parallel configuration. Inputs A, B, C and D are applied to port 1, port 2, port 3 and port 4 of MRR1, respectively, as shown in Fig. 12 (Rakshit and Roy 2016b). The multiplexed output is obtained at the MRR2 through port. The individual binary combination of S1 and

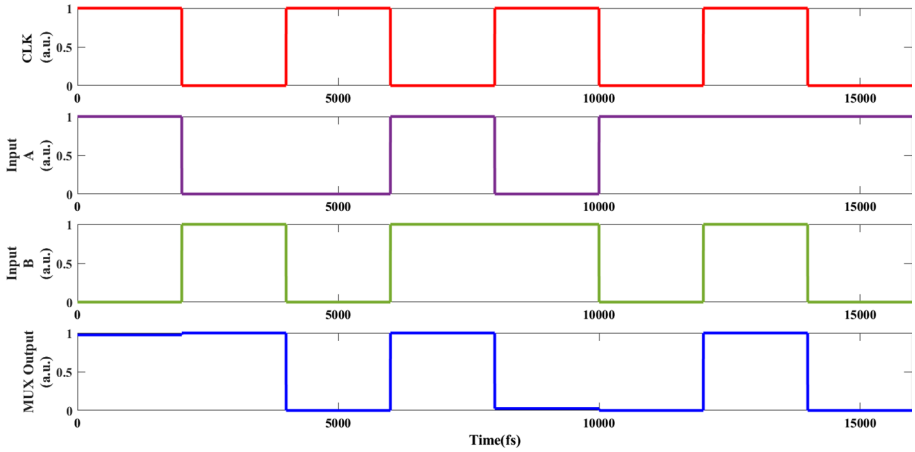


Fig. 11 Simulation results of MRR-based 2:1 Multiplexer

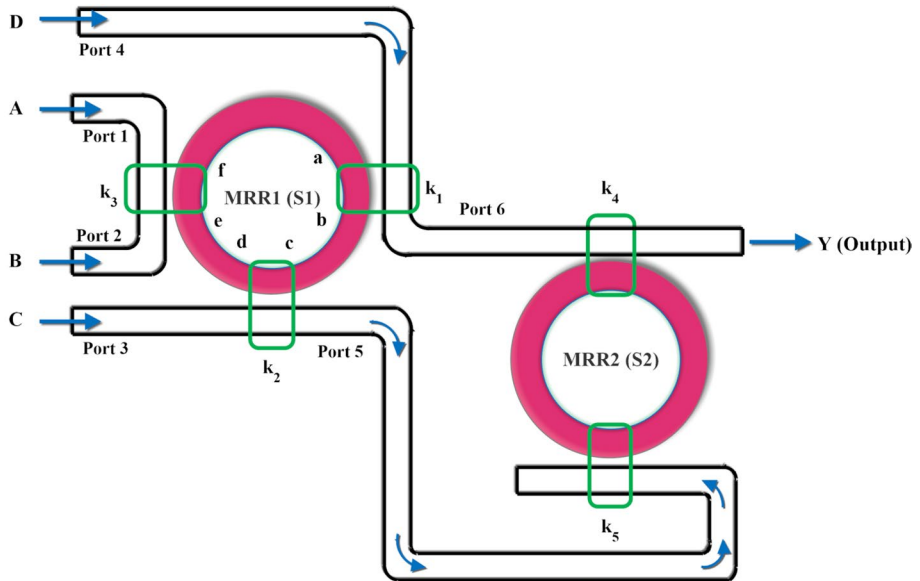
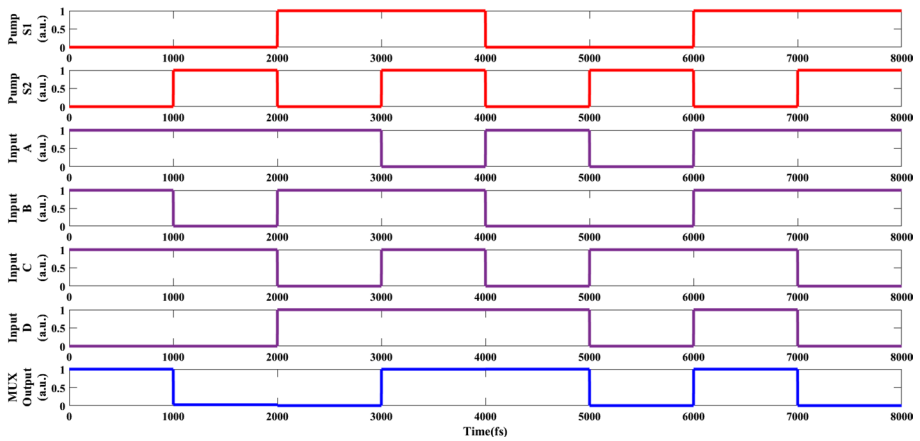


Fig. 12 Implementation of MRR-based 4:1 MUX

S2 selects one of the inputs as the output of the MRR2. The Boolean expression of the 4:1 MUX operation is  $Output = \overline{S1} \cdot \overline{S2} \cdot A + \overline{S1} \cdot S2 \cdot B + S1 \cdot \overline{S2} \cdot C + S1 \cdot S2 \cdot D$ , and the corresponding truth table is given in Table 6. Figure 13 shows the simulation results of the MRR-based 4:1 MUX operation.

**Table 6** Truth table of MRR-based 4:1 MUX (X=don't care)

Select or control lines		Data inputs				Output
S1	S2	A	B	C	D	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

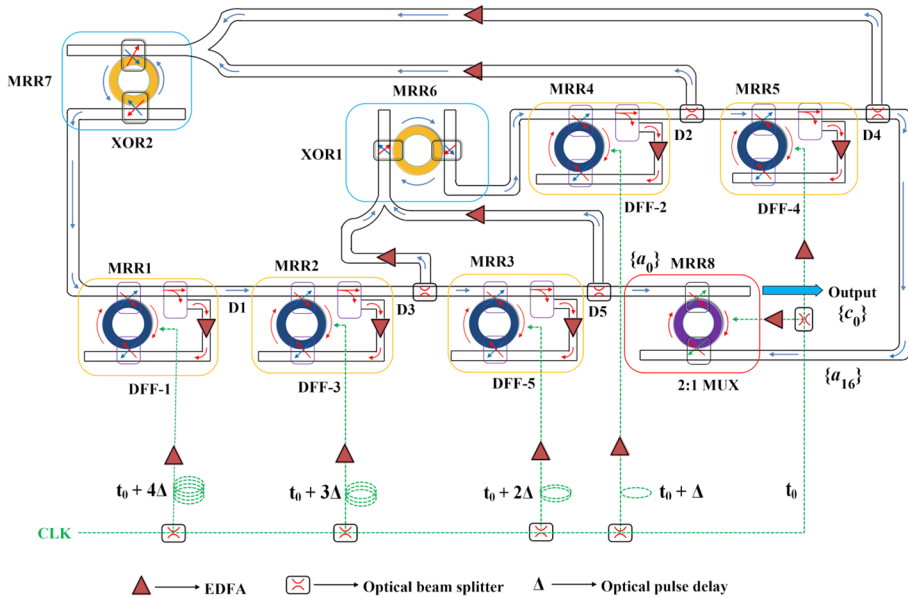


**Fig. 13** Simulation results of MRR-based 4:1 MUX

**E. MRR-based all-optical implementation of parallel PRBS generator for speed doubling**

The designed AO parallel PRBS generator for speed doubling consists of clocked D flip-flops, XOR gates and 2:1 multiplexer implemented with MRR-based switches. Figure 2 shows that a 5-bit degree PRBS generator requires five D flip-flops, two XOR gates and a 2:1 MUX for this purpose. The AO implementation of Fig. 2 is shown in Fig. 14. We get the PRBS with double speed at the 2:1 MUX output. All employed modules exploit MRR-based technology, as described before.

In Fig. 14, MRR1 to MRR5 represent clocked D flip-flops, XOR gates are represented by MRR6 to MRR7 and 2:1 MUX is represented by MRR8. The output of MRR1 (DFF-1) acts as the input to MRR2 (DFF-3). The output of MRR2 is split by an optical beam splitter into two parts, of which one goes to the input of MRR3 (DFF-5) and the other to one input of MRR6 (XOR1). The output of MRR3 is also split into two parts, of which one goes to the input of MRR8 (2:1 MUX) as PRBS  $\{a_0\}$  required for PRBS speed doubling and the other one acts as the second input of MRR6. The output of MRR6 acts as the input



**Fig. 14** MRR-based AO implementation of 5-bit degree parallel PRBS generator for rate doubling

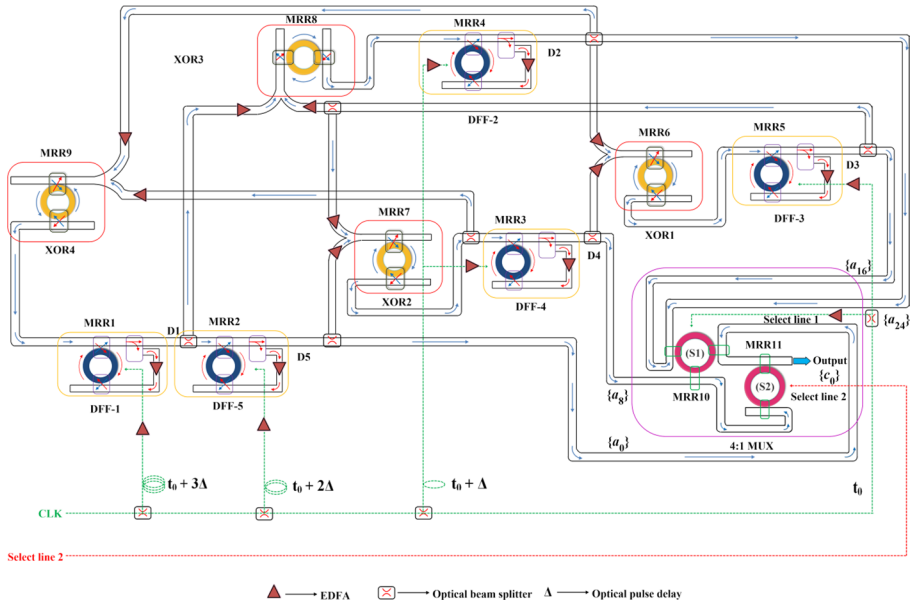
of MRR4 (DFF-2). The MRR4 output acts as the input of MRR5 (DFF-4) as well as the input of MRR7 (XOR2). One part of the MRR5 output goes to the input of MRR7 and the other part goes to the add port of MRR8 as the other PRBS  $\{a_{16}\}$  required for PRBS speed doubling. The output of MRR7 is connected to the input port of MRR1. The doubled speed PRBS,  $\{c_0\}$ , is finally acquired at the output port of MRR8.

The same optical pump signal (CLK) is split into an equal number of instances (Tucker et al. 1988) and applied to all DFFs and MUX. The power of each clock instance is uniformly maintained by exploiting EDFAs on the same material platform (Agazzi et al. 2010). By deploying compact and tunable optical delay lines at each clock instance, synchronization between all DFFs can be achieved. The picosecond timing required for the whole operation can be provided at the desired rate of hundreds of Gb/s (Wang et al. 2001). Since in our design the clock signal is launched from left to right, delay lines indicated by symbol ‘ $\Delta$ ’ must be inserted in inverse order to the DFFs position, i.e.  $4\Delta$ ,  $3\Delta$ ,  $2\Delta$ ,  $\Delta$ , so that all DFFs work simultaneously. An EDFA is inserted at every input of the XOR gates to maintain the power of the signal at sufficient level, as the XOR input acts both as pseudo-pump and probe signal (Rakshit et al. 2021).

#### F. MRR-based all-optical implementation of parallel PRBS generator for speed quadrupling

According to Sect. 2, four outputs from the 5-bit stage parallel PRBS generator are required for speed quadrupling. Figure 3 shows that five D flip-flops, four XOR gates and a 4:1 MUX implemented with MRR-based switches are used for this purpose. The PRBS of quadrupled speed is obtained at the 4:1 MUX output. The AO MRR-based implementation is shown in Fig. 15, which is equivalent to Fig. 3.





**Fig. 15** MRR-based all-optical implementation of 5-bit degree parallel PRBS generator for rate quadrupling

MRR1 to MRR5 represent the 5 clocked D flip-flops, XOR gates are represented by MRR6 to MRR9 and 4:1 MUX is composed of MRR10 and MRR11. The working principle of this design is similar to that described above for PRBS speed doubling. The required four phase-shifted PRBS replicas, i.e.  $\{a_0\}$ ,  $\{a_8\}$ ,  $\{a_{16}\}$  and  $\{a_{24}\}$ , are obtained from the output of DFF-5, DFF-4, DFF-3 and DFF-2, respectively. These outputs are connected to the corresponding inputs of the 4:1 MUX to generate at its exit the PRBS of quadrupled speed,  $\{c_0\}$ . For this purpose, the optical pump signal (CLK) applied to MRR10 plays the role of select line S1, while the clock signal of doubled frequency acts as select line S2.

### G. Practical implementation issues

In this subsection, we discuss some practical implementation issues concerning the MRR count required for higher PRBS rate multiplication factors, including the case of higher order reference PRBS, the limit in the multiplication, and the compatibility of the proposed method with current optical integration techniques.

Specifically, for a given PRBS order,  $r$ , or length,  $2^r - 1$ , the MRR count is determined by the number of XOR gates required to multiply the PRBS original rate by  $q$  times. As deduced from reference [Laskin and Voiginescu 2006, cf. Table I], this number of XOR gates equals  $q$ , provided that  $q \leq r$ . This condition is verified from Figs. 2 and 3, where 2 and 4 XOR gates are employed to double and quadruple the speed of the reference 5-th order PRBS, respectively. Also it can be checked that this rule-of-thumb applies for other multiplication factors, such as 3 and 5 [O'Reilly 1975, cf. Figures 3c, e, respectively]. Since the XOR gate is implemented using one MRR switch (Fig. 8), this means that the MRR count scales with the multiplication factor. This holds up to  $q=r+1$  [Laskin and Voiginescu 2006, cf. Table I], while as  $q$  is increased beyond  $r$ , the required number of XOR gates is dramatically increased. For instance, in order to multiply the rate of a PRBS

of length  $2^7-1$  by 16 times, which denotes that  $16 > 7$ , 23 XOR gates are required (Chen and Yang 2012).

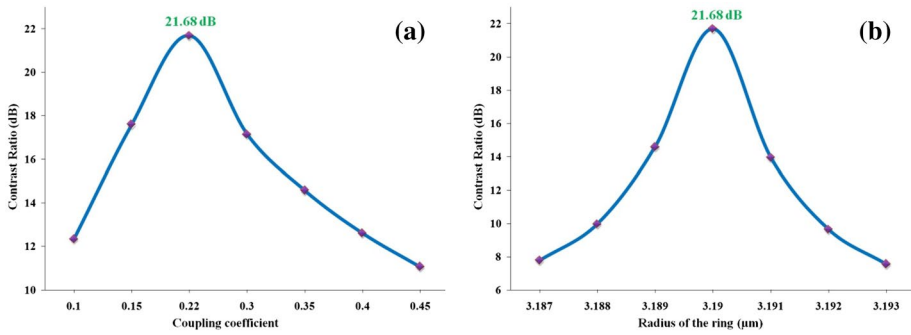
Regarding the limit in multiplication, we note that for the PRBS longest standardized length,  $2^{31}-1$ , the maximum possible multiplication factor is 16. This value is specified so that not only it satisfies the necessary condition described in the previous paragraph, i.e.  $16 < 31$ , but it also ensures that by being a power of 2 it is mutually prime to the period of the reference PRBS, i.e.  $\gcd(p, q) = 1$ , where  $\gcd()$  stands for the greatest common divisor (Murashko 2007). The latter condition is necessary so that the new PRBS obtained through the process of rate multiplication using the parallel architecture will not only exhibit increased speed but it will also be exactly the same as the original PRBS, as a consequence of the PRBS decimation property. This is the case for the considered 2- and 4-rate multiplication of the 5-th order PRBS, while 3- and 5-rate multiplication would also be possible (since  $\gcd(31, 3) = 1$  and  $\gcd(31, 5) = 1$ ) but the produced PRBS would be different than the prototype one (Laskin 2006). Now 16 MRRs for the equal number of required XOR gates plus 31 MRRs for the equal number of required D flip-flops results in a total amount of MRRs that could allow for the whole PRBS circuit to operate satisfactorily. The PRBS speed enhancement method that relies on the suitable exploitation of the parallel architecture requires the same MRR count for a given multiplication factor irrespectively of the reference PRBS order. This can be checked and confirmed by comparing the number of XOR gates required for 2-, 4-, 8- and 16-fold rate increase, which is the same, i.e. 2, 4, 8 and 16, respectively, regardless of the PRBS length, i.e.  $2^7-1$ ,  $2^{15}-1$ , and  $2^{31}-1$  [Laskin and Voiginescu 2006, cf. Table I].

Based on the MRR count estimation given above, it can be stated that both PRBS higher multiplication factors and higher order reference PRBS in MRR-based implementations are feasible from an MRR integration perspective. In fact, owing to MRRs very compact size and small footprint, it has been possible to build and demonstrate switch fabrics of enhanced logic functionality comprising of many MRRs (Xu and Soref 2011). To this aim, MRRs are compatible with microelectronic nanofabrication methods and material systems, especially the mature Complementary Metal–Oxide–Semiconductor (CMOS) and established silicon photonics, respectively (Li et al. 2015). Thus this similarly suggests that it would be possible to exploit this available technology and interconnect integrated MRR-based D flip-flops, XOR gates and MUX to form all-optical complex sequential circuits, such as the PRBS generator in parallel configuration.

## 5 Performance metrics

The quality of the generated optical signals can be assessed by means of metrics, such as the Contrast Ratio (CR), the Extinction Ratio (ER), the Amplitude modulation (AM) (Zoiros et al. 2006; Hossain et al. 2021b) and the On–Off Ratio (OOR) (Hossain et al. 2021b). The performance of the designed AO parallel PRBS generator in terms of these metrics critically depends on the MRR coupling coefficient and radius. For acceptable performance of the parallel PRBS generator for rate doubling and quadrupling, the CR and ER must be as high as possible and at least 10 dB. In this manner, the maximum portion of the input signal will be available at the output. Conversely, AM should be as low as possible for uniform output. On the other hand, the value of OOR is  $> 20$  dB for high performance.

The CR is defined as:



**Fig. 16** CR versus **a** MRR coupling coefficient, **b** MRR radius

$$CR \text{ (dB)} = 10\log\left(\frac{P^1_{mean}}{P^0_{mean}}\right) \tag{10}$$

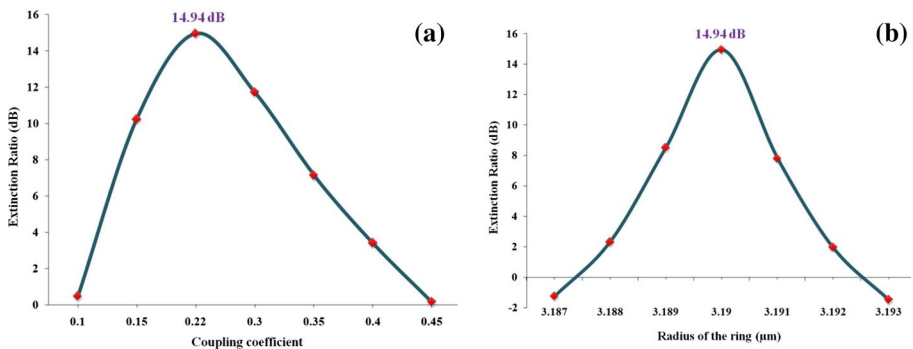
where  $(P^1_{mean})$  and  $(P^0_{mean})$  is the mean value of output intensity for high level and low level, respectively. The CR variation versus the coupling coefficient and radius of MRR5 in Fig. 14 is depicted in Fig. 16. As indicated in the graph, the optimum value of CR is 21.68 dB and is obtained for the combination  $k=0.22$  and  $R=3.19 \mu\text{m}$ .

The ER is defined as

$$ER \text{ (dB)} = 10\log\left(\frac{P^1_{min}}{P^0_{max}}\right) \tag{11}$$

where  $P^1_{min}$  and  $P^0_{max}$  are the minimum and maximum values of the peak intensity of high and low level, respectively. The ER change versus the coupling coefficient and radius of MRR5 in Fig. 14 is depicted in Fig. 17. As indicated in the graph, the optimum value of ER is 14.94 dB and is achieved for the combination  $k=0.22$  and  $R=3.19 \mu\text{m}$ .

The AM is defined as



**Fig. 17** ER versus **a** MRR coupling coefficient, **b** MRR radius

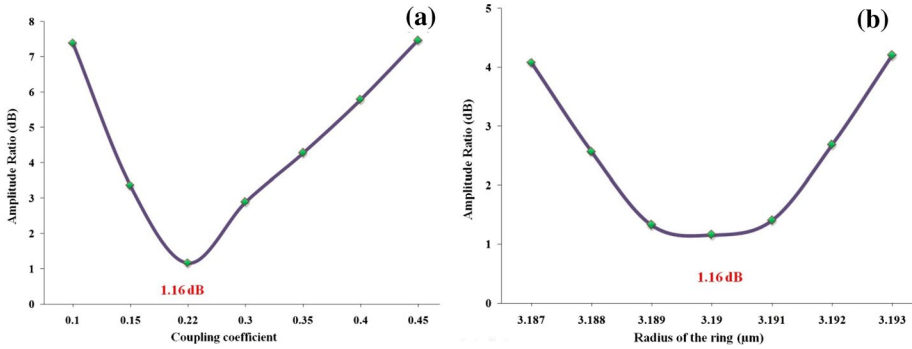


Fig. 18 AM against a MRR coupling coefficient, b MRR radius

$$AM \text{ (dB)} = 10 \log \left( \frac{P_{max}^1}{P_{min}^1} \right) \tag{12}$$

where  $(P_{max}^1)$  and  $(P_{min}^1)$  is the maximum and minimum value of high level, respectively, at the MRR output. The variation of the AM versus the coupling coefficient and radius of MRR5 in Fig. 14 is depicted in Fig. 18. As indicated in the graph, the optimum value of AM is 1.16 dB and is attained for the combination  $k=0.22$  and  $R=3.19 \mu\text{m}$ . These results show that the AO parallel PRBS generator achieves better performance than its serial counterpart for the same rate multiplication (Hossain et al. 2021a).

The On–Off Ratio (OOR) is also a useful figure-of-merit of the MRR-based AO parallel PRBS generator and it can be expressed according to (13) (Hossain et al. 2021b), where  $T_{max}$  and  $T_{min}$  represent the MRR “ON” and “OFF” intensity at resonance, respectively:

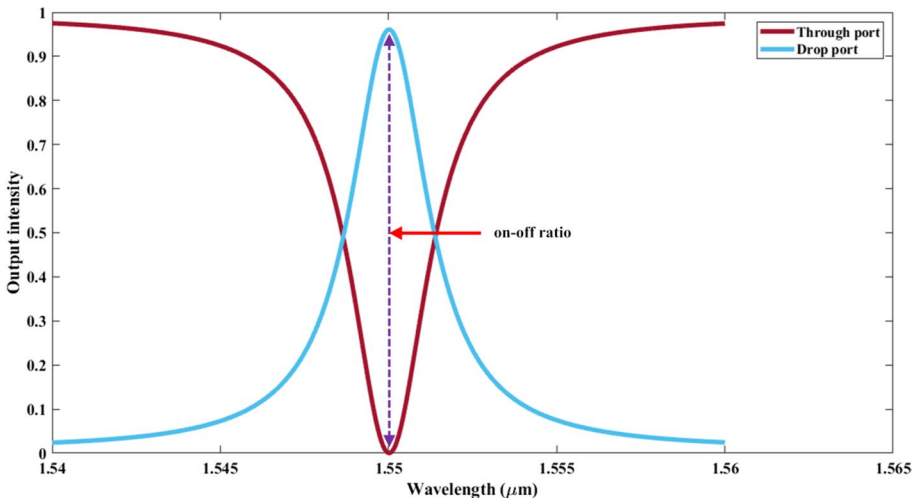
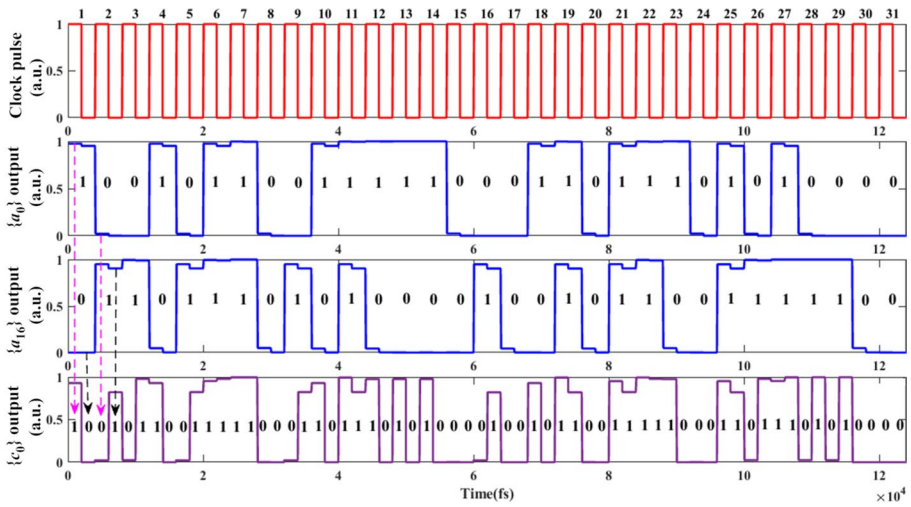


Fig. 19 MRR On–Off ratio

**Table 7** MRR parameters values for parallel PRBS generator simulation

Sl. No	Parameter	Symbol	Optimized value
1	Coupling coefficient of all MRRs	k	0.22
2	MRR radius	R	3.19 μm
3	MRR effective cross-sectional area	A	0.2 μm <sup>2</sup>
4	MRR resonant wavelength	λ <sub>res</sub>	1.55 μm
5	MRR linear refractive index	n <sub>0</sub>	3.48
6	MRR nonlinear refractive index	n <sub>2</sub>	6 × 10 <sup>-18</sup> m <sup>2</sup> /W
7	MRR attenuation coefficient	α	0.0005 μm <sup>-1</sup>
8	TPA coefficient	β	9.95 × 10 <sup>-10</sup> cm/W



**Fig. 20** Simulation results of rate doubling at 500 Gb/s with AO 5-bit degree parallel PRBS generator

$$\text{On – Off Ratio} = \frac{T_{\max} (\text{MRR drop port})}{T_{\min} (\text{MRR through port})} \tag{13}$$

Using Eqs. (6), (7) and (13) we obtain and plot Fig. 19, from which the ORR is found to be nearly 34.03 dB. This attained value ensures high performance of the MRR-based AO circuit (Saeung and Yupapin 2008).

### 6 Parallel PRBS generator rate doubling and quadrupling simulation results

The operation of the designed MRR-based AO parallel PRBS generator for rate doubling and quadrupling has been simulated assuming rectangular non-return-to-zero (NRZ) data pulses. Technologically, these pulses can be generated in the optical domain at hundreds of Gb/s per data channel by exploiting the recent advancements of photonic materials together with those in digital signal processing (Zhu et al. 2021). Table 7 lists the parameters values

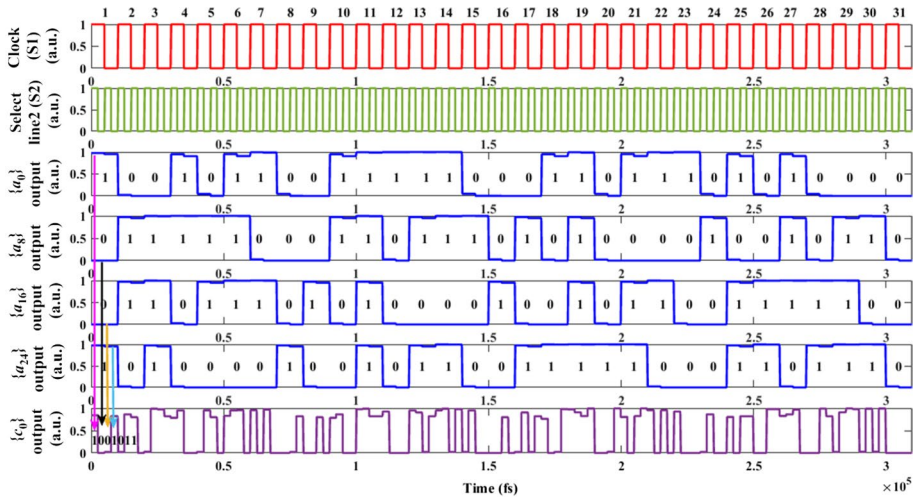


Fig. 21 Simulation results of rate quadrupling at 400 Gb/s with AO 5-bit degree parallel PRBS generator

used in the simulations. In particular those for the MRRs coupling coefficient and radius are the optimized ones that have been specified according to Sect. 5. The simulation results of PRBS rate doubling and quadrupling using the parallel PRBS generator are shown in Figs. 20 and 21, respectively.

The data rates achieved here using the parallel PRBS generator are 500 Gb/s and 400 Gb/s for speed doubling and quadrupling, respectively.

The simulation results shown in Figs. 20 and 21 agree with those cited in Table 1 and 2, respectively, which supports the correctness of the adopted design approach.

### 7 Conclusion

In conclusion, we have proposed and described the design of an all-optical parallel PRBS generator for speed enhancement by combining D flip-flops, XOR gates and 2:1 and 4:1 multiplexers implemented using microring resonator-based switches. Using as reference a 5-bit degree PRBS, we achieved PRBS rate doubling and quadrupling to 500 Gb/s and 400 Gb/s, respectively. The operation of the sequential circuit has been simulated and the obtained results have been validated by comparison to the corresponding truth tables. The performance of the scheme has been evaluated and optimized by considering and quantifying the impact of MRR critical operating parameters on appropriate metrics. With the proper MRR design, which is technologically feasible, the predicted values of these metrics guarantee high performance rate multiplication. In this manner, and owing to the advantages of MRR-based technology, the AO parallel PRBS generator holds the promise of extending the sequential functionalities of ultra-high speed signal processing in the optical domain.

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## Declarations

**Conflict of interest** The authors have declared no conflict of interest.

**Ethics approval** This article does not contain any studies with human participants or animals performed by any of the authors.

**Consent to participate** All authors are agreed and gave their consent to participate in this research work.

**Consent for publication** All authors are agreed and gave their consent for the publication of this research paper.

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