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SDR-Based Readout Electronics for the ECHo Experiment

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Abstract

Due to their excellent energy resolution, the intrinsically fast signal rise time, the huge energy dynamic range, and the almost ideally linear detector response, metallic magnetic calorimeters (MMC)s are very well suited for a variety of applications in physics. In particular, the ECHo experiment aims to utilize large-scale MMC-based detector arrays to investigate the mass of the electron neutrino. Reading out such arrays is a challenging task which can be tackled using microwave SQUID multiplexing. Here, the detector signals are transduced into frequency shifts of superconducting microwave resonators, which can be deduced using a high-end software-defined radio (SDR) system. The ECHo SDR system is a custom-made modular electronics, which provides 400 channels equally distributed in a 4 to 8 GHz frequency band. The system consists of a superheterodyne RF frequency converter with two successive mixers, a modular conversion, and an FPGA board. For channelization, a novel heterogeneous approach, utilizing the integrated digital down conversion (DDC) of the ADC, a polyphase channelizer, and another DDC for demodulation, is proposed. This approach has excellent channelization properties while being resource-efficient at the same time. After signal demodulation, on-FPGA flux-ramp demodulation processes the signals before streaming it to the data processing and storage backend.

Keywords Metallic magnetic calorimeters · Software-defined radio · Frequency-division multiplexing · Microwave SQUID multiplexer · Data acquisition · Polyphase channelizer

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1 Introduction

Metallic magnetic calorimeters (MMC) offer excellent sensor properties for various applications. The energy resolution and dynamic range, fast signal rise time, and the almost ideally linear detector response are the main benefits compared to other calorimeter types [1]. One of the first experiments employing large-scale MMC detector arrays with thousands of pixels is the *Electron Capture in ^{163}Ho experiment* (ECHo) [2].

ECHo is designed to reach sub-eV/c^2 sensitivity on the electron neutrino mass by calorimetrically measuring the electron capture (EC) spectrum of the nuclide ^{163}Ho with MMCs. The present stage of the experiment, ECHo-100k, aims at an event rate of over 10^5 Bq over all sensors. Assuming 10 Bq per sensor, the experiment will require an amount of 10^4 sensors. As a consequence, the use of a conventional dc-SQUID[1]-based parallel readout [1] requiring up to ten leads per detector channel is impossible, due to constraints on the thermal heat load, system complexity, and cost.

A promising solution for reading out such large MMC-based detector arrays is microwave SQUID multiplexing [3, 4]. This technique has proven to provide high multiplexing factors for transition edge sensor arrays. However, it has not been used for reading out metallic magnetic calorimeters within a real application due to a number of reasons: Existing microwave SQUID multiplexers that have been developed for TES readout, for example, do not provide enough bandwidth per channel to resolve the intrinsic fast signal rise time of MMCs [1, 5], employ inductive chokes within the input circuit [3] that would strongly affect the signal size of MMCs [1], and do not provide impedance matching of the input circuitry to existing MMCs [1, 6]. Therefore, the development of microwave SQUID multiplexers specifically optimized for MMC readout is required. The remainder of this paper will briefly introduce the microwave SQUID multiplexing technique. After that, an overview of the room temperature electronics customized explicitly for the ECHo experiment will be given. The heterogeneous channelization is one of the critical components and will, therefore, be described in more detail. Eventually, some of the first results are presented.

2 Microwave SQUID Multiplexing

Reading out a huge amount of metallic magnetic calorimeters with very few connections interfacing the cryostat can be achieved using microwave SQUID multiplexing. This method is a frequency-division multiplexing (FDM) scheme that modulates the sensor information on the amplitude and phase of a microwave signal [3]. The carriers are in the range between 4 and 8 GHz, and a single channel is designed to occupy 1 MHz of baseband bandwidth. For the ECHo experiment, a total number of 400 readout channels are spread over the 4 GHz spectrum. Each channel is separated

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[1] Direct-current superconducting quantum interference device.
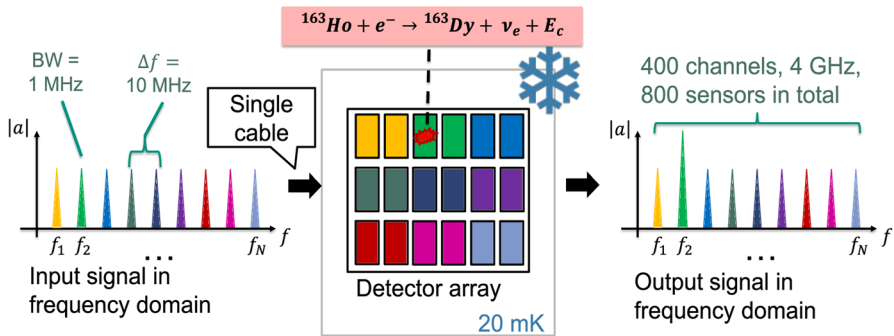
Fig. 1 Readout scheme for microwave SQUID multiplexing: a tone comb is used to stimulate the sensor channels, which modulate the amplitude and phase due to deposited energy (Color figure online)

by 10 MHz to minimize the cross talk between adjacent channels. The sensors are coupled through a microwave resonator to a common transmission line. The array of resonator channels can be measured by introducing a frequency comb to the transmission line of the sensor array. Every tone corresponds to the resonance frequency of an individual channel, each being coupled to two sensors. One sensor shifts the resonance to a higher frequency, one to a lower frequency. By monitoring the polarity of the resulting phase shift signal, events in different sensors can be easily distinguished. The transmitted comb can be measured at the output of the transmission line. A sensor event changes the S_{21} parameter of the resonance, thus the amplitude and phase of the corresponding tone. This modulation can be measured in the output signal (see Fig. 1). However, signals happening synchronous in time in both pixels appear as a summed signal that can be misinterpreted as a signal whose height is given by the difference of the energy of both events. Nevertheless, this scenario is very unlikely taken into account the expected event rate such that the enhancement of the overall channel count exceeds this potential drawback significantly.

3 Software-Defined Radio Hardware

The detector signals are transduced into frequency shifts of superconducting microwave resonators that can be deduced using a high-end software-defined radio (SDR) system. Although SDR is quite common in communication engineering, commercially available systems cannot fulfill the requirements of the ECHo project. Therefore, a custom-made SDR system is being developed. It combines analog mixing and digital signal processing (see Fig. 2). Existing setups either cover a large multiplex and small signal bandwidth [7] or small multiplex and large signal bandwidth [8].

The proposed system is designed specifically for the ECHo experiment such that it can continuously acquire and process all 400 channels in the frequency band between 4 and 8 GHz. The signal processing chain includes both analog RF mixing and digital signal processing within a field-programmable gate array (FPGA).
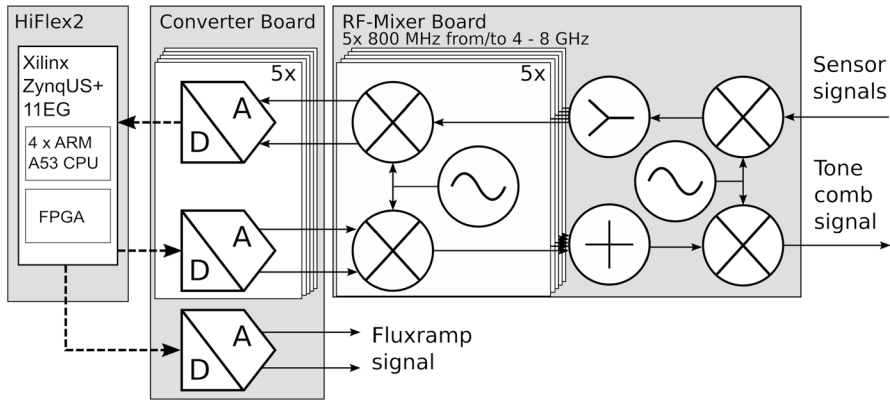
Fig. 2 Signal flow diagram of the SDR system: the FPGA is connected to five ADC, DAC pairs that are connected to individual I&Q mixers (×). With integrated local oscillators, the spectra are mixed in an intermediate frequency band. Afterward, the generated tone comb spectra are then combined (+) and mixed (×) again to resonators frequency interval. The output tone comb is fed in the cryostat where it is modulated by the sensor array. Vice versa, received modulated tone comb is mixed down to an intermediate band, split (≻) and frequency converted to the complex basebands. Filters and signal-conditioning elements are not shown in the diagram. The front end also provides two low-frequency outputs for the fluxramp modulation signals

The electronics of ECHo divides the spectrum into five sub-bands that cover after anti-aliasing filters a bandwidth of 800 MHz each [9]. Five I&Q mixers are used, in which the in-phase and quadrature components are generated by AD9144 digital-to-analog converters and recorded by AD9680 analog-to-digital converters. Both are operated at 1 GS/s sampling rate. The frequency conversion builds on a two-stage superheterodyne converter with an intermediate frequency (IF) band. This allows to take advantage of well-balanced, lower bandwidth I&Q mixers for the first stage. The mixers translate between a 800 MHz complex baseband and an IF band between 0.5 GHz and 4.5 GHz. Subsequently, the 800 MHz IF subspectra are joined to a common IF spectrum, which is translated to the RF band of the resonators by conventional mixers. Additionally, a MAX5898 dual-channel digital-to-analog converter is integrated to provide a fluxramp modulation signal for the SQUIDs [10]. Fluxramp demodulation is beyond the scope of this paper and will not be further discussed here.

For digital signal processing, the custom FPGA board HiFlex2 is used. It integrates a Xilinx Zynq US+ 11EG [11] system-on-chip with a quad-core ARM processor, a real-time processor, and an FPGA. The FPGA region provides 2928 DSP slices, 298560 CLB LUT, 600 36 kbit BRAM blocks, and 80 244 kbit URAM blocks.[2] The greater part of the digital signal processing is realized in the FPGA (see Fig. 3). On the sender side, the FPGA generates the frequency comb, which is transmitted to the DAC. On the receiver side, the frequency comb is split into its

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[2] DSP: Digital signal processor, CLB LUT: configurable logic block lookup table, BRAM: block random access memory, URAM: ultra random access memory.
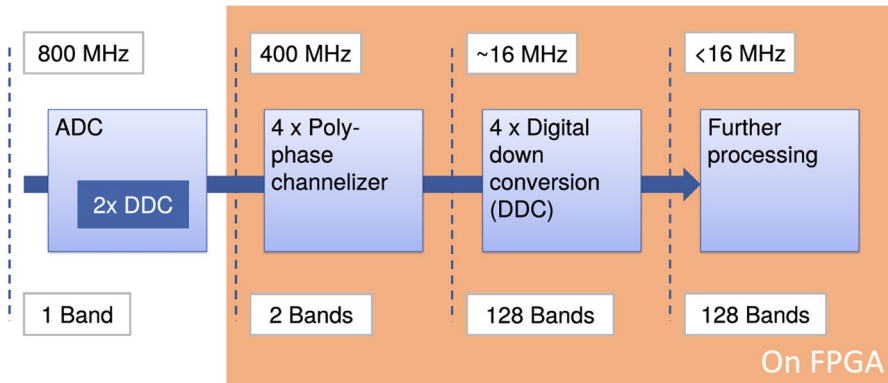
Fig. 3 Channelizing chain on the acquisition side with DDC on ADC chip, and filtering on FPGA. ECHo employs five chains resulting in a total of 640 sub-bands after the filters (Color figure online)

channels using the channelization cascade, being described in the next section. After that follows the fluxramp demodulation, resulting in the individual detector signals. The last step is event detection for each pixel and the transmission of the event data to the backend server. The processor on the board is mostly used for calibration and configuration purposes as well as forwarding data to the backend server [9].

4 Channelization Cascade

The channelization of the resonator signals is one of the critical components of the ECHo SDR system. In comparison with existing readout systems for MKID[3] [7, 8] and TES[4] [12] ECHo's channelization takes advantage of new design space parameters—a next-generation FPGA and ADCs [9]. This allows on the one hand operating the filters with higher clock frequencies up to 500 MHz and on the other hand, ADCs with internal signal processing. The ADC integrates on-chip DDC that splits the input bandwidth into two separate channels. This feature enables fully pipelined, nonparallel operation of the filters in the FPGA even with significantly increased ADC sample rate.

After the coarse channelization by analog mixing described in Sect. 3, the fine channelization of the 800 MHz bands is done digitally. An efficient concept is to decimate the signal as early as possible to be able to operate sequentially and utilize time-division multiplexing (TDM). Therefore, several mixing and decimating stages are implemented on the hardware (see Fig. 3). The first stage, a DDC, is calculated on the ADC chip. Two of the four on-chip DDC convert the input spectrum to 400 MHz bands with 63.3 dB alias protection (385 MHz with > 100 dB alias protection). The separated 400 MHz bands are transferred to the FPGA via a JESD204B

[3] Microwave kinetic inductance detectors.

[4] Transition edge sensors.
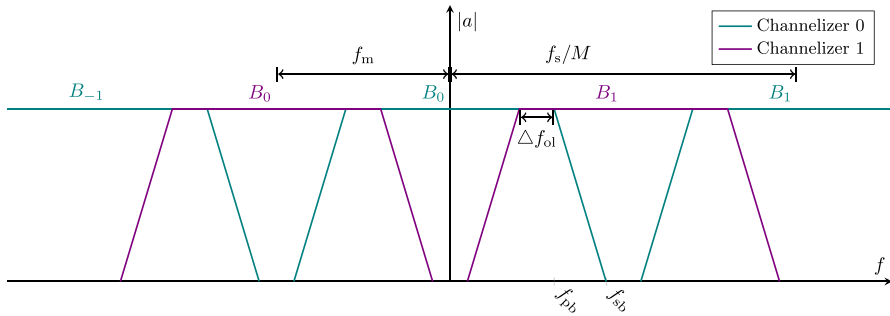
Fig. 4 Two polyphase channelizers are calculated. They are operated at a sampling rate of $f_s = 500$ MHz. The decimation of $M = 32$ allows to split the received spectrum into 32 equidistant sub-bands per filter (five are shown in the picture). One of the filters is applied after mixing the input signal with $f_m = f_s/M$. This method leads to an overlapping band structure between the two output spectra. The used coefficients provide a pass-band (f_{pb}) and a stop-band (f_{sb}) to guarantee the isolation from the next sub-band of the same filter and the overlap $f_{ol} = 3.2$ MHz to the second filter (Color figure online)

link. In the FPGA, each band is duplicated, one delayed, one shifted in frequency. This duplication is required to cover blind intervals of the polyphase channelizer (see Fig. 4). On each of these bands, two 32-band polyphase channelizers [13] are applied, two for the delayed and two for the mixed spectrum.

Each 400 MHz band pair is then split into 128 equidistant sub-bands with a bandwidth of 15.625 MHz. In the first implementation, the polyphase channelizer was chosen with > 80 dB stop-band attenuation at 10 MHz stop-band, 5.5 MHz pass-band frequency, with − 0.2 dB attenuation pass-band edge. The bands of the mixed and delayed variant are overlapping by 3.2 MHz to allow the demodulation at the pass-band edge. For these specifications, a 521-coefficient polyphase low-pass filter was used. The polyphase filter was implemented as an 18-tap TDM FIR filter with cycled coefficient sets. Within the channelizer, the resulting TDM samples are reordered in a buffer and processed by a 32-point pipelined FFT core (resources in Table 1). One resulting sub-band contains 1–2 resonator channels which are amplitude demodulated in the next step. The channelization decreases the sample rate by a factor of 32, resulting in 15.625 MHz. This scheme allows efficiently calculating the demodulation with the same structure in a time-division multiplexing scheme. A DDC was implemented to mix and filter the 32 TDM channels. The prototype FIR for the DDC was designed with nonfinal parameters. It uses a symmetric 12-coefficient structure, with the same stop-band attenuation of > 80 dB, a pass-band of 1 MHz, with − 2.78 dB at pass-band edge (resources in Table 1). The channelizer chain was implemented and verified on an FPGA platform (Xilinx ZCU102) in a loop-back configuration without converters. The modules archive the targeted clock frequency of 500 MHz. A resulting capture of the frequency response can be found in Fig. 5. The combination of the channelizer and DDC for 400 channels has a extrapolated footprint of 41.3% of the employed FPGA. This gives

Table 1 Resource consumption of the digital signal processing chain

	DSP48E2	CLB LUT	BRAM36
Polyphase channelizer	87	3443	1.5
Digital down conversion	17	2316	8
Total of 10 chains	1210	80740	175
Utilization of HiFlex2 for 10 chains (%)	41.3	27	29.2
Effective resources per resonator channel	3.03	201.9	0.439
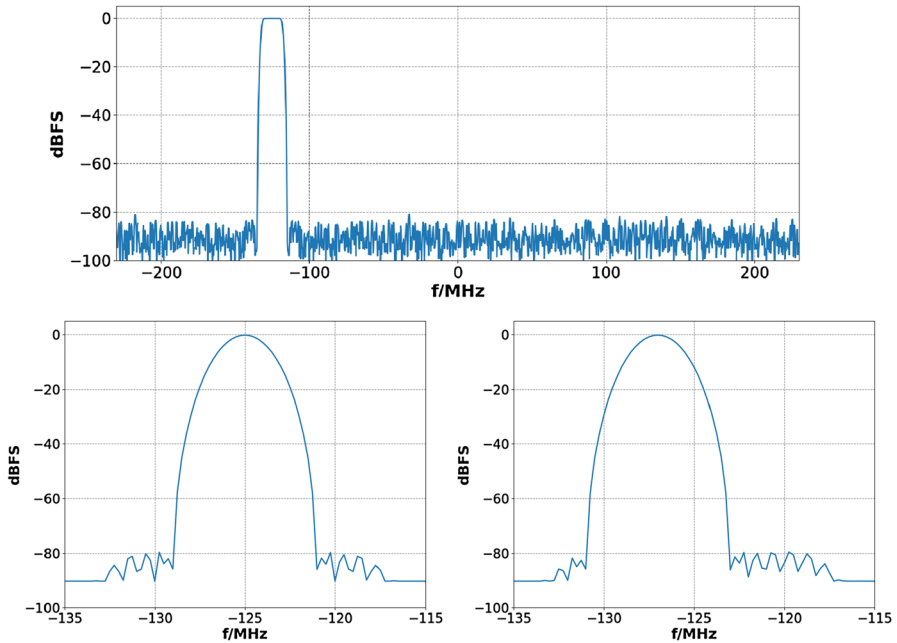
Fig. 5 Complex frequency response of a single channel of the polyphase channelizer (top). Pass-band of the shown channel after the DDC, including filtering (bottom, left: 0 Hz, right: − 2 MHz mixing) (Color figure online)

freedom to improve the characteristics of the filter structure and coefficients and integrate further modules. The demodulated channels are streamed through a DMA core to the processing system of the used Xilinx Zynq SoC. From there, it is saved on a solid-state drive.

In the next development step, the signal processing chain will be extended by additional modules, such as fluxramp demodulation [12] and event detection on the same FPGA device. Besides this, an adjustment of the channelizer and DDC characteristics is planned to fit the final parameters.

5 Summary

The ECHo experiment utilizes large MMC sensor arrays to increase the event rate and gain statistics. Parallel readout of the sensor array is not feasible; hence, microwave SQUID multiplexing is needed. The designed SDR system will cover the 4 GHz FDM processing bandwidth with analog front end and a digital processing backend. The prototype of the channelization system for ECHo is shown to be suitable for an efficient implementation on an FPGA. This efficiency gives room to further adapt the parameters to the requirements of the ECHo design values. In the next step, the fluxramp demodulation and event detection will be integrated.

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