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Comparison of *p*-*n* and *p*-*i*-*n* vertical diodes based on *p*-PMItz/*n*-Si, *p*-PMItz/*n*-4HSiC and *p*-PMItz/*i*-SiO_2/*n*-Si heterojunctions

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ABSTRACT

In this paper, we present a comprehensive comparison study between *p*-*n* and *p*-*i*-*n* vertical diodes employing diverse heterojunction configurations under dark conditions. The diodes are fabricated utilizing *p*-PMItz as the organic semiconductor layer interfacing with different inorganic substrates, including *n*-Si (n-type silicon), *n*-4HSiC (*n*-type 4H silicon carbide), and incorporating an intrinsic SiO_2 (silicon dioxide) layer in the *p*-PMItz/*i*-SiO_2/n^{++}-Si configuration. The current–voltage and dielectric characteristics are analyzed to discern the performance discrepancies among these diode configurations. The influence of heterojunction interfaces and band alignments on device behavior is investigated, shedding light on the charge transport mechanisms within these structures. Our findings reveal distinct trends in device characteristics for *p*-*n* and *p*-*i*-*n* diodes, highlighting the significance of heterojunction design in optimizing device performance. This comparative analysis offers valuable insights for the development of efficient organic–inorganic hybrid diodes tailored for various optoelectronic applications.

1 Introduction

Ongoing research in the field of *p*-*n* and *p*-*i*-*n* junctions with organic semiconductors involves the development of hybrid organic/inorganic semiconductor heterojunctions, which can expand the scope of purely organic or inorganic junctions [1]. These hybrid junctions can be used in various electronic and optoelectronic devices, such as solar cells, diodes, and transistors [2–5]. One approach to creating these hybrid junctions is through doping semiconductors, which can optimize the functionality of these devices [6, 7]. Organic semiconductor diodes fabricated using doped/undoped (high-low) homojunction structures

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have shown promise in providing controlled and high-quality current [8].

The concept involves positive and negative charges from ionized donors and acceptors in *n*-type and *p*-type organic semiconductors, respectively, creating a mixed *i*-layer co-deposited with both types of semiconductors [9]. Organic semiconductor diodes can be built in various architectures, including *p*-*n*-diodes, *p*-*i*-*n*-diodes, and Schottky diodes, each serving specific functions. There has been extensive research and investigation into the possible applications of multi-junction-based organic semiconductor devices, which are characterized by organic semiconductors grown on inorganic wafers [10, 11]. Increasing mobility in both vertical and lateral directions is crucial to enhance organic semiconductors' performance in complex multi-junction devices. This can be achieved by introducing structural order through organic polycrystals and single crystals, enabling band-like charge transport and maximizing charge carrier mobility [12]. Organic semiconductors are versatile materials used in various applications like OLEDs, solar cells, transistors, and sensors, with the potential for electrically driven organic lasers, overcoming challenges associated with low current densities and losses due to charge injection [13]. Overall, ongoing research in this field aims to improve the performance and functionality of electronic and optoelectronic devices by optimizing the properties of organic and hybrid semiconductor *p*-*n* and *p*-*i*-*n* junctions.

To describe charge transport mechanisms in diverse materials, however, there exist a number of models, including Poole–Frenkel, Schottky, and space charge limited-conduction (SCLC) mechanisms [14]. Carrier trapping centers exist in prohibited bandgaps, which have a significant impact on the electrical characteristics of semiconductor semiconductors. In the space charge limited-current model, current has a power-law dependence on applied voltage ($I \propto V^m$), and this model is used to describe the electrical properties of semiconductor and insulator materials [15]. A prior work examined some surface and optoelectronic properties of phenanthroimidazole derivative (PMItz), an organic semiconductor of the *p*-type [16].

Overall, using of a new organic layer (*p*-PMItz), the device architecture of *p*-*n* and *p*-*i*-*n* diodes can impact their performance, making them a promising alternative to traditional inorganic diodes for device applications. The choice of electrodes and *p*-PMItz organic layer can also impact their current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) characteristics, with In (indium) and Ag (silver) being commonly used for the anode and cathode, respectively. In this study, we provide an extensive comparative analysis of *p*-*n* and *p*-*i*-*n* vertical diodes using various heterojunction arrangements. An intrinsic SiO_2 (silicon dioxide) layer is incorporated in the *p*-PMItz/*i*-SiO_2/n^{++}-Si configuration, and the diodes are manufactured using *p*-PMItz as the organic semiconductor layer interacting with various inorganic substrates, such as *n*-Si (*n*-type silicon) and *n*-4HSiC (*n*-type 4H silicon carbide).

2 Material and methods

The material and methods section outlines the systematic approach to developing and characterizing vertical diodes composed of *p*-PMItz/*n*-semiconductor and *p*-PMItz/*i*-SiO_2/*n*-semiconductor heterojunctions. Conducted an extensive literature review to understand existing knowledge about vertical diodes. Identified key research gaps, challenges, and potential improvements.

- Material Selection and Preparation:
  - Selected appropriate semiconductor material for heterojunction.
  - Synthesized *p*-PMItz and characterized its properties [17].
  - Prepared semiconductor material and *p*-PMItz in suitable forms for device fabrication.
- Device Fabrication:
  - Designed the structure of vertical diodes based on *p*-PMItz/*n*-semiconductor and *p*-PMItz/*i*-SiO_2/*n*-semiconductor heterojunctions.
  - Fabricated devices using standard semiconductor fabrication techniques, including deposition, lithography, and etching.
- Characterization Techniques:
  - Implement various characterization techniques to evaluate the structural and electronic properties of the fabricated diodes.
  - Use techniques such as scanning electron microscopy (SEM), and Optical Bandgap analyze

– Device Testing:

  - Set up experimental conditions to test the electronic characteristics of the diodes.
  - Measure the generated electrical signals.
  - Evaluate the diode performance parameters.

– Optimization:

  - Iterate the fabrication and testing process to optimize the performance of the diodes.
  - Adjust parameters such as layer thickness, material composition, and device architecture based on the experimental results.

– Data Analysis:

  - Analyze the collected data using statistical and graphical methods.
  - Compare the results with existing literature and discuss the significance of findings.

2.1 Optical bandgap of *p*-PMItz

To find PMItz's bandgap, the fluctuation of $(\alpha hv)^2$ with energy (hv) was plotted. PMItz absorption measurements were used for this. Figure 1 shows the graph PMItz $(\alpha hv)^2$–(hv). Based on the information gleaned from the graph, 3.02 eV was determined to be the optical bandgap (E_g).

2.2 Experimental procedure

In this process, *n*-Si, *i*-SiO_2/n^{++}-Si, and *n*-4HSiC substrates were utilized to fabricate the devices. All materials underwent cleaning in an ultrasonic bath containing a soapy water solution for 10 min. Subsequently, the substrates were thoroughly rinsed with ultrapure water. *i*-SiO_2/n^{++}-Si substrates were not subjected to further cleaning and were dried with nitrogen gas after removal from the solution. *n*-Si and *n*-4HSiC substrates were immersed in acetone in a glass beaker and underwent ultrasonic cleaning for 10 min. Following cleaning with acetone, the *n*-Si and *n*-4HSiC substrates were transferred to a glass beaker filled with propanol and underwent another 10 min of ultrasonic cleaning. After cleaning with propanol, the surfaces of the *n*-Si and *n*-4HSiC substrates were dried with nitrogen gas, completing the substrate cleaning process.

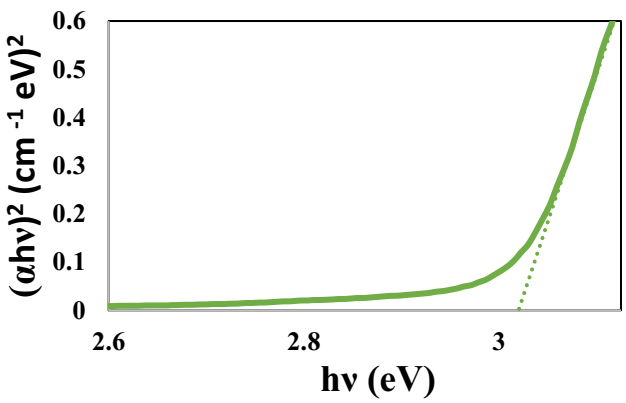

Fig. 1 Optical bandgap of PMItz

Before deposition of Ag (silver) and In (indium) contacts, about 99.9% purities, were deposited onto *p*-PMItz using the PVD (Physical Vapor Deposition) method. Ag contact deposition was performed using a Tungsten spoon crucible at a pressure of 5.3×10^{-5} Torr and a temperature of 21 °C. In contact deposition was carried out using a molybdenum spoon crucible at a pressure of 2.0×10^{-5} Torr and a temperature of 21 °C. The contacts were masked and cast in circular form with a diameter of approximately 0.777 mm. Six devices have been fabricated as illustrated in Fig. 2.

In order to analyze the electrical properties of these devices, *I-V* measurements were carried out at room temperature using a Keithley 2400 source meter. Figure 3 illustrates the workings of the system.

3 Results and discussion

3.1 Main electronic characteristics

The current-conduction (CC) mechanism in the semiconductor devices is dependent on many factors such as the organic film, its thickness and permittivity, homogeneity of barrier height, the level of doping atoms into semiconductor, series (R_s) and shunt (R_{sh}) resistances, surface states/traps, located at the interface of organic layer/semiconductor, surface cleaning of semiconductor wafer, fabrication processes and formation of electrode contacts even at in same conditions. The standard thermionic emission (TE) model was generally used using the forward bias *I–V* measurements to investigate the CC mechanism in these structures. However, it usually deviated from the TE model for the above reasons [18, 19].

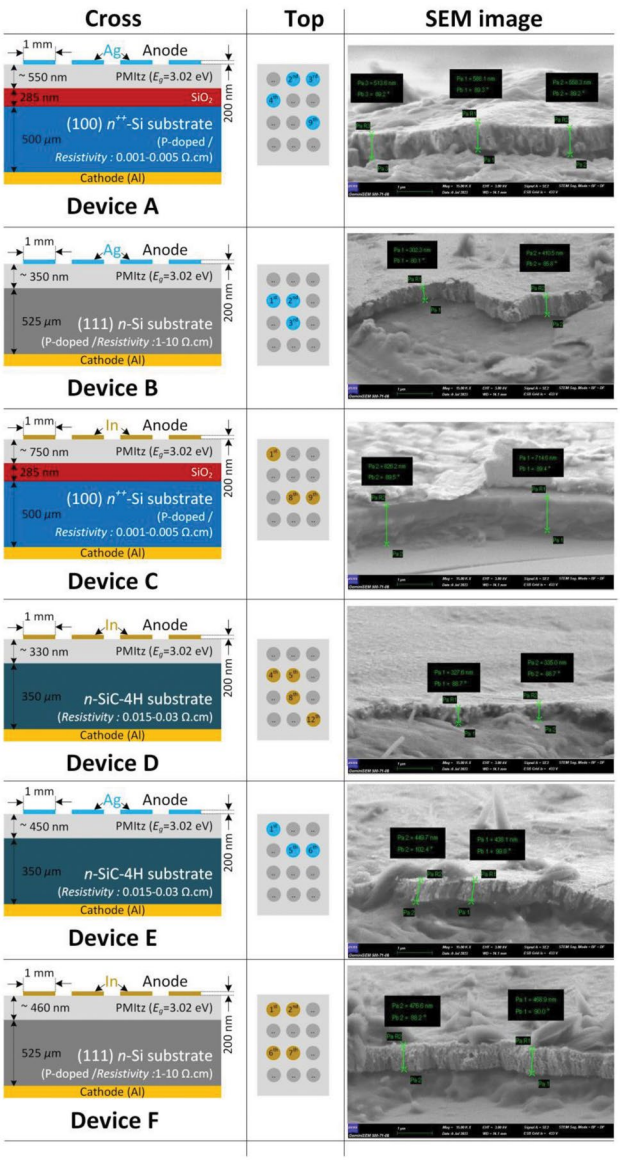

Fig. 2 Schematic illustration of the devices and SEM image

Based on *I–V* measurements conducted in the ambient environment of our fabricated device, we plotted the *I–V* characteristics curve in dark conditions for various contacts. Figure 4 illustrates the plot depicting the *I–V* characteristics of the devices for both forward and reverse bias at room temperature. This confirms that the device exhibits appropriate rectifying diode-like behavior, which can be analyzed using the TE theory. According to this theory, current flow is governed by majority carriers overcoming a potential barrier, where only electrons with energy surpassing the barrier contribute to the current. By maintaining the turn-on voltage at approximately 0.3 V, which is lower than the applied bias voltage, the current increases rapidly in response to the bias voltage, indicating typical diode behavior.

As depicted in Fig. 4, the diode exhibits an exponential increase in forward bias current with voltage, whereas the reverse bias current remains low and relatively independent of voltage. The devices demonstrate good rectifying behavior under dark conditions, as illustrated in Fig. 4. These characteristics provide information about the *p*-PMItz/*n*-Si, *p*-PMItz/*n*-4HSiC and *p*-PMItz/*i*-SiO_2/n^{++}-Si heterojunctions parameters, including the ideality factor (n), barrier height (ϕ_{Bo}), and reverse saturation current (I_o). The *I–V* behaviors of organic/inorganic heterojunctions are indicated. At low voltages, these junctions exhibit characteristics similar to Schottky diodes or heterojunctions [18]. The widely recognized nearly perfect equation describing the relationship between I and V can be expressed as [18]:

$$I = I_O\left[exp\frac{q(V - IR_s)}{nkT} - 1\right] \quad (1)$$

In this context, n represents the ideality factor, I_O signifies the reverse saturation current, V denotes the applied bias voltage, q stands for the electronic charge,

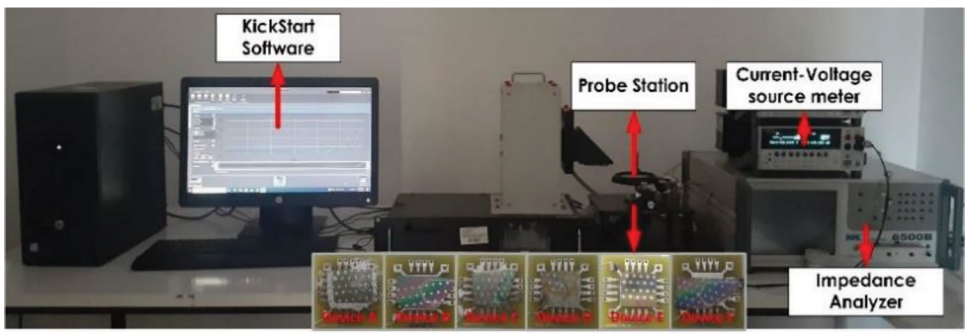

Fig. 3 The measurement system

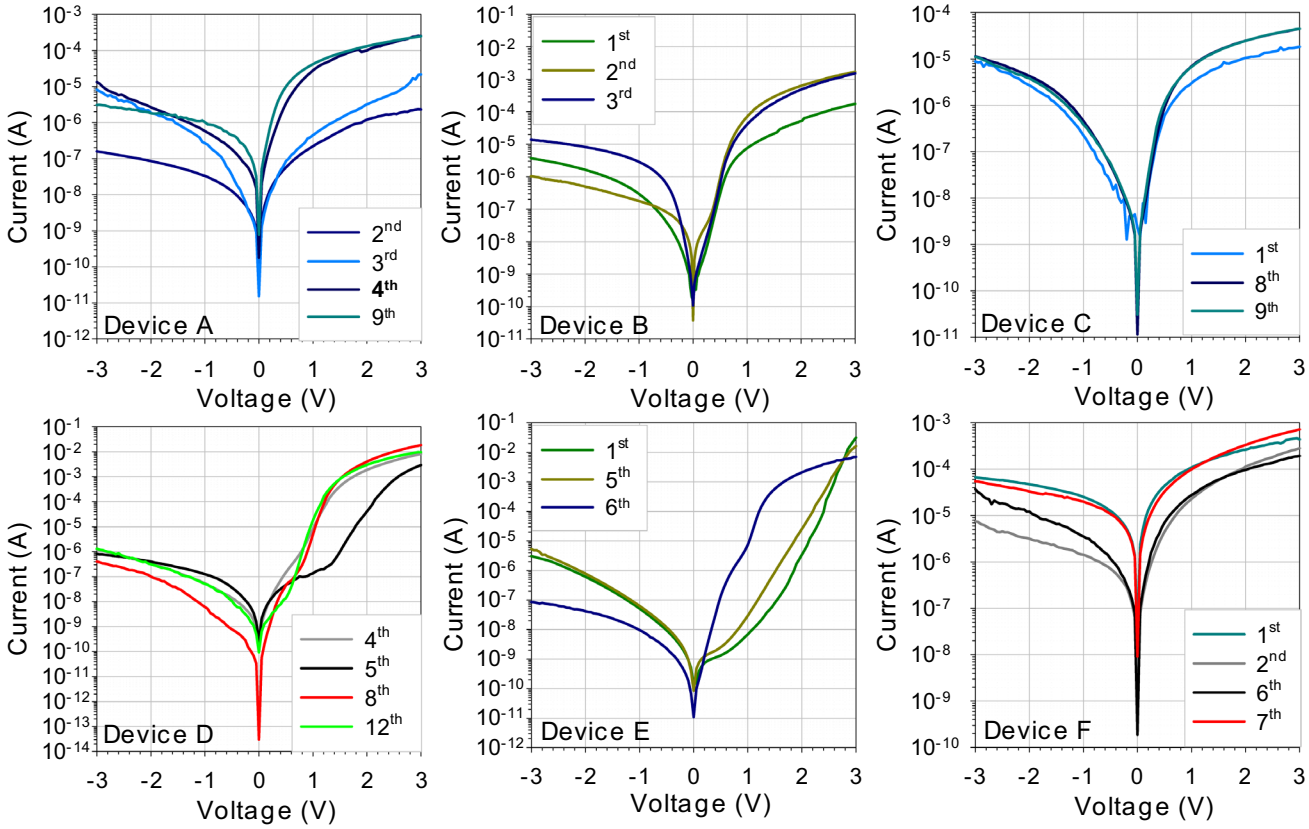

Fig. 4 The devices' semi-logarithmic *I-V* characteristics for forward and reverse bias at room temperature

equivalent to 1.602×10^{-19} *C*, *k* represents the Boltzmann constant, which amounts to $1.3806 \times 10^{-23} \frac{J}{K}$, *T* indicates the absolute temperature measured in Kelvin, R_s denotes the series resistance of the diode, and the term IR_s represents the voltage drop across the R_s. [18]. The value of I_O can be derived from the portion of the straight-line intercept of $\ln I - V$ curves at $V = 0$, and it is provided by:

$$I_O = AA^*T^2\left[exp(-\frac{q\Phi_{BO}}{kT})\right] \tag{2}$$

Here, A represents the rectifier contact area, which is equal to $7.85 \times 10^{-3} cm^2$, and A^* signifies effective Richardson constant (112 A.(K.cm)$^{-2}$ for *n*-Si and 146 A.(K.cm)$^{-2}$ for *n*-4H-SiC. The value of the zero-bias or apparent barrier height ϕ_{BO} can be determined using Eq. (3). The *n* values for these diodes were also computed from the linear portion of the $InI - V$ plots, which can be expressed as follows [18]:

$$n = \frac{kT}{q}\left(\frac{dV}{d(\ln I)}\right) = 1 + \frac{d}{\varepsilon i}\left(\frac{\varepsilon s}{Wd} + qNss\right) \tag{3}$$

In Eq. 3; the d, ε_i, ε_s, W_d, and N_{ss} quantities are the interlayer thickness, dielectric of interlayer, dielectric of semiconductor, and surface states, respectively. Consequently, the value of ϕ_{BO} is computed from Eq. 2 using the obtained values of I_O and A for each diode as follows [18]:

$$\phi_{BO} = \frac{kT}{q} In\left(\frac{AA^*T^2}{I_O}\right) \tag{4}$$

The ϕ_{BO}, n, R_s, R_{sh}, and rectifier ratio (RR) values were computed for the entire devices and each contact, as presented in Table 1. Among devices B, D, E, and F with *p-n* structure with different metal contacts, it has been observed that in devices with *p*-PMITz/*n*-Si junctions, the n and I_o values of Device B are lower than Device F, and the ϕ_{BO} and RR values are higher. Better results were observed for Device B with Ag metal contact of the same junction. On the other hand, in devices with *p*-PMITz/*n*-4HSiC junctions, the ϕ_{BO}, n and I_o values of Device D and Device E are seen to be close to each other and exhibit contact-based differences. It has been observed that the RR output of

Table 1 The main parameters of the *p-n* and *p-i-n* heterojunctions

Device	Contact	from *TE*			from *Ohm's Law*		from *Cheung's*	
		$I_O\,(A)$	n	$\Phi_{BO}\,(eV)$	$R_{sh}(K\Omega)$ at -3V	$R_s(K\Omega)$ at 3V	$R_s\,(K\Omega)$	RR
Device A	2nd	1.99×10^{-8}	16.58	0.73	18,847.75	1301.29	1206.7	1.45×10^{1}
	3rd	1.98×10^{-8}	12.85	0.73	367.70	139.24	141.28	2.64×10^{0}
	4th	8.22×10^{-7}	11.36	0.63	227.27	12.03	10.94	1.89×10^{1}
	9th	4.12×10^{-6}	17.27	0.59	974.82	12.17	13.31	7.00×10^{0}
Device B	1st	2.80×10^{-10}	2.94	0.83	817	17.14	43.83	4.77×10^{1}
	2nd	2.77×10^{-10}	2.63	0.83	2888	1.77	1.45	1.63×10^{3}
	3rd	4.99×10^{-10}	2.69	0.82	218	1.98	1.56	1.10×10^{2}
Device C	1st	2.03×10^{-7}	14.83	0.67	340.14	163.93	153.30	2.07×10^{0}
	8th	2.74×10^{-7}	12.44	0.66	263.16	67.26	66.06	3.91×10^{0}
	9th	3.59×10^{-7}	13.71	0.65	269.72	67.10	64.95	4.02×10^{0}
Device D	4th	3.18×10^{-9}	5.36	0.77	2439.02	0.36	0.72	6.70×10^{3}
	5th	5.40×10^{-9}	9.78	0.76	3702.27	1.02	3.9	3.63×10^{3}
	8th	6.90×10^{-10}	5.16	0.81	7484.82	0.16	0.13	4.64×10^{4}
	12th	4.88×10^{-10}	5.33	0.82	2253.48	0.31	0.14	2.21×10^{3}
Device E	1th	2.55×10^{-10}	12.49	0.83	980.39	0.10	0.22	1.03×10^{4}
	5th	2.14×10^{-10}	8.34	0.84	561.59	0.18	0.30	3.06×10^{3}
	6th	2.71×10^{-9}	4.97	0.78	34,866.51	0.43	0.31	8.17×10^{4}
Device F	1st	3.87×10^{-6}	7.32	0.59	44.98	6.83	15	6.59×10^{0}
	2nd	2.26×10^{-6}	6.77	0.61	397.95	10.56	10.26	3.78×10^{1}
	6th	1.37×10^{-7}	4.60	0.68	80.65	15.50	6.22	5.20×10^{0}
	7th	1.02×10^{-7}	4.88	0.68	54.75	4.15	4.6	5.19×10^{0}

devices D and E is higher than the other devices, and their values show different results despite having the same junction structures. Additionally, the values of n are considerably higher than unity. On the other hand, in devices with *p*-PMITz/*i*-SiO_2/n^{++}-Si insertions, the n values of Device C are higher than in other devices, besides contact-based differences. Although it is expected that the n value should be unity in the ideal case, it is considerably different in practical applications due to the native/deposited interfacial layer, its ε_i and d values, N_{ss}, doping atoms (acceptor/donor) or depletion layer width as expressed as $[n = 1 + (d_i/\varepsilon_i)(qN_{ss} + \varepsilon_s/W_d)]$ [18]. The n values of inhomogeneous devices with a distribution of lower BHs or patches may be dominated by current flowing through lower barriers, leading to an increase in the current.

Additionally, it was observed that ϕ_{BO} and RR values were lower than other devices. The observed discrepancies between basic electrical parameters are usually rooted in the voltage-dependent, the used calculated method, which corresponds to different voltage ranges, barrier inhomogeneity, a special distribution of N_{ss} and dislocations at the junction, and interfacial layer. As seen in Eq. 3, higher values of N_{ss}, interlayer thickness, low-dielectric interlayer, and also barrier inhomogeneity yield an important increase in n value. Even if these diodes are grown under the same conditions and on the same semiconductor, they may give different results due to reasons such as the shape of the barrier, the thickness and inhomogeneity of the interfacial layer, and the inhomogeneous distribution of dopant atoms.

The parameters of R_s and R_{sh} are crucial for assessing device quality and impacting the performance of diodes. Diodes possess R_s and an interlayer, leading to the distribution of the total applied voltage among them and the depletion layer. Consequently, the reliability and quality of these devices are particularly associated with the interlayer, R_s and R_{sh}. Ideally, R_s and R_{sh} values are expected to be 0 and exceed $10^9\Omega$ respectively, in an ideal scenario [20]. However, practical circumstances often deviate from this ideal. Various methodologies exist in research to compute R_s parameters for Schottky diodes or heterojunctions,

including Ohm's law, the Cheung and Cheung method utilizing forward bias $I-V$ parameters of diodes, and Norde methods. These approaches are employed to yield reliable and valid results for R_s, which are subsequently compared across different diodes, with R_s and R_{sh} parameters initially deduced from the forward bias region and the reverse bias region of the $I-V$ parameters, respectively, utilizing Ohm's law, which are shown in Fig. 5.

3.2 Dielectric characteristics

The $C-V-f$ and $G-V-f$ outputs of the configuration were acquired at ambient conditions and are depicted in Fig. 6a and b. In this representation, the accumulation capacitance registered at 3 V shifts from 26.4 to 510 nF. By examining the outcomes aligned to the accumulation, depletion, and inversion regions, the capacitance of the configuration escalates with rising voltage but steadily diminishes towards the intense opposite domain. Additionally, the capacitance in the accumulation and depletion regions decreases with rising frequency. Through varying frequencies, electronic parameters such as diffuse potentials (V_D), donor density (N_D), and the depletion region width (W_D) are computed from the C^{-2}–V–f curve. The intersection points with the voltage axis provide the built-in voltage (V_{bi}) values, which are presented in Table 2. For a comprehensive analysis of capacitance, the C^{-2}–V relationship is elucidated utilizing the following correlation. [18, 21]:

$$C^{-2}=\frac{2}{q\varepsilon_s\varepsilon_o A^2 N_D}(V_{\mathrm{bi}}+V_R) \tag{5}$$

In this context, V_R, q, ε_s, ε_0, and A denote the reverse bias voltage, the elementary charge, the dielectric constants of the semiconductor and vacuum, and the Schottky contact area, respectively. Upon assessment, it was observed that the $C^{-2}-V-f$ curves, representing capacitance versus voltage at various frequencies, exhibited linear characteristics and were almost parallel to each other within the voltage range of − 2 to 2 V. By plotting gradient lines for each frequency and obtaining their equations, the V_D and the N_D values are calculated based on the

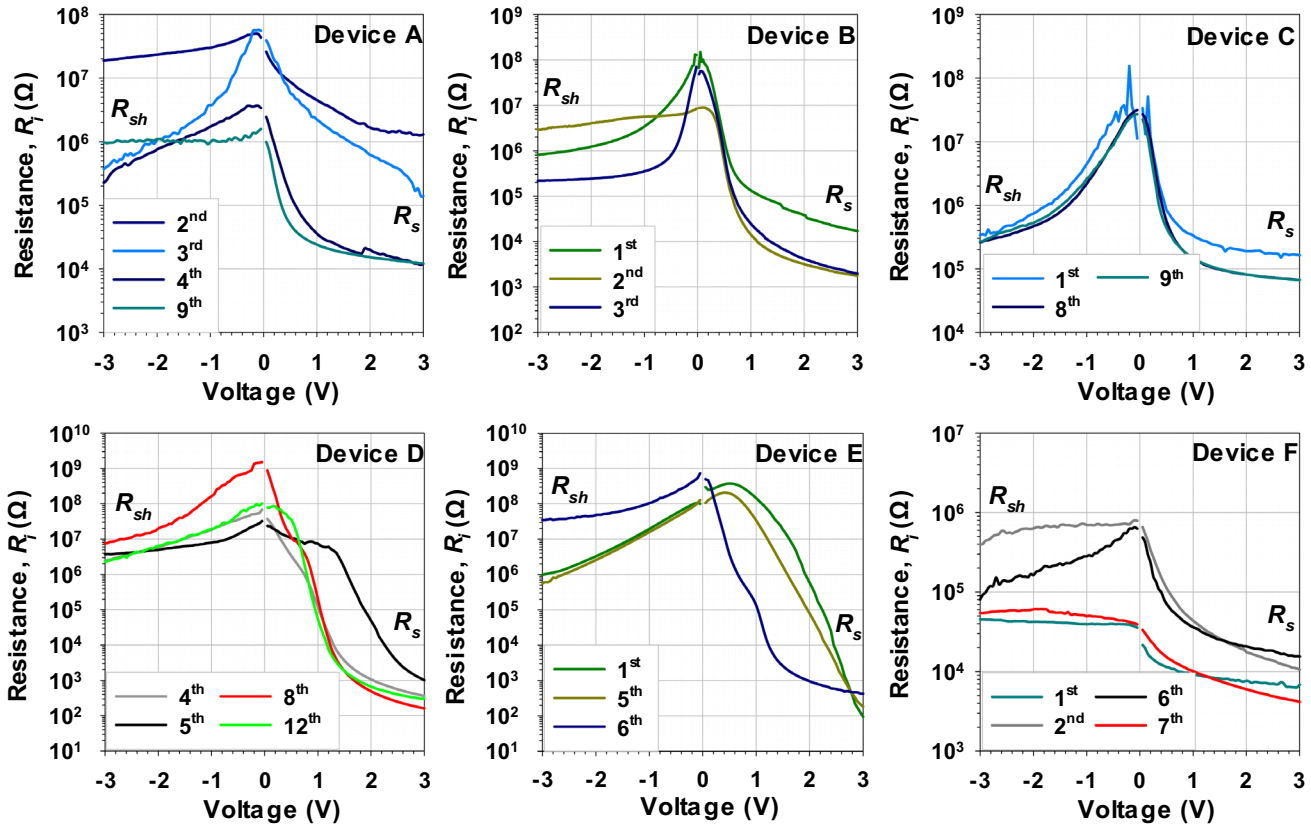

Fig. 5 The $R_i vs V_i$ characteristics of the *p-n* and *p-i-n* heterojunctions to determine both R_s and R_{sh} values

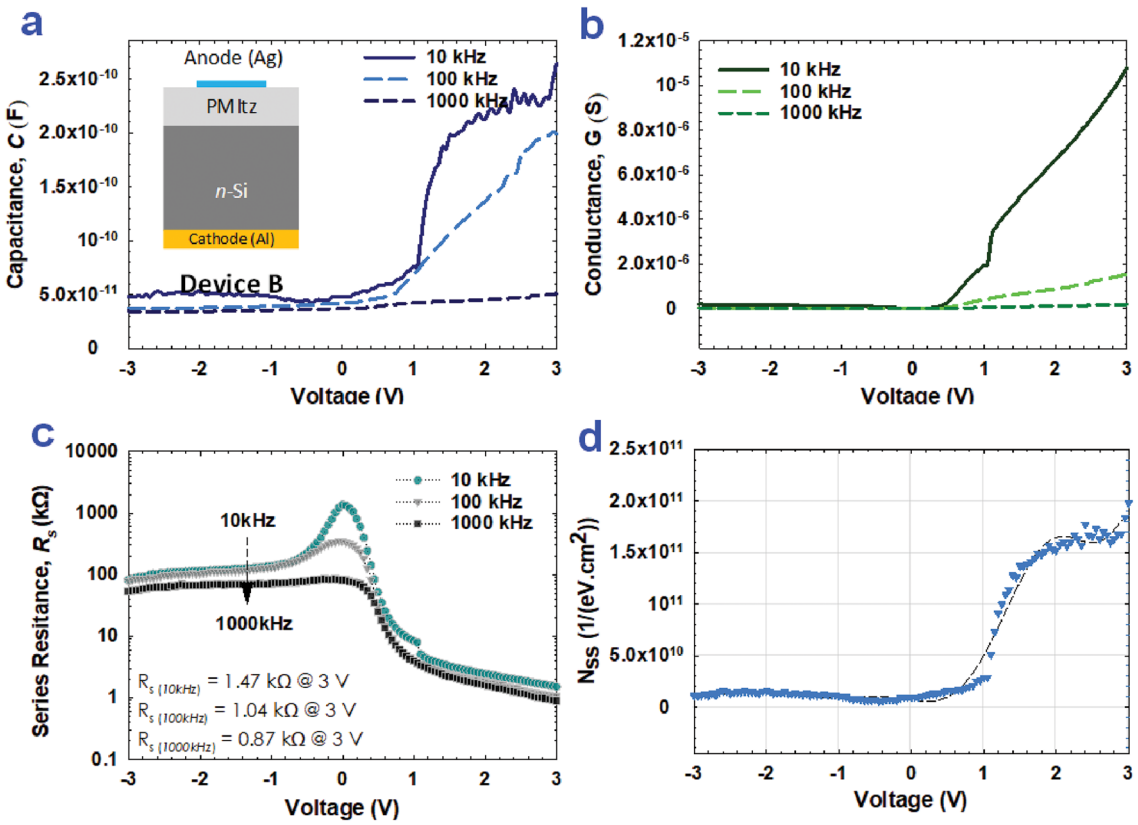

Fig. 6 **a** capacitance and **b** conductance, series resistance (**c**), and N_{ss} (**d**) characteristics corresponds to the accumulation, depletion, and inversion regions of the Device B, at distinct frequencies

Table 2 The calculated electronic parameters of Device B heterojunction structure at distinct frequencies

F (kHz)	$N_D\,(cm^{-3})$	$E_F\,(eV)$	$\phi_{B(C-V)}(eV)$	$\Delta\,\phi_B\,(meV)$	$W_D\,(nm)$	$E_m\,(\frac{V}{cm})$	$R_s(k\Omega)$ at 3.0 V
10	8.23×10^{14}	0.261	2.219	0.016	512	2.22×10^{4}	1.47
100	3.83×10^{14}	0.280	1.728	0.013	644	1.30×10^{4}	1.04
1000	6.72×10^{14}	0.266	2.969	0.017	666	2.36×10^{4}	0.87

intersection points with the voltage axis, representing the built-in voltage V_{bi} values, for each frequency. The V_{bi} values of the configuration typically range from approximately 1.0–2.0 V and demonstrate increased sensitivity with higher frequencies.

The V_D diffusion potential for each frequency value is inferred from V_{bi} obtained from the $C^{-2}-V-f$ graph. [18]:

$$V_{bi} = V_D - \frac{kT}{q} \tag{6}$$

The W_D, derived from the points where the C^{-2}–V–f curves intersect and their gradients [18]:

$$W_D = \left(\frac{2\varepsilon_s\varepsilon_0\left(V_{bi}+V_R\right)}{qN_D}\right)^{\frac{1}{2}} \tag{7}$$

In theory, the Fermi level (E_F) of a Schottky diode or heterojunction structure is [18]:

$$E_F = \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right) \tag{8}$$

In this scenario, the effective density of states (N_c) at the conduction band equals $4.82\times10^{15}T^{1.5}(m_e^*/m_0)^{1.5}$. The ratio of the effective electron mass for silicon is 1.08. Moreover, the $\frac{kT}{q}$ rep-

resents the thermal energy [22]. Furthermore, the relationship between the barrier height $\phi_{B(C-V)}$, V_D, E_F, and $\Delta\phi_B$ is provided in Eq. 9:

$$\phi_{\mathrm{B\ (C\text{-}V)}} = \mathrm{V}_D + E_F - \Delta\phi_B \tag{9}$$

Here, $\Delta\phi_B$ represents the reduction of the image force barrier lowering and can be computed in the following manner [18]:

$$\Delta\phi_B = \left(\frac{qE_m}{4\pi\varepsilon_S\varepsilon_0}\right)^{\frac{1}{2}} \tag{10}$$

In Eq. 10, E_m denotes the electric field and can be determined using the subsequent correlation [18]:

$$E_m = \left(\frac{2qN_DV_{bi}}{\varepsilon_S\varepsilon_0}\right)^{\frac{1}{2}} \tag{11}$$

By utilizing the $C-V-f$ outputs, all electronic parameters were determined using the aforementioned calculation methods and are detailed in Table 2. In this context, the W_D, $\phi_{B(C-V)}$, $\Delta\phi_B$ and E_m parameters were noticed to rise with ascending frequency (see Fig. 6). Experimentally, the values dependent on frequency exhibit significant variation at ambient conditions. Specifically, the N_D, W_D, and $\phi_{B(C-V)}$ values experience changes within the ranges of $8.23-3.83\times10^{14}cm^{-3}$, 512–666 nm, and 1.728–2.969 eV, respectively, with increasing frequency. The higher values of ϕ_B can be explained by the higher intercept voltage (V_{bi}) values due to the high doping donor atoms and native/deposited interfacial layer.

When analyzed concerning the applied frequency ($\omega = 2\Pi f$), Nicollian and Brews introduced the equivalent admittance characterized by the parallel capacitance (C_m) and conductance (G_m/ω) as defined in Eq. 12 [23, 24];

$$\mathrm{Y} = G_m + \mathrm{j}\omega C_m \tag{12}$$

The C_m and G_m/ω results of Device B corresponding to the accumulation, depletion, and inversion regions are illustrated in Fig. 6a and b. The C_m and G_m/ω values demonstrate a gradual decrease towards the strong inversion region, while they indicate an increase in the strong accumulation region with increasing voltage.

As the frequency increases, the peaks of C_m and G_m/ω values diminish within the robust accumulation zone and relocate towards the area of accumulation. By employing the capacitance and conductance measured in the robust accumulation area, defined as C_{ma} and G_{ma}, the series resistance (R_s) can be computed using the subsequent equation [23]:

$$R_S = \frac{G_{\mathrm{ma}}}{[G_{ma}^2 + \omega^2 {C_{ma}}^2]} \tag{13}$$

where when C_{ox} is represented as follows when $C_{\mathrm{ma}} = C_{\mathrm{ox}}/(1+\omega^2R_s^2C_{ox}^2)$ is substituted within Eq. 13:

$$C_{ox} = C_{ma}\left[1+\left(\frac{G_{\mathrm{ma}}}{\omega C_{ma}}\right)^2\right] = \frac{\varepsilon_i\varepsilon_oA}{\delta} \tag{14}$$

where $\varepsilon_i = 11.8\varepsilon_o$ and $\varepsilon_o = 8.85x10^{-14}F/cm$. A represents the rectifier contact area and is equivalent to $7.8539x10^{-3}cm^2$. When utilizing the second part of the equation mentioned above, the calculated layer thickness (δ) is determined to be 412 nm at 100 kHz. Additionally, the PMItz thickness measured using SEM described in Fig. 2 is in the range of 302 nm to 410 nm while the δ value calculated from Eq. 14 is in good agreement.

Utilizing Eq. 13, the R_s-V-f graph is depicted in Fig. 6c. Observationally, R_s values decrease as frequency increases in the reverse biasing region. Moreover, they demonstrate voltage independence for high frequencies. The R_s values vary in practice, contingent upon both frequency and applied voltage, owing to the distribution of interface trap state density (N_{ss}). The value of N_{ss} in the voltage range is computed in Fig. 6d. With a voltage range change from − 3 to 3 V, the N_{ss} values, in this case, change from 1.1×10^{10} to 1.98×10^{11} $\mathrm{cm^{-2}\ eV^{-1}}$. According to these findings, N_{ss} is located between the metal/*p*-PMItz and *p*-PMITz/*n*-type Si in two distinct zones.

Dielectric properties are crucial in electronic devices based on capacitors and transistors. Hence, the dielectric constant $\varepsilon\prime$, dielectric loss ε'', loss angle $tan\delta$, *a.c.* electrical conductivity σ_{ac}, and magnitudes of the real and imaginary parts $M\prime$ and M'' of the complex electric module can be determined using the C_m and G_m/ω outputs. Relative dielectric permittivity (ε^*), representing the interaction between the electric field and the material in a complex form, is expressed as follows [25, 26]:

$$\varepsilon^* = \varepsilon\prime - i\varepsilon'' \tag{15}$$

where $\varepsilon\prime$ and ε'' also denote the stored and expended energy, respectively. The real part ($\varepsilon\prime$) of ε^*, in a wide range of frequencies in the strong accumulation area ($V_G > 0$) can be calculated using the following equation [24–26]:

$$\varepsilon\prime = \frac{C_m}{C_o} = \frac{C_m d}{\varepsilon_0 A} \tag{16}$$

where C_o represents the capacitance magnitude of an empty capacitor and is determined by $C_o = \varepsilon_o\,(\frac{A}{d})$. In this equation, A denotes the area of the rectifier contact, and d represents the organic layer's thickness, which equals 412 nm. The imaginary part (ε'') of the complex form, depicting dielectric dissipation related to energy dissipation, is established through conductivity measurements. Dielectric dissipation peaks when $\omega = \frac{1}{\tau}$ and must be minimized for thin film layers, significantly influencing device performance. The expression for dielectric dissipation ε'' is given as follows [25, 26]:

$$\varepsilon'' = \frac{G_m d}{\omega \varepsilon_0 A} = \frac{G_m}{\omega C_0} \tag{17}$$

where G_m represents the conductivity of the structure and ω is the angular velocity. By utilizing the imaginary (ε'') and real ($\varepsilon\prime$) parts of the permittivity, the loss angle $tan\delta$ values can be calculated as follows [30]:

$$tan\delta = \frac{\varepsilon''}{\varepsilon\prime} \tag{18}$$

Figure 7 illustrates the characteristics of ε′, ε″, and tan δ of the heterojunction structure as a function of frequency within the voltage range of − 3 V to + 3 V. In Fig. 7a, the ε′ values in the accumulation region increase with decreasing frequency up to 10 kHz. Additionally, a little change is observed in $\varepsilon\prime$ values at the inversion region. These increments are attributed to N_{ss} surface and dipole polarizations at low frequencies up to 10 kHz, while they are caused by the R_s at higher frequencies [27]. C_m and G_m/ω characteristics are measured at different frequencies.

The ε'' values in Fig. 7b show a comparable peak for low frequencies ($f \leq 10$ kHz) in the depletion region, peaking approximately 0.5 V. The limited number of majority carriers positioned between the bandgap change from reverse bias voltage to forward bias voltage is the cause of this phenomenon. N_{ss} and interface polarization are responsible for such peak behaviors at low frequencies in the inversion and depletion regions of the ε'–V and ε''–V parameters [26].

In the forward bias region of Figure 7c, the loss tangent (tanδ) value increases up to 1000 kHz, while in the reverse bias region, there is little change. On the other hand, the peak values that are observed first rise and then fall at 10 kHz. The aforementioned phenomena can be explained by the produced device's capacitance and conductance values being

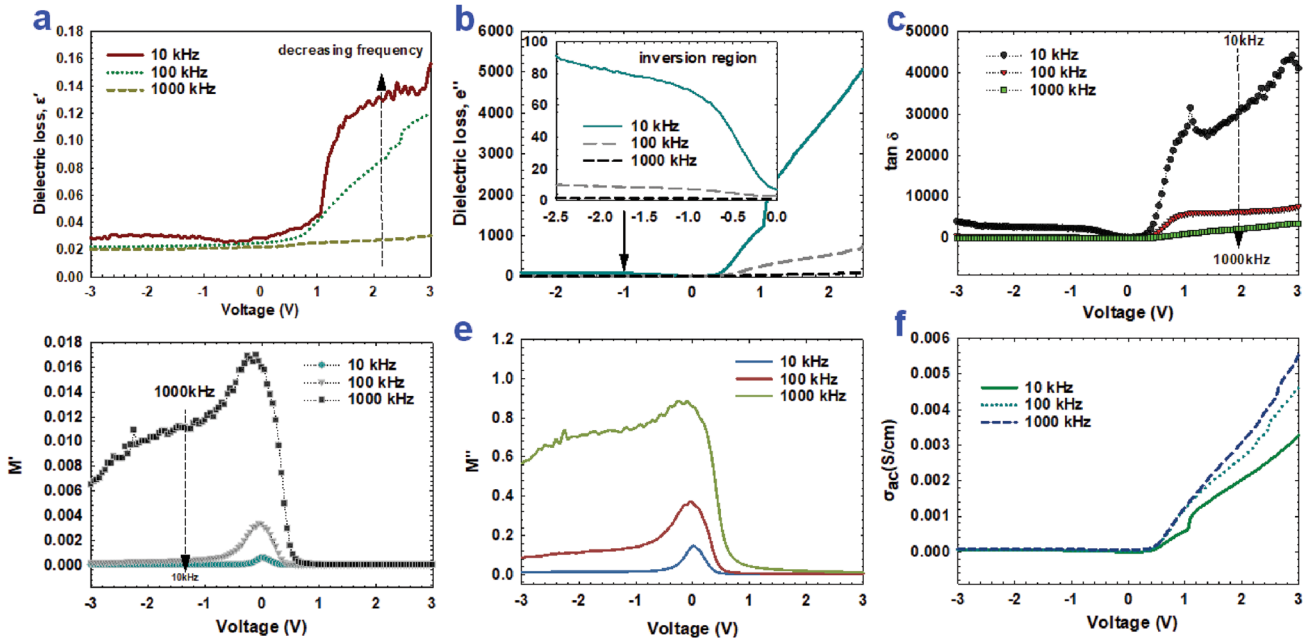

Fig. 7 The $\varepsilon\prime$ (**a**), ε'' (**b**), tan δ (**c**), M' (**d**) and M'' (**e**) and σ_{ac} (**f**) characteristics by using voltage dependent for the Device B, at distinct frequencies

sensitive to the series resistance and interface quality [26].

Based on ε^*, the components of the complex electric modulus (M^*) are divided into real (M') and imaginary (M'') components as follows [28]:

$$M^* = \frac{1}{\varepsilon^*} = M' + jM'' = \frac{\varepsilon'}{(\varepsilon')^2 + (\varepsilon'')^2} + j\frac{\varepsilon''}{(\varepsilon')^2 + (\varepsilon'')^2} \quad (19)$$

The voltage-dependent M' and M'' values at the wide-ranged frequency are computed and expressed in Fig. 7d and e using Eq. 19. It is evident that frequency substantially impacts the M' and M'' values in this case. Furthermore, M'' values exhibit a peak in the depletion region and a maximum value as the frequency increases.

The *a.c.* electrical conductivity (σ_{ac}) of organic layer is a vital parameter providing insights into the material properties and is determined using the following equation [29]:

$$\sigma_{ac} = \varepsilon'' \omega \varepsilon_0 \quad (20)$$

As frequency increases, Fig. 7f clearly shows an increase in σ_{ac}. This increase is thought to be caused by the polarization decreasing with frequency. More carriers contribute as polarization decreases, which increases a.c. conductivity and decreases polarization, increasing σ_{ac}. It is noticed that σ_{ac} is voltage-independent at low frequencies and changes voltage dependently at high frequencies.

Using the organic layers in heterojuncions, the electronic characteristics of vertical diodes are developed by evaluating the dielectric characteristics in detail. Therefore, considerable research has been done on the performance of dielectric characteristics in the literature. Table 3 presents Device B's maximum dielectric constant $\varepsilon max'$ values based on *p*-PMItz/*n*-Si. Notably, the dielectric constant ε_{max}' value of the *p*-PMItz thin film is 0.16 at 10 kHz.

Table 3 The C_o, C_{ox}, ε_{max}' and δ values of Device B

f (kHz)	10	100	1000
C_o(F) at 3 V	1.69×10^{-09}	1.69×10^{-09}	1.69×10^{-09}
C_{ox}(F) at 3 V	2.64×10^{-10}	1.99×10^{-10}	5.1×10^{-11}
ε'_{max}	0.16	0.12	0.03
δ		412 nm	

3.3 Energy band diagram

Schematic energy band diagram models of *p*-*n* and *p*-*i*-*n* vertical devices employing diverse heterojunction configurations are presented in Fig. 8. The diodes are fabricated utilizing *p*-PMItz as the organic semiconductor layer interfacing with different inorganic substrates, including *n*-Si (*n*-type silicon), *n*-4HSiC (*n*-type 4H silicon carbide), and incorporating an intrinsic SiO_2 (silicon dioxide) layer in the *p*-PMItz/*i*-SiO_2/n^{++}-Si configuration. Here, the device's band alignment, interlayer, and Fermi level energy are demonstrated. In previous study, the fabricated devices have a bandgap of 3.02 eV (E_g) [16]. It is shown from the band diagram that the devices are electron–hole pairs. Electrons in the conduction band and holes in the valence band are shown. This has the potential to create a flow of electrons and holes. Thus, bias was created by transporting electrons with this flow.

4 Conclusion

In conclusion, our comparative study of *p*-*n* and *p*-*i*-*n* vertical diodes utilizing different heterostructure configurations based on *p*-PMItz/*n*-Si, *p*-PMItz/*n*-4HSiC, and *p*-PMItz/*i*-SiO_2/n^{++}-Si sheds light on the intricacies of organic–inorganic heterojunction devices under dark conditions. Through comprehensive analysis of *I*-*V* and dielectric characteristics, we have elucidated the distinct performance attributes arising from variations in heterojunction interfaces and band alignments. We observed unique trends in device characteristics for *p*-*n* and *p*-*i*-*n* diodes, indicative of different charge transport mechanisms governed by the specific heterojunction configurations. The incorporation of an intrinsic SiO_2 layer in the *p*-PMItz/*i*-SiO_2/n^{++}-Si configuration introduces additional complexity but offers intriguing possibilities for tailoring device properties. These findings contribute to advancing our understanding of organic–inorganic heterojunction devices and provide valuable insights for optimizing their performance in vertical diode applications. Future research directions may support further refinement of heterojunction design, investigation of device stability under various operating conditions, and exploration of novel materials and architectures to harness the full potential of organic–inorganic hybrid diodes.

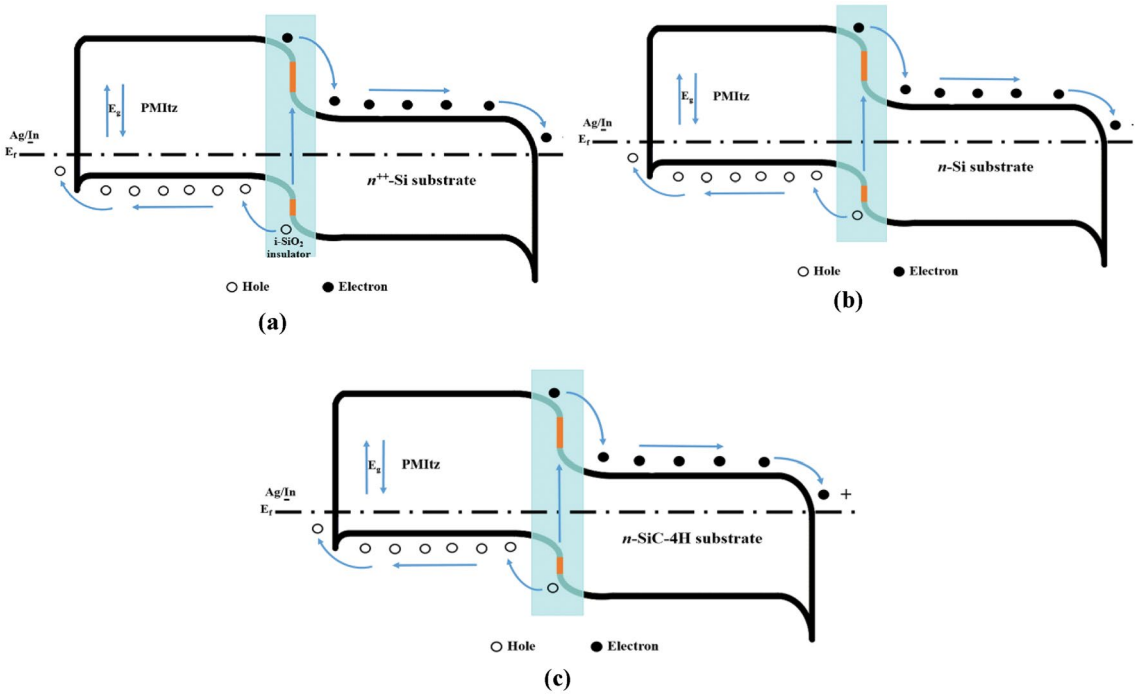

Fig. 8 Schematic energy band diagram models of the *p*-PMItz/*i*-SiO_2/n^{++}-Si (**a**), *p*-PMItz/*n*-Si (**b**) and *p*-PMItz/*n*-4HSiC (**c**) fabricated devices

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Author contributions

AAA is involved in writing original drafts, validation, formal analysis, and conceptualization. OC is involved in writing, review and editing, supervision, methodology, investigation, formal analysis, and conceptualization.HM is involved in data curation and analysis. FÜ involved in samples preparation. MZ is involved in material synthesis, and PMItz film formation. ŞA involved in final manuscript checking and supervision.

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Data availability

The data supporting this study's findings is available from the corresponding author upon reasonable request.

Declarations

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