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A comparison electrical characteristics of the Au/(pure-PVA)/n-Si and Au/(CdTe doped-PVA)/n-Si (MPS) type Schottky structures using *I–V* and *C–V* measurements

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ABSTRACT

In this study, both the Au/(pure-PVA)/n-Si (MPS-1) and Au/(CdTe:PVA)/n-Si (MPS-2) type Schottky diodes (SDs) were fabricated onto the same n-Si wafer in same conditions. After that, their electrical parameters were obtained from the current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements and compared to each other to determine the effect (CdTe:PVA) interlayer on the performance of MPS type SD. The saturation current (I_s), ideality factor (n), rectification ratio (RR = $I_{for.}/I_{rev.}$), zero-bias barrier height (Φ_{Bo}), and series/shunt resistances (R_s, R_{sh}) were derived utilizing *I–V* data. The values of I_o, n, and Φ_{Bo} were found as 9.13×10^{-7} A, 11.07, 0.63 eV for MPS1 and 1.54×10^{-10} A, 3.97, 0.85 eV for MPS2, respectively. The C^{-2}–V graphs were drawn for 0.7 MHz to obtain the doping concentration of donor atoms (N_D), Fermi energy (E_F), BH/($\Phi_B(C–V)$), depletion layer width (W_D), and maximum electric field (E_m). The $N_{ss} - (E_c - E_{ss})$ profile for two SDs was produced from the *I–V* data by considering the voltage dependence of n and BH. The values of surface states (N_{ss}) were changed between 4.8×10^{13} and 1.7×10^{14} eV^{-1} cm^{-2} for MPS1 and 5×10^{12} and 1.15×10^{13} eV^{-1} cm^{-2} for MPS2, respectively. All experimental results show that the (CdTe:PVA) interlayer significantly improved the quality of the MS type SDs rather than (pure-PVA) in terms of lower values of leakage/saturation current, n, N_{ss}, and higher RR, BH, and R_{sh} when compared (pure-PVA) interlayer. The (CdTe:PVA) interlayer may be used instead of the conventional interlayer in the future.

1 Introduction

The work function of metals that are used as back and rectifier contacts, and the semiconductor, according to Schottky–Mott theory, determines the ohmic and/or rectifying behavior of metal–semiconductor (MS) and metal-interlayer-semiconductor MIS-type SDs devices [1–7]. For instance, to make an-ohmic contact onto an n-Si wafer, the work function of metal (Φ_m) must be lower than that of semiconductor (Φ_s), but to make a

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rectifier or Schottky contact, Φ_m must be higher than Φ_s. However, with *p*-type Si or a semiconductor, the situation is completely opposite. Today, the primary scientific/technological challenge in MIS-type SDs is increasing their performance while lowering production costs by employing various acceptable high-dielectric pure or metal/metal-oxide doped polymer layers [1, 2, 7–13]. A polymer interlayer is typically inexpensive, flexible, and can be easy to grow, with excellent mechanical/dynamic strength. However, it has low conductivity/dielectric values, but they may be improved by doping them with a low fraction of some metal or metal-oxide and graphene [8–13]. Apart from this, several studies have been conducted on the electrical properties of nanocomposite structures formed by doping organic or inorganic nanoparticles [14–17]. These structures can have various effects on their own properties and on the properties of semiconductor devices when used as interlayers in heterostructures [18]. Because both the N_{ss} and R_s are more effective on both the electrical features, they must be considered in the computations. Surface states may arise during the cleaning surface of the semiconductor and fabrication process, which include some unsaturated dangling bonds, oxygen vacancies, atom-like bonds, and dislocations at the junction of interlayer/semiconductor interface in the semiconductor bandgap (E_g) [1–5, 19–22]. These states/traps can collect or release an increasing number of electrons, acting as recombination centers. Series resistance, on the other hand, can be generated by the semiconductor's back and rectifier contacts, its bulk resistance, and highly and non-uniformly doped donor/acceptor atoms. Shunt resistance is typically caused by leakage-current channels along the interfacial layer, shunt patches from the probe wire to the rectifier contact, and ground [3–5].

In our previous study [23], we aimed to produce Au/(CdTe:PVA)/n-Si (MPS) type structures instead of conventional MIS structures, and their electrical parameters were obtained depending on frequency and voltage between 1 and 700 kHz. The voltage-dependent profiles of N_{ss} and their lifetimes (t) were also obtained from the parallel conductance method. Almost all electrical parameters were found to have strong functions of frequency and voltage. More information on the frequency and voltage-dependent basic electric parameters can be found in our previous study [23]. Herein, the influence of the interfacial polymer layer on the electrical properties of Au-PVA-*n*Si (MPS1) and Au-(CdTe:PVA)-*n*Si (MPS2) type SDs was investigated in this study. The *I*–*V* and *C*–*V* measurements were performed in a wide range of voltages to achieve this goal. When compared to pure PVA interlayer, the MPS type SD performs well with low I_o or leakage current, n, surface states (N_{ss}), and higher BH, R_{sh}. The BH value was determined to be 0.85 eV for MS with pure PVA and 0.59 eV for (CdTe:PVA) interlayer, indicating that this second interlayer plays a key role in modifying the BH.

2 Experimental procedures

The ($Cd(CH_3COO)_2$) and (Na_2TeO_3) precursors have 99% purity were supplied from Merck-company to prepare CdTe-nanostructures. Firstly, 0.2 M (20-cc) of Na_2TeO_3 and ($Cd(CH_3COO)_2$) and 2 M of NaOH solutions were prepared separately in the deionized water (DW) then combined under-stirring and then it was irradiated by ultrasonic waves at 100 Watt during 15 min. After that, it was cleaned and filtered and finally annealed at about 40 °C for 45 h. Both the MPS1 and MPS2 type SDs were fabricated onto the same *n*-Si substrate with (100) float zone, 280 μm thickness, and 5 Ω cm resistivity. Secondly, the wafer was cleaned with acetone, methanol, H_2O_2, NH_4OH, and HF solutions in an ultrasonic bath to remove the native SiO_2 and dried with N_2 gas. Secondly, the high purity (99.999%) metal (Al) was thermally grown onto the whole back side of the wafer at 1 μTorr and sintered at 500 °C for 5 min to obtain good ohmic contact. The (CdTe-PVA) was prepared by dispersing 10 mg of CdTe-nanostructure in 5 ml of (5% PVA) polymer, and then it was performed on the front of *n*-Si substrate by spin/coating technique. In the last step, Au (99.999%) contact was grown wafer to prepare MPS-1 and MPS-2 at 10^{-6} Torr. The *I*–*V* and *C*–*V* measurements were carried out by use of a Keithley 2400 source meter and HP4192-A impedance meter, respectively. The fabricated schematic diagram of the Au/n-Si with pure and (CdTe:PVA) interfacial layer and measurement system is given in Fig. 1.

3 Results and discussion

The initial analysis findings were acquired for the produced CdTe powder material using X-ray diffraction (XRD) patterns with two new samples. In Fig. 2a, the XRD representation of CdTe powder is demonstrated.

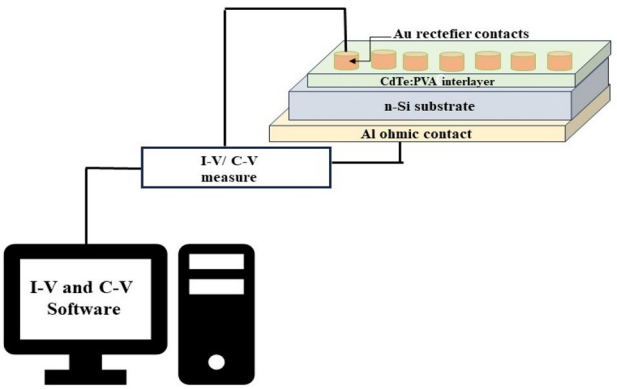

Fig. 1 The schematic diagram of the Au/(CdTe:PVA)/*n*-Si SDs and measurement system

The XRD examination disclosed that the polycrystalline zinc-blende structure aligns with peak positions at $2\theta = 23.80°$, 39.40°, and 46.50°, corresponding to orientations (111), (220), and (311), respectively (based on JCPDS Data File: 75-2086-cubic). The XRD pattern affirms the creation of pure CdTe semiconductor crystal powder free from any impurities. The XRD model, validating the purity of crystalline CdTe materials, presents distinct and uncontaminated peaks with no shifts. In Fig. 2b, the field emission scanning electron microscopy image provides a detailed visualization of the cadmium telluride (CdTe) nanostructures. The image illustrates the arrangement of the nanostructures in a distinct sheet-like configuration. The observed polydisperse nature of the nanostructures' thickness, which ranges between 50 to 500 nm, underscores the heterogeneous nature of the CdTe

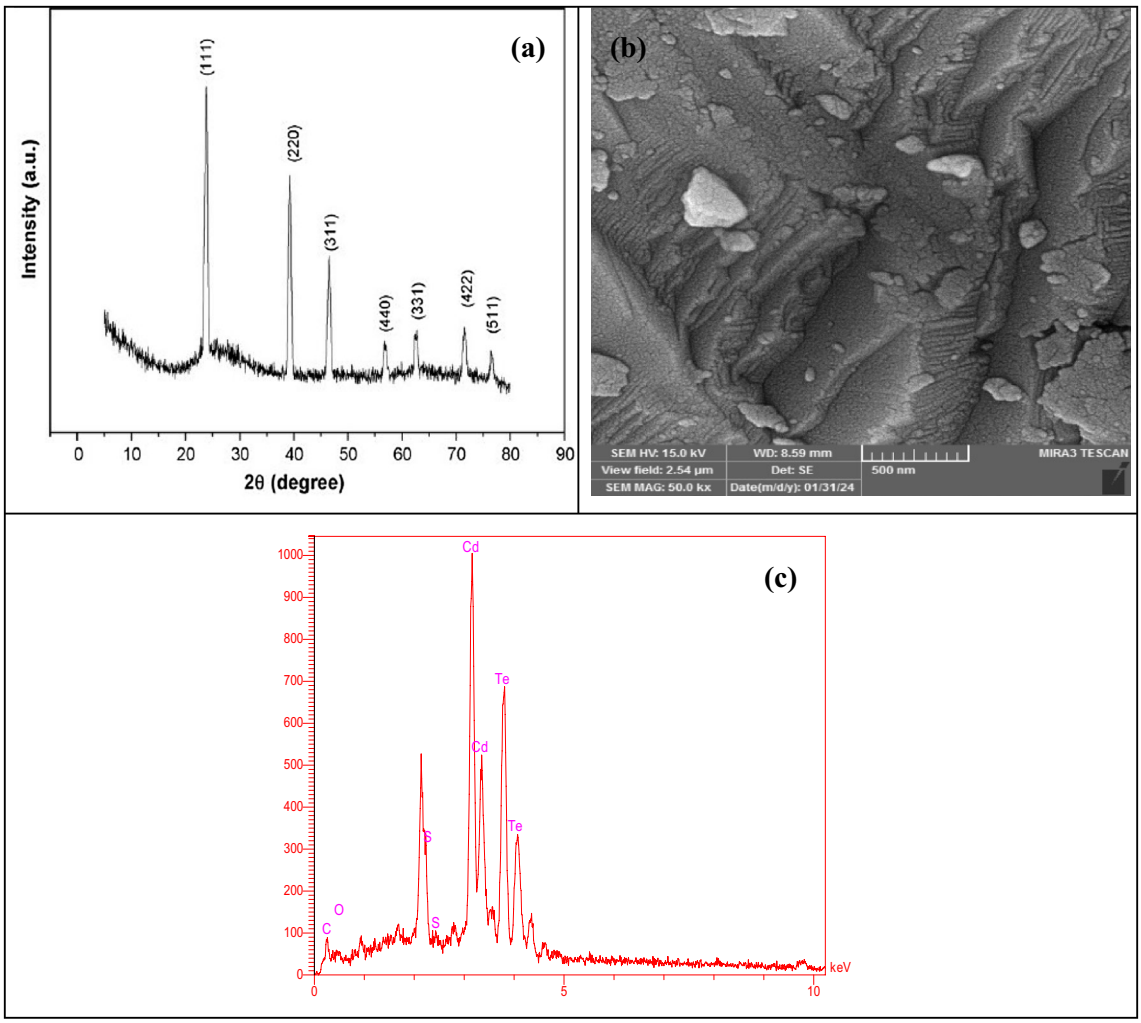

Fig. 2 **a** XRD pattern of the CdTe nanostructure, **b** Field Emission Scanning Electron Microscope (FE-SEM) image, and **c** EDX analysis of the CdTe nanostructure

nanostructures. The results of the EDX analysis are presented in Fig. 2c, indicating the outcomes obtained from the energy dispersive spectroscopy analysis. The results demonstrate that the composition of CdTe is relatively stoichiometric with a weight percentage and atomic ratio of approximately 1:1. This finding provides valuable insights into the proximity and stoichiometric composition of CdTe, as revealed by the EDX method.

3.1 The current–voltage characteristics

The ln(*I*)–*V* curves of the constructed pure-PVA and (CdTe: PVA) interlayers at room temperature are shown in Fig. 3. These charts clearly show a decent linear regime for modest bias voltage, but they start to deviate from linearity due to the presence of R_s and the interfacial-layer. When the voltage is more than $3kT/q$, the essential electrical properties of these SDs can be derived from their linear region using TE theory as follows [1, 2, 4–6, 24–27].

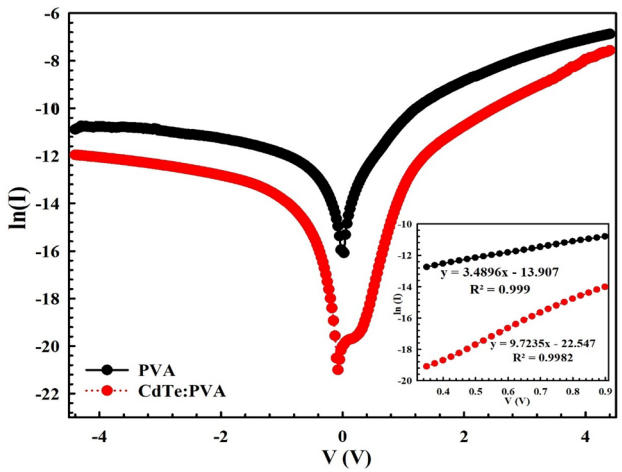

Fig. 3 The semi-logarithmic *I*–*V* plot of the MPS1 and MPS2 type SDs

$$I(V) = \left(AA^*T^2\right)\exp\left(-\frac{qe\Phi_{B0}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \cong I_0\exp\left(-\frac{q\Phi_{B0}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)\right] \quad (1)$$

The q and k constants are well known in the literature, whereas A, A^*, Φ_{Bo}, and n is the SD area (=7.8510^{-3} cm^2), Richardson-constant (which theoretically takes 112 A/(cm K)^2 for n-Si), zero bias BH, and ideality factor, respectively. Using the following relationships [1, 4–6], we can derive values of I_o, n, and Φ_{Bo} from the slope and intercept point at zero-bias voltage by evaluating the linear regime of ln(*I*)–*V* curves based on Eq. 1 [1, 2].

$$n(V) = \frac{qV_i}{kT\left(d\ln I_i/dV_i\right)} = 1 + \frac{d_i}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (2)$$

$$\Phi_{B0} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_o}\right) \quad (3)$$

Table 1 also includes the I_o, n, and Φ_{Bo} values obtained for two separate samples. As shown in Table 1, the existence of N_{ss}, tunneling via these traps and patches/lower barriers, image force lowering in BH, and generation and recombination (GR) currents can all explain the obtained greater value of n for two SDs.

The voltage-dependent resistance (R_i) profile of the MPS1/MPS2 type SDs was derived from Ohm's-Law and is shown in Fig. 4. As demonstrated in this figure, the value of R_i becomes essentially constant at adequately higher forward voltages and sufficiently lower reverse voltages, corresponds to the true values of R_s (=4.11 kΩ) and R_{sh} (=0.25 MΩ) for MPS1 and 1.17 k and 0.63 MΩ for MPS2 SD, respectively. As can be seen in Table 1, the value of I_o for MPS2 SD is 1.69×10^{-4} times lower than for MPS1 SD, and the value of n is similarly 2.79 times lower than for MPS1, indicating that the MPS2 SD performs well. The higher values of R_s can be rooted in the formation of back ohmic and front-rectifier/Schottky contacts, the use of wireless to get electric contact, the bulk resistivity of the semiconductor, and some impurities or dislocations on the surface of the semiconductor. On the other hand, the

Table 1 Basic electrical parameters of the MPS1and MPS2 SDs obtained from the *I*–*V* data

Sample	I_o (A)	n	Φ_{B0} (eV)	R_s (Ω)	R_{sh} (Ω)	RR (±4.5 V)
Au/PVA/n-Si (MPS1)	9.13×10^{-7}	11.07	0.63	4.11×10^3	2.54×10^5	75.11
Au/(CdTe:PVA)/n-Si (MPS2)	1.54×10^{-10}	3.97	0.85	1.17×10^4	6.30×10^5	78.74

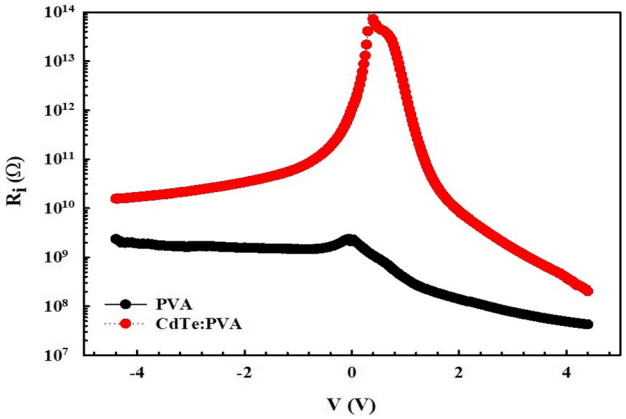

Fig. 4 The R_i–V plots of the MPS1 and MPS2 type SDs obtained from Ohm's law

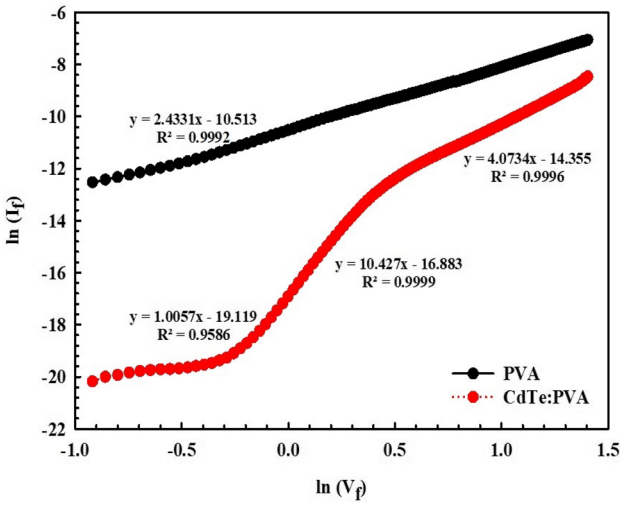

Fig. 5 The ln (I_f) – ln(V_f) curves of the MPS1 and MPS2 type SDs

obtained higher value of n both for MPS1 and MPS2 SD can be explained by the existence of the interfacial layer at Au/n-Si, N_{ss}, and depletion layer width (W_D) as seen in Eq. 2. The other reason for the higher values of n can be explained the Gaussian distribution of barrier height at MS interface and generation-recombination current [1, 5, 7]. According to Tung [6], barrier height at the M/S interface may include many patches or lower barriers at around mean BH. In this case, electrons that do not have enough energy to pass through the average barrier can be easily passed through these patches or lower barriers, leading to an increase in the current or n.

The forward bias ln (I_f)–V_f plots for MPS1 and MPS2 type SDs were made to examine whether the doping concentration of the interlayers impacts the charge-transport mechanisms (CTMs). As shown in Fig. 5, while this plot has one linear part with a slope of 2.43 for the MPS1 SD, it has three linear regimes with different slopes for the MPS2 SD, which are referred to as (region-I for low bias voltages), (region-II for intermediate bias voltages), and (region III for high bias voltages), respectively, due to current variations with applied bias voltage being proportional as $I \propto V^m$ [2, 22]. The values of these three linear sections for MPS2 SD were found to be 1.01, 10.43, and 4.07, respectively. In the CTM, however, Ohmic behavior dominates for MPS2 type SD. Trap charge limited current (TCLC) dominates both regimes 1 and 2, respectively, in region-1. In general, Ohm's law or behavior tends to be more effective when the slope is closer to unity, SCLC is effective when the slope is almost 2, and TCLC is effective when the slope is greater than 2 [22]. In other words, as the slope (m) value approaches 2, the SD approaches the "trap-filled" limit rather than the ohmic limit, and so many much-electrons may escape from the energy states, contributing to the space–charge limited current (SCLC) [2, 22, 23]. But, when the value of m exceeds two, it shows that CTM is governed by the (TCLC). Based on such a mechanism, increasing the level of injection electrons causes traps/defects to fill and the space charge to rise [22, 23].

The existence of N_{ss} and an interlayer can alter the I_f–V_f characteristics. According to Card and Rhoderick [5], when the thickness of this layer is greater than 3 nm, the value of n becomes higher than unity for SDs with N_{ss} are equilibrium by semiconductor. The distribution of $N_{ss} - (E_c - E_{ss})$ in the MS/MIS-type SDs is reckoned with voltage-dependent ($n(V)$) and effective BH (Φ_e) using the I_f–V_f data to determine the influence of different doping levels in interlayers. The following formulas derived by Card and Rhoderick [5, 12, 22] can be utilized to calculate voltage-dependent profiles of the n and BH.

$$N_{ss}(V) = \frac{\varepsilon_0}{q}\left[\frac{\varepsilon_i}{d_i}\left(n(V_i) - 1\right) - \frac{\varepsilon_s}{W_D}\right] \quad (4)$$

In this equation, ε_s and ε_i are the permittivity of the semiconductor and interlayer, respectively, whereas d_i and W_D represent the thickness of the interlayer and depletion layer [1–4]. On the bottom of the conduction band (E_c) for an n-Si, the energy level of these states (E_{ss}) was derived using the following relationships [1, 3, 5]:

$$\Phi_e(V) = \Phi_{B0} + \left(1 - \frac{1}{n(V)}\right)V \tag{5a}$$

$$q\left(E_c - E_{ss}\right) = \left(\Phi_e - V\right) \tag{5b}$$

Thus, the N_{ss} vs $(E_c - E_{ss})$ curves of the MPS1 and MPS2 SDs were determined from the I_f-V_f data by accounting for both the voltage dependence of n and Φ_e(V) using Eqs. 2, 4, and 5a, 5b and is shown in Fig. 6. As shown on Fig. 6, the energy dependent-profile of N_{ss} has a ''U'' shape because to peculiar behavior of them in the Si bandgap. Because of the passivation impact of surface states, the N_{ss} values for MPS2 are 10 times lower than for MPS1 [10, 12, 27–33].

3.2 Capacitance–Voltage (*C-V*) characteristics

The following relationship [2] describes the relationship between reverse bias voltage (V_R) and capacitance per unit area.

$$C^{-2} = \frac{2\left(V_o + V_R\right)}{q\varepsilon_s\varepsilon_o A^2 N_D} \tag{6}$$

The terms V_o and N_D in Eq. 6 represent the intercept-voltage of the C^{-2} vs V curve, respectively. The voltage-dependent C–V curve of the MPS1 and MPS2 type SDs are shown in Fig. 7. Behavior of the curves is similar to the MOS capacitor, has three regimes between − 5 V and 0 V (inversion), 0 V and 1.2 V (depletion), 1.2 V and 5 V (accumulation). As seen in Fig. 8, the C^{-2} vs V curve displays strong linear behavior in the inversion area over a large voltage range. As a result, basic electronic parameters of MPS1 and MPS2 type SDs, such as diffusion potential (V_D), Fermi energy level (E_F), maximum electric field (E_m) at the junction, W_D, and ($\Phi_B(C–V)$) were extracted from the intercepts and slopes of the C^{-2} vs V plots and are tabulated in Table 2. [1, 4, 10, 34–41].

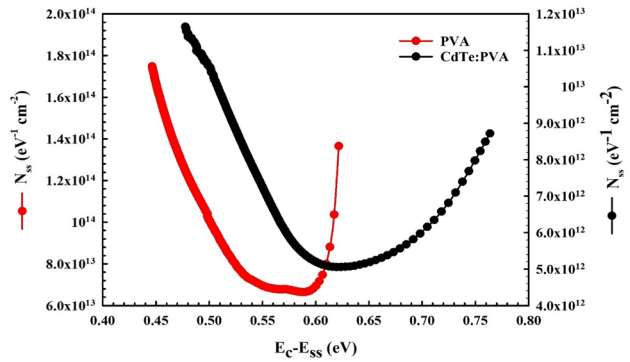

Fig.6 The N_{ss} vs $(E_c - E_{ss})$ profiles of the MPS1 and MPS2 SDs

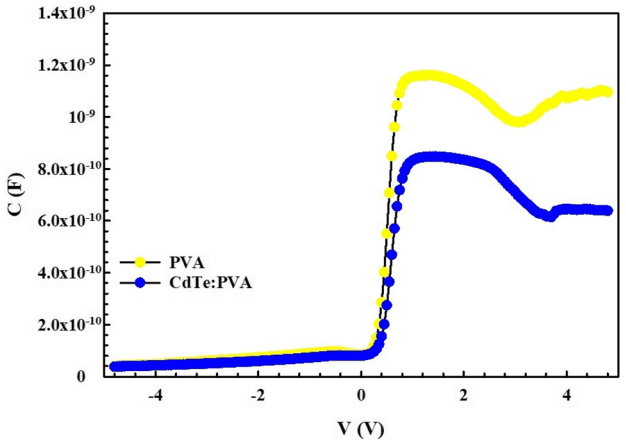

Fig. 7 The *C–V* curves of the MPS1 and MPS2 type SDs

$$V_D = V_0 + \frac{kT}{q} \tag{7a}$$

$$E_F = \left(\frac{kT}{q}\right)\ln\left(\frac{N_C}{N_D}\right) \tag{7b}$$

$$E_m = \left[\frac{2qN_D V_0}{\varepsilon_s\varepsilon_0}\right]^{1/2} \tag{7c}$$

$$W_D = \left[\frac{2\varepsilon_s\varepsilon_0 V_D}{qN_D}\right]^{1/2} \tag{7d}$$

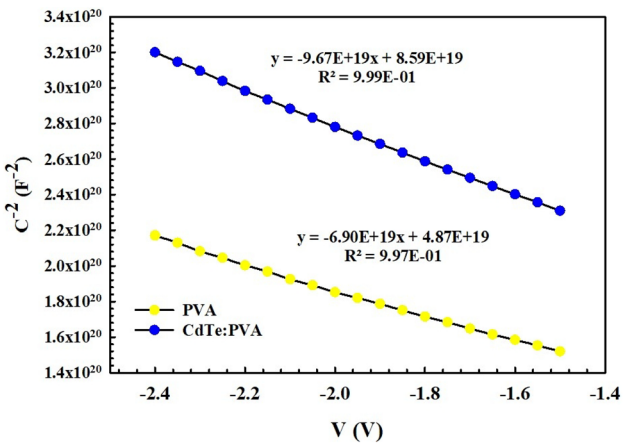

Fig. 8 The C^{-2} vs V curves of the MPS1 and MPS2 SDs

Table 2 Some electrical parameters obtained from the C^{-2} vs V plot at 700 kHz

Sample	V_o (V)	V_D (eV)	N_D (cm^{-3})	E_F (eV)	E_m (Vcm^{-1})	W_D (μm)	$\Delta\Phi$ (meV)	Φ_B (eV)
MPS1	0.706	0.731	2.82×10^{15}	0.230	6.60×10^{4}	58.1×10^{-5}	28.5	0.960
MPS2	0.888	0.913	2.01×10^{15}	0.239	6.30×10^{4}	77.0×10^{-5}	27.7	1.150

$$\Phi_B = V_{D0} + \frac{kT}{q} + E_F - \Delta\Phi_B = V_D + E_F - \Delta\Phi_B \quad (7e)$$

As shown in Table 2, the BH obtained from the reverse bias C^{-2} vs V curve at 700 kHz for two types of SDs is much higher than the obtained from the ln (I_f) vs V_f plot because of the nature of the measuring technique and the voltage dependency of these electrical parameters [2, 5–7]. Furthermore, as shown in Tables 1 and 2, the value of BH for MPS2 SD is greater than that for MPS1 SD. As a result, all experimental electrical parameters collected are influenced by the applied bias voltage, interfacial layer permittivity and thickness, and series resistance. In summary, it can be said that using a (CdTe:PVA) interfacial layer improves SD performance in terms of lower n, N_{ss}, I_o, and greater BH, R_{sh}, and depletion layer width. As a result, it can be utilized successfully in place of conventional insulators created using established processes.

4 Conclusion

This study examines the influence of the CdTe:PVA polymer layer on the electrical properties of both the Au-PVA-nSi/(MPS1) and Au-(CdTe:PVA)-nSi/(MPS2) interfacial polymer layers built onto the n-Si wafer. To achieve this goal, I–V and C–V measurements were taken over a wide range of voltage. The I–V measurements determined basic electrical parameters such as I_0, n, RR, BH, R_s, and R_{sh}, while the C–V measurement computed N_D, BH, W_d, and E_m. The I_0, n, and Φ_{B0} values were obtained from the forward bias LnI-V plot as 9.13×10^{-7} A, 11.07, and 0.63 eV for MPS1 and 1.54×10^{-10} A, 3.97, and 0.85 eV for MPS2, respectively. Doping concentration of donor-atoms (N_D), Fermi energy (E_F), $BH/(\Phi_B(C–V))$, depletion layer width (W_d), and maximum electric-field (E_m) were calculated from the C^{-2}–V graphs drawn for 0.7 MHz. The $N_{ss} - (E_c - E_{ss})$ profile for two SDs was produced from the I–V data by considering the voltage dependence of n and BH. The energy levels used for MPS1 and MPS2 were changed to 4.8×10^{13}–1.7×10^{14} eV^{-1} cm^{-2} and 5×10^{12}–1.15×10^{13} eV^{-1} cm^{-2}, respectively. However, all experiments showed that the use of a (CdTe:PVA) interlayer at the Au/n-Si interface significantly improved the quality of the Au/(pure-PVA)/n-Si SD. When compared to a pure PVA interlayer, the (CdTe:PVA) interlayer structure exhibited lower values of leakage current, ideality factor, and interface states, as well as greater RR, BH, and shunt resistance. The (CdTe:PVA) interfacial polymer layer can be used instead of standard insulators like SiO_2 and SnO_2 due to its low cost, simple growing and fabrication methods, high dynamic stress, and flexibility properties. The BH value was predicted to be 0.85 eV for MPS1 with pure PVA and 0.59 eV for the interfacial layer (CdTe:PVA). Therefore, the second interfacial layer is crucial in modifying the BH.

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Author contributions

All authors contributed approximately the same to the preparation of the samples and them interpretation, reviewing, writing. ÇŞG: Manufacturing, investigation, measurements, calculations, writing, reviewing and editing. MU: Investigation, measurements, calculations, reviewing and editing. ŞA: Review, editing and supervising.

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Data availability

The datasets generated and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest There are no conflicts to declare.

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