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Electrical properties of PVC:BN nanocomposite as interfacial layer in metal-semiconductor structure

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ABSTRACT

In this study, a comprehensive examination is assumed to investigate the influence of interfacial layers composed of polyvinyl chloride (PVC) and polyvinyl chloride-boron nitride (PVC: BN) on the electrical characteristics of the Au/n-Si structure. Two distinct structures, namely Au/PVC/n-Si (MPS1) and Au/PVC: BN/n-Si (MPS2), are fabricated for this purpose. The provided boron nitride (BN) nanostructures are analyzed using X-ray diffraction (XRD) patterns to determine their average crystalline size and surface morphology. Following the structural analysis, current-voltage (I–V) measurements are conducted over an extensive voltage range (± 3 V). Subsequently, the fundamental electrical properties of the developed Schottky structures are determined using various methods and compared. Experimental results indicate that the PVC: BN nanocomposite leads to an increase in the potential barrier height (BH), shunt resistance (Rsh), and rectifying rate (RR = IF/IR), while simultaneously decreasing the ideality factor (n), series resistance (Rs), and surface states density (Nss). It was discovered that the MS structure's RR was 7 times lower than that of the MPS2 structure. Moreover, the energy-dependent N_{ss} density is also derived using n(V) and $\Phi_{B0}(V)$ functions. Based on the $\ln(I_R)–V_R^{0.5}$ profile at the reverse bias region, the Schottky-emission (SE) type conduction mechanism is effective for MS structures, whereas Poole-Frenkel-emission (PFE) is effective for MPS structures.

1 Introduction

Owing to its capacity for either rectifying or non-rectifying behavior, the Schottky diode (SD), a fascinating electronic instrument in solid-state physics, is created when a metal junction is established for the semiconductor. The determining factor that affects whether an electrical current flows in a single direction is the height of the potential barrier created at the MS contact interface [1–4]. Nevertheless, the active dangling bonds on the semiconductor surface cannot be completely neutralized by employing traditional methods such as thermal oxidation or anodic oxide to grow an insulator layer between it and the metal [5–10]. As a result, many researchers have recently concentrated on improving these devices' characteristics with the use of doping metal or metal-oxide into organic/polymer interlayers rather than traditional insulators because of

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their special features such as easy-grown procedures; known as the solid-liquid phase separation, electro-spinning, and sol–gel [11–15].

The efficiency of the MS structure is thought to be improved using a high-dielectric polymer or nanocomposite in terms of an increment of the potential BH at the metal/semiconductor interface and RR, a reduction in the density of surface-states (N_{ss}) at the interface of the semiconductor and interfacial layer, and a decrease in series resistance (Rs) [16–23]. The numerous benefits of polymers, including small cost, good dielectric strength, flexibility, high capacity, adequate mechanical strength, low weight, and easy processing, lead to using them and their nanocomposites in constructing MPS structures [7, 11, 12]. The only disadvantage of pure polymers, i.e., low electric conductivity, can easily be improved by doping them with roughly 3–7% of a metal or metal oxide [13–15].

The thermoplastic polymer polyvinyl chloride (PVC) has excellent insulating qualities. PVC comes in stiff and soft varieties, with 1500–3000 MPa elastic moduli. It has a 100 °C melting point, however, with addition of a heat stabilizer, it can be heated to 260 °C. Due to its volume resistivity, dielectric constant values, and high-dielectric loss tangent, PVC is generally suitable for use in the production of insulating materials with low voltage and frequency [16]. PVC is a polar polymer, and some polar groups (such as C–Cl) will produce depolarization, resulting in increased dielectric constant. In addition, the chloride ions produced under degradation conditions will reduce its electrical insulation [17].

Boron nitride (BN) has become a particularly popular chemical because of its carbon-related properties. The properties of boron nitride in cubic form, which is extremely hard and thermally conductive, are like those of diamond. Boron nitride is a high heat and chemically resistant compound composed of boron and nitrogen, with the chemical formula BN. It is available in various crystalline structures that share electronic properties with carbon lattices. The hexagonal form, like graphite, is the most stable and relatively soft among boron nitride polymorphs. This type is commonly used as a lubricant and an additive in cosmetic and personal care products. Another variety, the cubic form known as c-BN with a zincblende or sphalerite structure such as diamond, is less hard than diamond but surpasses it in thermal and chemical durability [18]. The structure of BN nanotubes and carbon nanotubes (CNTs) is comparable. Like carbon nanotubes, BN nanotubes have unique physical characteristics but are not toxic. They possess various desirable qualities, including stability as an insulator, resistance to high-temperature oxidation, intriguing piezoelectricity, and optical features [19]. Beyond these attributes, BN nanotubes can be utilized to create an ideal insulating tubular shield for encapsulating certain materials. The unique properties of BN nanotubes will play a crucial role in advancing applications in the fields of electronics, optoelectronics, energy storage, nano-semiconductor technology, and biomedical science [20, 21].

Altindal et al. manufactured a MPS-type SD with a structure of Au/PVC:Sm_2O_3/n-Si and compared its electrical performance to an Au/n-Si (MS) diode. They discovered that the ideality factor (n) decreases from 5.85 to 2.27 and the value of Φ_{B0} rises from 0.59 to 0.84 eV providing that a thin film is placed at the metal/semiconductor interface. Additionally, the interface state densities and leakage current (I_0) decrease in MPS-type SD compared to MS type [22].

In this study, an investigation was conducted to assess whether the interfacial layers of PVC and PVC:BN enhance the performance of the MS structure. The analysis included three semiconductor devices: Au/n-Si, Au/PVC/n-Si (referred to as MPS1), and Au/PVC:BN/n-Si (referred to as MPS2) structures. Following the synthesis of BN nanoparticles, the nanocrystalline surface structure's average size was determined using XRD patterns and SEM. Electrical parameters, such as leakage current (I_0), ideality factor (n), barrier height at zero bias voltage (Φ_{B0}), series/shunt resistances (R_s, R_{sh}), rectifying rate (RR), and energy-dependent interface states density (N_{ss}), were calculated from I–V characteristic measurements for the MS, MPS1, and MPS2 structures. Finally, the current conduction mechanism in these structures was examined under reverse and forward bias voltages.

2 Experimental details

2.1 Synthesis of BN nanoparticles and preparation of PVC:BN nanocomposite

To synthesize BN nano-powder, the precursors of Boric acid (H_3BO_3), and hydrazine monohydrate ($N_2H_4H_2O$) were employed. Initially, deionized water was used to dissolve 2.5 g of H_3BO_3 and 8 g of NaN_3

with the magnetic stirring process for 30 min. The mixture was then incubated at a temperature of 300 °C for 16 h in a nitrogen-filled muffle furnace. After the incubation period was over, the mixture was rinsed with deionized water before being vacuumed for 2–3 h at a temperature of 100 °C in a vacuum pump. It is necessary to mention that the PVC:BN nanocomposite was resulted by dissolving 0.5 g of the PVC polymer powder into 99.5 ml of deionized water and then evenly dispersing 10 mg of BN nano-powder into 5 ml of the resulting solution.

2.2 The manufacturing procedure the MS and MPS structures

A one-side polished n-Si wafer with a diameter of 5.08 cm, a thickness of 300 μm, a resistivity of 1–10 Ω.cm, and a float-zone of (100) was used for the fabrication of the MS-, MPS1-, and MPS2-type SDs. Before manufacture, n-Si wafers were first washed with deionized water for about 10 min in an ultrasonic bath after being submerged in ammonium peroxide to eliminate the native oxide layer formed at two sides of the wafer. Next, it was rinsed for 3 min in a solution/mixture of acetone, ammonium hydroxide, hydrogen peroxide, hydrofluoric acid, and deionized water. After rinsing with deionized water for 10 min, the n-Si wafer was thoroughly dried using pure nitrogen gas (N_2). Subsequently, a layer of high-purity (99.99%) Au, with a thickness of 150 nm, was thermally evaporated onto the entire back side of the cleaned n-Si wafer in a high-vacuum metal-evaporation system at a pressure of 10^{-6} Torr. The wafer was then annealed in an atmosphere of N_2 gas at a temperature of 550 °C for five minutes to establish a reliable back-ohmic contact.

Circular-shaped Au rectifier contacts, with an area of 7.85×10^{-3} cm^2 and a thickness of 150 nm, were applied to a section of the n-Si wafer, which was divided into three portions to create the Au/n-Si (MS) structure (refer to Fig. 1). To produce Au/PVC/n-Si and Au/PVC:BN/n-Si MPS-type semiconductor devices (SDs) under identical conditions, similarly shaped Al rectifier contacts were thermally deposited onto the PVC polymer and PVC:BN nanocomposite layers. Thus, the fabrication process for three distinct SDs (MS, MPS1, and MPS2) was completed. Figure 2 illustrates the schematic of the constructed MPS-type SD and its corresponding energy-band diagram. It is worth noting that a KEITHLEY (Model 2450) device was utilized to measure the forward-reverse

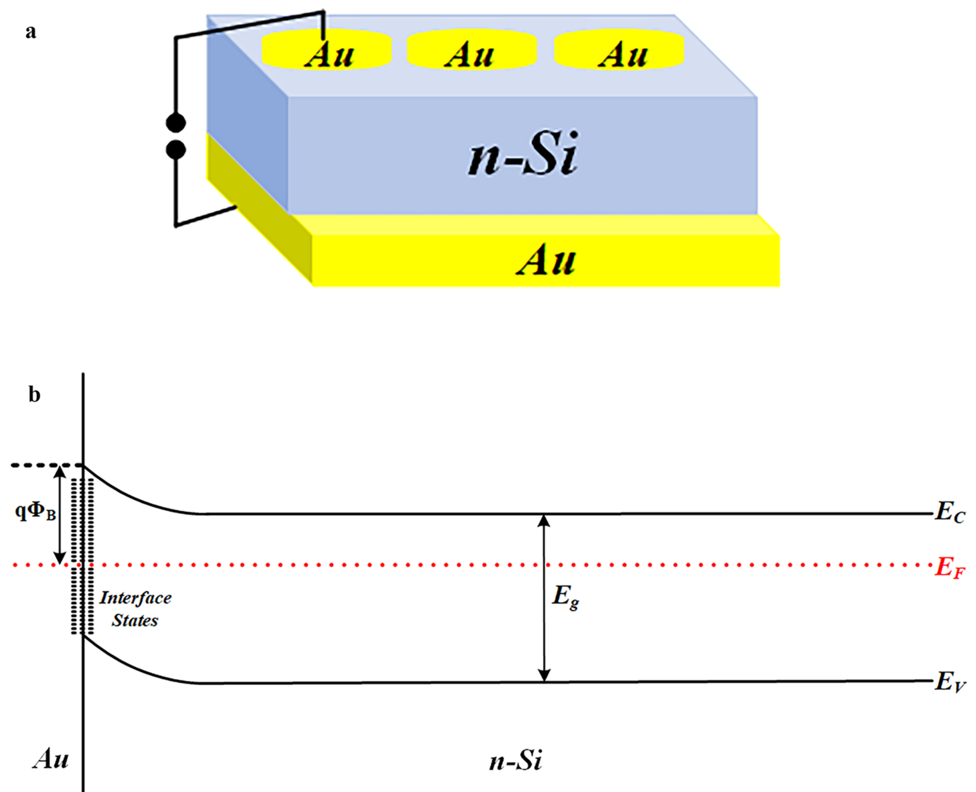

Fig. 1 **a** The schematic of the fabricated MS structure and **b** corresponding energy-band diagram

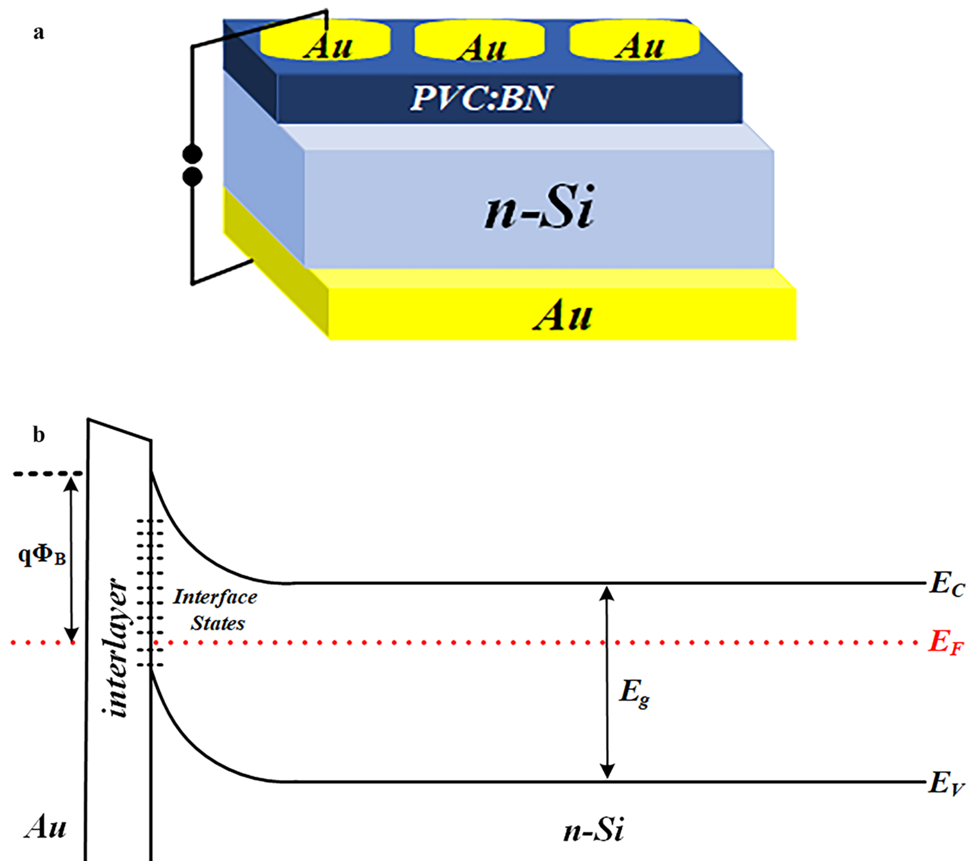

Fig. 2 **a** The schematic representation of the fabricated MPS structure and **b** corresponding energy-band diagram

I–V characteristics of each prepared sample at room temperature.

2.3 XRD analysis of BN nanostructure

The BN nanostructure was characterized using the Philips X-pert instrument with Cu kα radiation at the wavelength of 1.55 Å. Figure 3 depicts the XRD pattern of the synthesized BN nanostructure that has a largest peak at $2\theta = 26.3°$ related to the Muller index of 200. As seen, other peaks at $2\theta = 41.3°$, 43.4°, 54.6°, and 75.6° related to Muller indices of 100, 101, 004, and 110 are supported by # JCPDF card No. 73-2095 [24]. The BN nanostructures are in hexagonal phase with $a = 2.503$ Å and $c = 6.661$ Å. Additionally, the Scherrer formula can be used to determine the crystallite sizes of the BN nanostructures [25]:

$$D = \frac{0.9\lambda}{\beta cos\theta} \tag{1}$$

where θ refers to the Bragg angle, β denotes the FWHM of the highest peak in the XRD pattern, λ and D being the X-rays wavelength and the crystalline size, respectively. The crystalline size of the BN nanoparticles is computed as 35 nm.

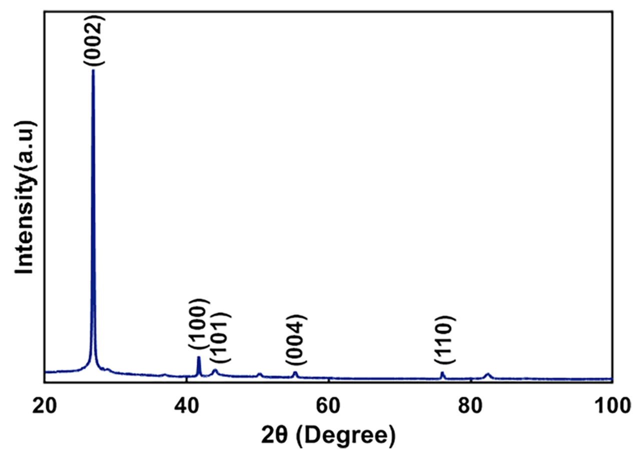

Fig. 3 XRD pattern of BN nanostructure

2.4 SEM

The SEM picture of the BN nanostructure is taken by the SEM (model LEO 1430 VP) to study the surface morphology of the prepared BN nanostructures. Figure 4 represents the SEM images of the synthesized BN nanostructure. It is obvious that the polydispersity and agglomerated BN nanoparticles, whose mean size is less than 1 μm, have been produced with various configurations.

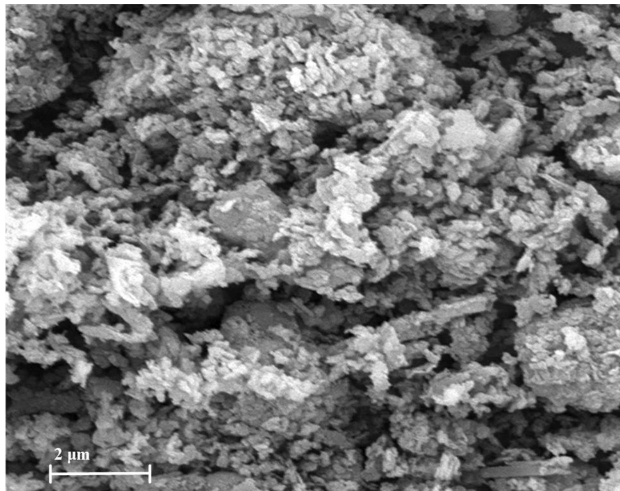

Fig. 4 SEM images of the BN nanoparticles

3 Results and discussion

In the MS- and MPS-type SDs, the transit of highly energetic electrons from the top of the potential barrier can be examined using TE theory. Given that $n > 1$ and R_s are present in MS or MPS type SDs, the relationship between forward voltage and current for $V \geq 3kT/q$ is defined as follows [26, 27]:

$$I = I_0\left[exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (2)$$

where IRs, n, and I_0 represent the voltage drop across the diode's series resistance, ideality factor, and leakage current, respectively. The semi-logarithmic representations of the $I–V$ characteristics profiles for the MS and MPS-type semiconductor devices at forward and reverse bias voltages are illustrated in Fig. 5a. Additionally, the value of I_0 is determined by utilizing the linear segment of the ln(I)-V curve at the forward bias voltage, as shown in Fig. 5b [26]. :

$$I_0 = AA^*\exp\left(-\frac{q\Phi_{B0}}{kT}\right) \quad (3)$$

with Φ_{B0} being the barrier height at $V = 0$, A^* is the impressive Richardson constant, and A is the area of the Schottky or rectifier constant. The amount of I_0 for MS-, MPS1-, and MPS2-type SD is 2.04×10^{-5} A, 1.12×10^{-6} A, and 2.05×10^{-6} A, respectively. If compared to the MS structure, the reverse-saturation

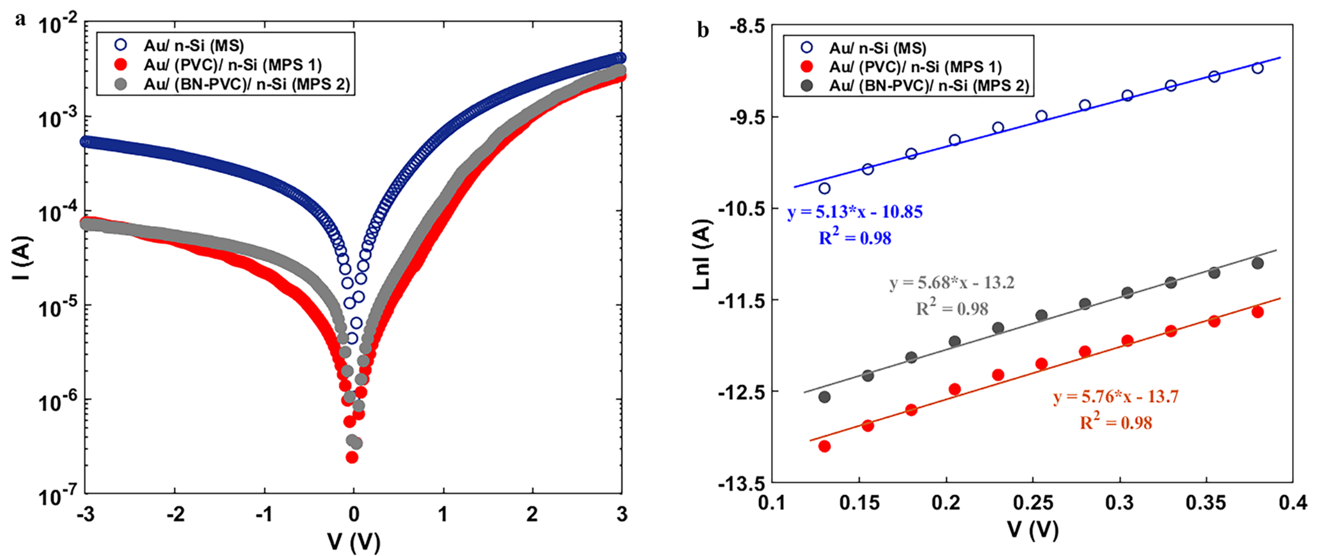

Fig. 5 **a** The semi-logarithmic curves of I–V characteristic, and **b** Ln(I)–V graphs for the prepared samples.

current of the MSP1- and MPS2-type SDs is one order smaller. Using Eq. (3), the Φ_{B0} quantity is given by [28]:

$$\Phi_{B0} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_{0}}\right) \quad (4)$$

The determined values of Φ_{B0} for the MS, MPS1, and MPS2 semiconductor devices are 0.559 eV, 0.635 eV, and 0.619 eV, respectively. Following this, the ideality factor of the manufactured structures can be derived by utilizing the slope of the linear section of the ln(I)-V curve [29]:

$$n = \frac{q}{kT}\left(\frac{dV}{d(lnI)}\right) \quad (5)$$

The computed values of n are 7.73 for MS, 6.88 for MPS1, and 7.03 for MPS2 structures. The doped polymer interlayer with high-dielectric value causes the n to diminish when the interfacial polymer layer is applied. It is necessary to note that the presence of thin films among the metal and semiconductor interface, width of the depletion layer, the inhomogeneity of the formed barrier at the interface of metal and semiconductor layers, and N_{ss} often have an impact on the ideality factor value. Moreover, several other processes including generation-recombination at 25 °C or higher, image-force reduction, and tunneling at the Schottky barrier by surface states or traps can influence the quantity of n as well as current conduction/transport mechanisms (CCMs/CTMs) [29, 30].

It is seen from Fig. 5a that these structures' rectifying behavior is good, particularly for MPS-type SDs. At the voltages of ± 3 V, the values of the rectifying ratio, defined as RR = I_F/I_R, are 11.1 for the MS, 38.4 for MPS1, and 81.9 for MPS2 structures. Comparing these values reveals that MPS-type SDs have a larger RR value than MS-type SD because PVC and the PVC:BN polymer interfacial layers have a passivated influence on N_{ss} and lowers R_s. Because of the BN nanoparticles in the PVC polymer layer, the MPS2-type SD possesses a higher RR value. Doping BN nanostructures into the PVC polymer layer, which is placed at metal/semiconductor interface, hence causes a reduction in I_0 and n as well as an increase in BH and RR values.

Additionally, the efficiency of MS- and MPS-type SDs is influenced by the series (R_s) and shunt (R_{sh}) resistances, two critical parameters [1, 23, 31, 32]. The quantity of R_{sh} is just acquired by the Ohm's law ($R_i = dV_i/dI_i$) from the I–V measurement at sufficient low reverse bias voltage but the R_s quantity could be computed using the TE, Norde, Cheung, and Nicollian-Brews procedures from the I–V data at the forward bias voltage and the C and G measurement at the accumulation region [1].

The profiles of R_i depending on the applied bias voltages for the MS-, MPS1-, MPS2-type SDs are semi-logarithmically demonstrated in Fig. 6. The real parts of R_i quantity, corresponded to the series (R_s) and shunt (R_{sh}) resistances, are practically fixed at the forward and reverse voltage biases (± 3 V), as shown in Fig. 6. Therefore, the obtained values of R_s for the MS-, MPS1-, MPS2-type SDs are 550 Ω, 825 Ω, and 556 Ω at the voltage of + 3 V, respectively. In addition, the quantities of R_{sh} at the bias voltage of -3 V are determined as 6.08 kΩ for MS, 31.6 kΩ for MPS1, and 45.5 kΩ for MPS2 structures. It is clear from comparing these numbers that the existence of the PVC:BN nanocomposite layer between the metal and semiconductor layers of the MPS_2-type SD results in improving the rectifying ratio by reducing leakage current, series resistance, and raising shunt resistance.

The following two relationships, named Cheung functions, are used to calculate the main electronic parameters (Φ_{B0}, R_s, and n) at the region of sufficiently strong forward bias voltage, which corresponds to the concave-curvature of Ln(I)-V profiles [33];

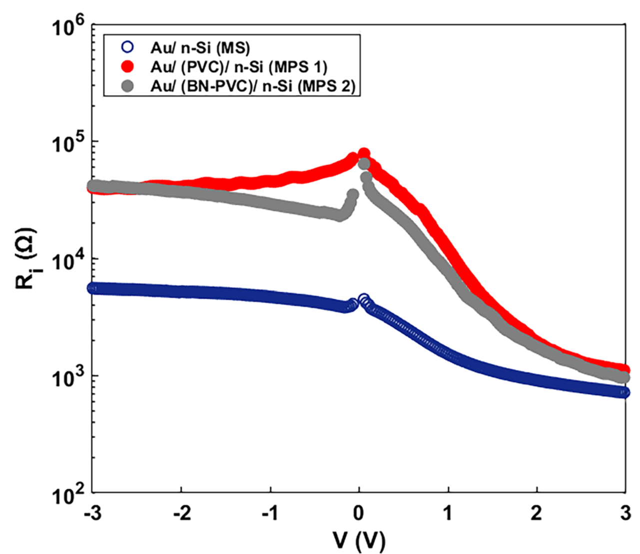

Fig. 6 The R i curves vs. V for the prepared samples

$$\frac{dV}{d(lnI)} = IR_s + \left(\frac{nkT}{q}\right) \tag{6a}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{A^*AT^2}\right) = IR_s + n\Phi_{B0} \tag{6b}$$

The presence of native or deposited interfacial layers and series resistance typically leads to deviations from linearity in ln(*I*)-*V* graphs, particularly in the forward bias region. Cheung functions display a linear segment in this range of applied voltages, enabling the derivation of (R_s, n) and (R_s, Φ_{B0}) parameters by utilizing the slope and intercept of d*V*/d(ln*I*)-*I* and H(*I*)-*I* graphs, respectively [33]. .

Figure 7 illustrates the I-dependent dV/d(lnI) and H(I) profiles for three different SDs. As can be seen, the extensive current range exhibits a well-linear behavior, making it possible to calculate the values of n, R_s, and Φ_{B0} using their slopes and intercepts. The key electrical parameters (n, R_s, and Φ_{B0}) computed by the TE theory and Cheung approaches are presented in Table 1 for manufactured SDs.

Generally, when the ln(I)-V graph deviates from linearity behavior, the Norde function is also able to

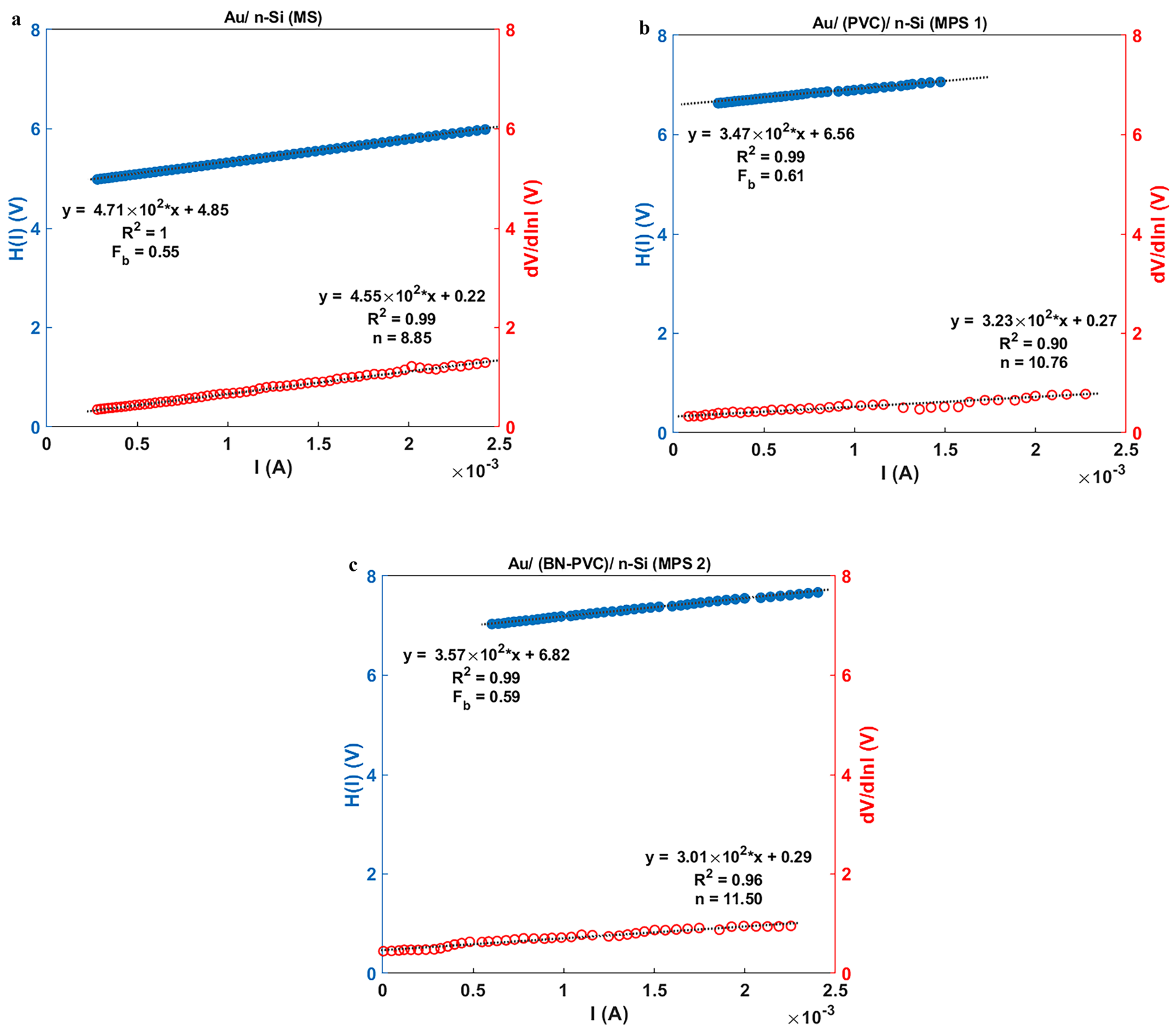

Fig. 7 Variations of dV/dln(I) and H(I) vs. I graphs of the manufactured SDs

provide the quantities of Φ_{B0} and R_s for the MS- and MPS-type SDs as follows [32]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I}{A^{*}AT^{2}}\right) \tag{7}$$

with γ being an integer number greater than ideality factor. Figure 8 represents the voltage-dependent F(V) for the fabricated based on Eq. (7). The values of Φ_{B0} and R_s could be obtained with utilization of a minimum point found at the concave part of the F(V) function as [32]:

$$\Phi_{B0} = F(V_{min}) + \frac{V_{min}}{\gamma} - \frac{kT}{q} \tag{8a}$$

$$R_s = \frac{kT}{q}\frac{(\gamma - n)}{I_{min}} \tag{8b}$$

Here, the minim point of F(V) function gives the parameters of V_{min} and I_{min}. Table 1 introduces the Φ_{B0} and R_s values given by the Norde function.

It must be noted that the interface states (N_{ss}) and non-uniformly doped atoms are to blame for a diode's less-than-ideal behavior. The voltage-dependent N_{ss} profile in the equilibrium condition is defined as [1, 34]:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{9}$$

where W_D denotes the depletion layer width, δ refers to the interlayer thickness, ε_s and ε_i being the permittivity of semiconductor and interfacial layer. The energy distinction between the conduction band edge and the N_{ss} level at a n-type semiconductor is defined as follows [1–3, 34]:

$$E_c - E_{ss} = q(\Phi_e - V) \tag{10}$$

In addition, the formula of n(V) and R_s gives the effective barrier height (Φ_e) as:

$$\Phi_e - \Phi_{B0} = \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{11}$$

Based on the Eqs. (9, 10 and 11), the energy-dependent N_{ss} plots for the manufactured structures are presented in Fig. 9. The peak of the N_{ss} curve for the MS-type SD is 6.74×10^{13} $eV^{-1}.cm^{-2}$, but the N_{ss} values for the MPS1- and MPS2-type SDs are 1.78×10^{13} $eV^{-1}.cm^{-2}$ and 1.79×10^{13} $eV^{-1}.cm^{-2}$, respectively. Thus, inserting PVC and PVC:BN interfacial layers reduce the maximum of the N_{ss} value for MS-type SD because they passivate the semiconductor surface [35–37].

Table 1 shows the primary electric parameters and N_{ss} density of the MS- and MPS-type SDs as determined by utilizing the Ohm's law, TE theory, Cheung,

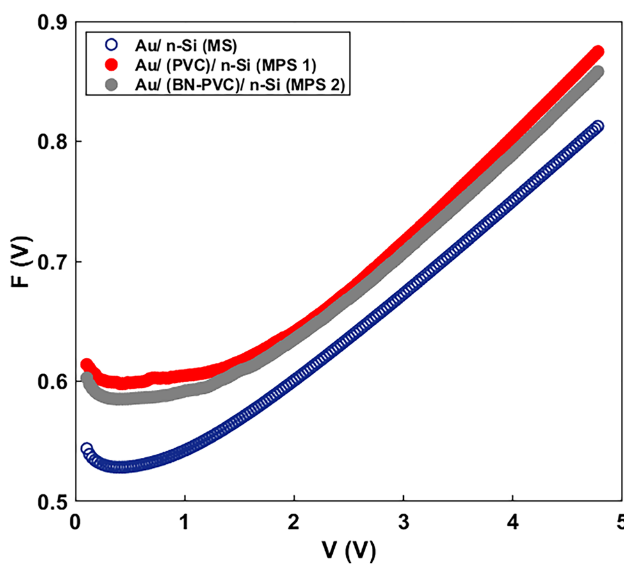

Fig. 8 The voltage-dependent F(V) function for the fabricated samples

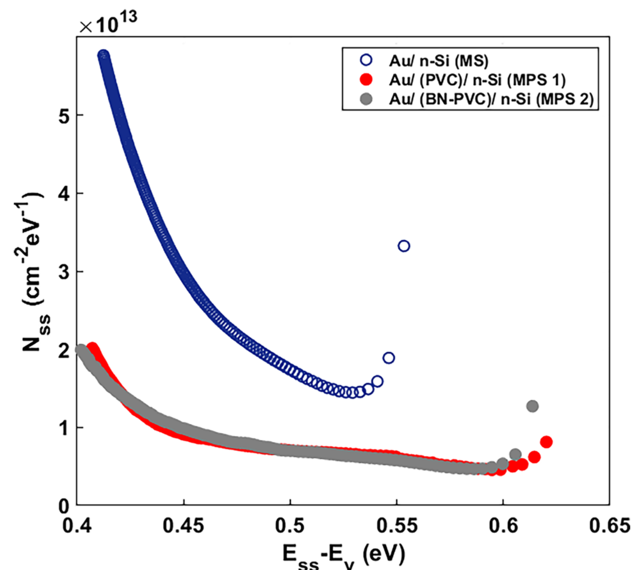

Fig. 9 Change of the energy dependent N ss curves for the prepared samples

Table 1 Electric factors of the prepared SDs determined using various approaches

Diode	Φ_{B0} (eV)			RR	R_s (Ω)				R_{sh} (kΩ)	n		$N_{ss} \times 10^{13}$ ($eV^{-1}.cm^{-2}$)
	TE	Norde	H(I)		TE	Norde	H(I)	dV/dln(I)		TE	dV/dln(I)	
MS	0.56	0.55	0.55	11	550	653	483	464	6.09	7.73	8.52	6.74
MPS1	0.63	0.66	0.63	38	825	888	500	433	31.6	6.88	8.85	1.78
MPS2	0.62	0.64	0.61	82	556	647	430	343	45.5	7.03	10.0	1.79

and Norde functions. As observed, using PVC and PVC:BN interfacial layers at the interface of the metal and semiconductor layers reduces the value of n in MPS-type SDs. Based on [$n = 1 + d_i/\varepsilon_s(\varepsilon_s/W_d + qN_{ss})$], the value of n, which represents the quality prepared SD, may deviate significantly from unity in practice due to a number of factors, including the presence of an interlayer, its thickness (d_i) and dielectric constant (ε_i), the measure of donor or acceptor atomic dopants, depletion layer width (W_d), a specific distribution of N_{ss} at the interface between the semiconductor and the interlayer, energy states in the semiconductor's band gap, image-force lowering of the semiconductor, generation-recombination electric charges, tunnelling through surface/interface-states, and barrier non-uniformities at the M/S interface [1–6]. On the other hand, the presence of these interlayers causes the BH of the MPS-type SDs to increase. It must be noted that the impurity bands introduced by lattice mismatches (broken bonds) between different layers are ignored, resulting in Φ_{B0} being underestimated [38]. Moreover, the trap or recombination central action introduced by doping is ignored, resulting in an overestimation of the effective current [39]. By increasing the R_{sh} and Φ_{B0} as well as decreasing the I_0, R_s, n, and N_{ss}, these interlayers improve the efficiency of the MS structure and the rectifying ratio. Regarding the values shown in Table 1, the results of the various calculations methods are in strong agreement with one another. These findings demonstrate that the PVC:BN interfacial layer, which has higher BH, R_{sh}, and RR and smaller I_0, R_s, n, and N_{ss}, can enhance the efficiency of the MS-type SD greater than traditional SiO_2. Similar results for the employed high-dielectric interfacial layer were also reported in the literature [7, 9, 29].

The free carrier current can also be affected by the interfacial layer, both in the reverse and forward bias voltage. Figure 10 shows the graphs of ln(I_F)-V_F for the MS- and MPS-type SDs fabricated in this research, which have two regions for the MS-type SD and three regions each for the MPS1- and MPS2-type SDs, each representing a separate conduction mechanism (CCM). Generally, deep trap creation at the interface of the interlayer and semiconductor can improve charge transmission. The slope of the two and three linear sections of the ln(I_F)-V_F profiles for the MS-type SD is equal to 1.0.9, 1.65; for the MPS1-type SD, it is 1.03, 3.20, 1.59; and for the MPS2-type SD, it is 1.48, 3.05, 2.01. When the slope's value is close to one, the semiconductor exhibits an ohmic manner (I–V) with the low voltage bias observed at section I, meaning the electrodes inject small charges into the semiconductor [1, 22, 34]. As a result of the predominance of the recombination-tunneling process, the current at section II reveals an exponential behavior of I–exp(V) by a slope greater than two [37]. Furthermore, the trap distribution of the space-charge limited current (SCLC) at the BN nanostructures band gap causes the current to alter similar to a power function (I–V^2) at section III of the MSP1- and MPS2-type SDs. It should be emphasized that the SCLC transport process only manifests when the charge content under equilibrium conditions is sufficiently lower than the charge concentration that was injected. Additionally, the increase in the number of electrons injected from the electrode causes the traps to fill up and the space charge to rise in the SCLC mechanism [1, 27, 34].

To examine the CCMs into MS- and MPS-type SDs at the reverse voltage bias, the change of the ln(I_R)-$V_R^{0.5}$ curves are introduced in Fig. 11. At the reversed-voltage bias, the mechanism of Poole-Frenkel (PF) and Schottky emissions might occur. Once PFE type CCM is overcome, the reverse electric current (I_R) is given by [29, 34, 37]:

$$I_R = I_0 \exp\left(\frac{\beta_{PF}}{kT}\sqrt{\frac{V}{d}}\right) \quad (12)$$

But it is indicated by the following relationship providing that the SE type CCM is predominance,

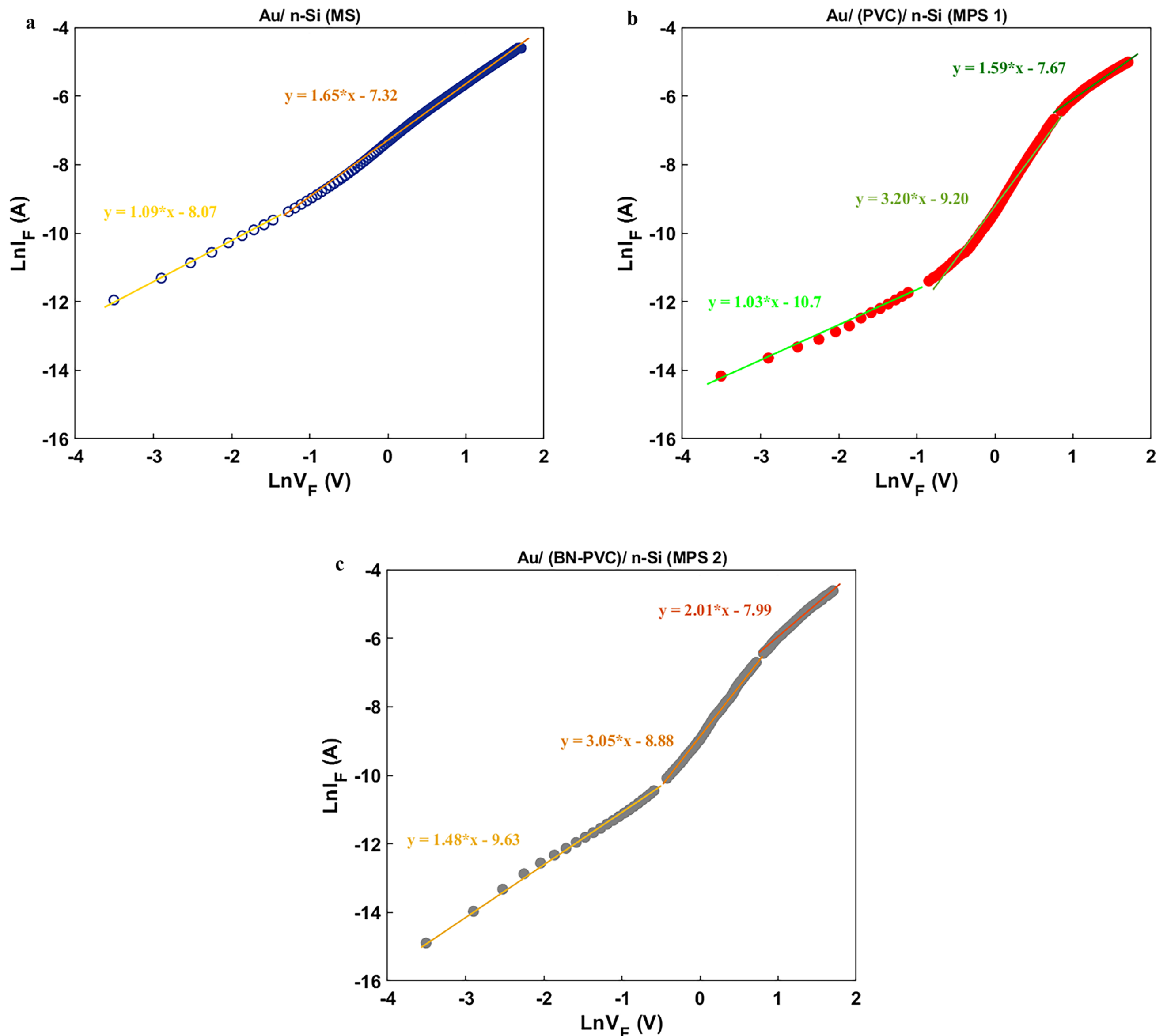

Fig. 10 The ln(I F)-V F profiles for the **a** MS, **b** MPS1, and **c** MPS2 structures

$$I_R = AA^*T^2\exp(-\frac{\Phi_B}{kT})\exp\left(\frac{\beta_{SC}}{kT}\sqrt{\frac{V}{d}}\right) \quad (13)$$

where β_{PF} and β_{SC} stand for the respective field lowering coefficients for the PFE and SE processes. The β_{PF}-β_{SC} relationship is typically expressed as follows [1, 29, 30]:

$$2\beta_{SC} = \beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon_r}\right)^{1/2} \quad (14)$$

with ϵ_r being the interlayer permittivity. Figure 11 illustrates linear behavior of the plots with a slope equal to the field lowering coefficient. According to the calculations, these numbers are 2.11 × 10^{-6} eV^{-1} $m^{0.5}V^{0.5}$ for MS-type SD, 1.81 × 10^{-5} eV^{-1} $m^{0.5}V^{0.5}$ for MPS1-type SD, and 1.00 × 10^{-5} eV^{-1} $m^{0.5}V^{0.5}$ for MPS2-type SD. For the MS-, MPS1-, and MPS2- SDs, the theoretical findings of PF are equivalent to 4.85 × 10^{-5} eV^{-1} $m^{0.5}V^{0.5}$, 1.34 × 10^{-5} eV^{-1} $m^{0.5}V^{0.5}$, and 1.39 × 10^{-5} eV^{-1} $m^{0.5}V^{0.5}$. It may be determined by comparing theoretical findings and experimental results that the SE

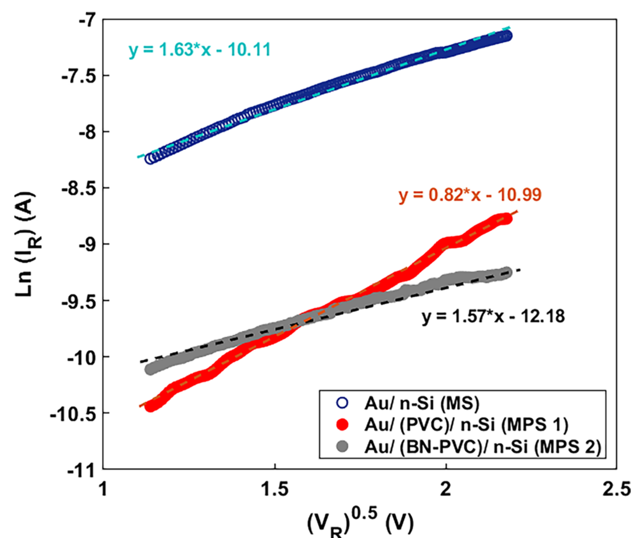

Fig. 11 The plot of ln(I R)-V R 0.5 for the MS-, MPS1-, and MPS2-type SDs

mechanism dominates for MS-type SD at reverse bias region whereas the PFE mechanism is prevailing for MPS-type SDs.

4 Conclusions

In this research, three MS-, MPS1-, and MPS2-type SDs with structures of Au/n-Si, Au/PVC/n-Si, and Au/PVC:BN/n-Si were carried out on the same n-Si wafer under the similar conditions. The key electronic features of these manufactured structures, namely I_0, BH, n, R_s, R_{sh}, RR, and N_{ss}, were derived using the various approaches and compared to one another with the measurement of I–V characteristics at the reverse and forward bias regions. In addition, the voltage-dependent Φ_{B0} and n into considered determine the energy-dependent N_{ss} density for three prepared samples. The computed I_0, Φ_{B0}, and n quantities were equal 2.04×10^{-5} A, 0.56 eV, 7.73 for MS-type SD, 1.12×10^{-6} A, 0.63 eV, 6.89 for MPS1-type SD, and 2.05×10^{-6} A, 0.62 eV, 7.03 for MPS2-type SD. It was discovered that the MPS2-type SD's RR was 7 times more than the MS-type SD's. Additionally, estimates of the MS, MPS1, and MPS2 structures' CCM were made at the reverse and forward bias region. The $\ln(I_R)$-$V_R^{0.5}$ graphs in the reverse voltage bias demonstrate that the PFE process occurs in the MPS structures while the SE-type CCM dominates in the MS structure. These experimental findings indicate that the PVC:BN interfacial layer enhances the efficiency of the MS structure by increasing Φ_{B0}, R_{sh}, and RR and decreasing n, R_s, and N_{ss}. Due to low cost, flexibility, small weight per molecule, and simple and inexpensive production processes, PVC:BN interfacial layer is therefore possible to successfully replace an interfacial insulator layer created by standard methods.

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Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Declarations

Competing interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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