

Frequency-dependent physical parameters, the voltage-dependent profile of surface traps, and their lifetime of Au/(ZnCdS-GO:PVP)/n-Si structures by using the conductance method

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ABSTRACT

In this study, frequency-dependent physical parameters, voltage-dependent of surface traps/states, and their lifetime of the Au/(ZnCdS-GO:PVP)/n-Si (MPS) type structures were investigated by using conductance measurements $(Y = 1/Z = G + j\omega C)$ both in wide range frequency (3 kHz-3 MHz) and voltage (from - 4.00 V to 1.50 V). Firstly, basic physical parameters such as density of doping donor atoms (N_D), diffusion potential (V_D), Fermi-energy (E_F), barrier height $\Phi_{\rm B}(C-V)$, depletion-layer thickness ($W_{\rm D}$), and maximum electric field (E_m) were calculated from these measurements for each frequency. These values were found as 1.69×10^{16} cm⁻³, 0.444 eV, 0.193 eV, 0.606 eV, 1.31×10^{-5} cm, 7.66 $\times 10^{4}$ V/cm for 10 kHz, and 1.42×10^{16} cm⁻³, 0.461 eV, 0.198 eV, 0.628 eV, 1.46×10^{-5} cm, 7.80×10^{4} V/cm for 3 MHz, respectively. While N_D decreases with increasing frequency, the other parameters increase. The density of surface states (N_{ss}) and their lifetimes (τ) were also obtained from conductance techniques. While the N_{ss} were changed between 2.78×10^{12} at 0.40 V and 2.61×10^{12} eV⁻¹cm⁻² at 1.3 V, and the N_{ss} -V curve shows two distinctive peaks which correspond to $0.5 \text{ V} (2.87 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2})$ and 1.2 V (2.68 × 10^{12} eV⁻¹cm⁻²), respectively. The values of τ were changed between 105 µs (at 0.4 V) and 15.3 µs (at 1.3 V) and decreased with increasing voltage as exponentially. These lower values of N_{ss} were attributed to the used (ZnCdS-GO:PVP) interlayer.

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1 Introduction

Since a thin film is grown between a semiconductor and metal as an interfacial layer, metal/semiconductor (MS) structures convert to metal/interlayer/semiconductor (MIS) type structures, and the existence of such interlayer gives them capacitor properties, which capable storage more and more electronic charges and so supply an additional/excess capacitance (C_{ex}) and conductance (G_{ex}) to the real-values of them [1–7]. While the *C* and *G* values at higher frequencies are independent of the frequency in ideal conditions and rise with applied biases increment, this case is considerably different at lower frequencies, and so the C and G values become quite dependent on the ability of N_{ss} to follow alternating signal [4, 6, 8]. In addition, when these devices have an interlayer, series resistance (R_s) , $N_{ss'}$ and dislocations, they considerably influence the electrical, optical, and dielectric features of the devices. The basic sources of the R_s are the back-ohmic and rectifier front-contacts, the probe wires usage for electrical measurements, the bulk-semiconductor resistivity, the existence of an interlayer as native or deposited interlayer, the doping atoms inhomogeneities, and the inhomogeneity of barrier height (BH) at M/S interface [1-3, 9, 10].

The stability of the surface of the semiconductor has an important role in the fabrication of semiconductor devices like an MS-type structure with/without an interlayer. In other words, all semiconductor devices are more useful for studying surfaces of semiconductors because their reliability and stability are highly related to preparing surface conditions and fabrication processes [11–13]. During the elaboration of these MS and MIS, more and more N_{ss} and dislocations may be produced, and their energies may be located at the junction in the semiconductor bandgap. These surface states act as recombination centers that can capture or release some electrons. They usually originate from non-saturated dangling bounds depending on the chemical composition of the interlayer and crystal lattice disorders [1–3, 14, 15]. The effect of these traps can be minimized either by good surface preparation and fabrication processes in very clean environments or by sufficiently high frequency utilizing voltagedependent capacitance and conductance measurements (C/G-V). The charges at traps cannot contribute to the measurements C and G values at higher frequencies ($f \ge 0.5$ MHz) because the relaxation time (τ) of them is long enough to permit the charges to move in or out of the trap in response to alternating signal [16–21]. But, R_s effects can be decreased by (i) making impedance measurements at enough low frequencies and (ii) applying an adjustment to the experimentally obtained *C* and *G* values for higher frequencies [2, 3].

In general, these traps are classified into five groups: (i) interface-trapped charges between interlayer and semiconductor, (ii) fixed oxide charges located near the interface; (iii) oxide trapped charges created by radiation, (iv) mobile ionic charges, (v) shallow-traps located near the conduction band (donor-type) or valance band (acceptor-type). Although there are many methods in the literature to determine and characterize the interface traps/states (D_{it} or N_{ss}), the most sensitive and accurate is the conductance method developed by Nicollian and Goetzberger which is more susceptible to $N_{\rm ss}$ values ~10⁹/(eV.cm²) [1, 2]. On the other hand, the one disadvantage of this method is quite laborious and time-consuming when compared to the low-high frequency capacitance (C_{LF} - C_{HF}) model developed by Castagne [22] and Hill and Coleman methods [16]. The conductance model is based on experimentally measured C_m and G_m values of the device as a function of voltage and frequency.

In our previous study [21], both the Au/ (ZnCdS:GO(1:1)-PVP)/n-Si (MPS1) and Au/ (ZnCdS:GO(1:0.5)-PVP)/n-Si (MPS2) SDs were fabricated onto the same n-Si wafer in same condition to determine the effect of doping rate of (ZnCdS:GO) on the electrical characteristics by using from the I-V and C/G-V (at 3 kHz and 3 MHz) measurements. For this aim, the basic electrical parameters (n, BH, and Rs) of them were also extracted from both the TE theory and Cheung functions to see their voltage dependence. Experimental results show that the MPS2 type SD is the best performance with respect to higher RR, $R_{sh'}$ and BH values, and low value of n, low leakage current, low N_{ss} low R_s, and high rectification ratio $(RR = I_{forward}/I_{reverse} at \pm 5 V)$, high BH when compared MPS1 type SD. Therefore, in this study, we aimed to achieve a better understanding of the effects of $N_{ss'}$ their lifetimes (τ), and R_s effects on the main electrical parameters, conduction mechanisms, and nature of barrier height (BH) formed at the M/S interface by using the used both conductance and $(C_{LF}-C_{HF})$ methods. For this aim, the impedance measurements were performed by utilizing a controllable HP 4192 A LF impedance analyzer between 1 kHz and 1 MHz, and all of them were performed via a microcomputer through an IEEE - 488 AC-DC converter card.

Experimental results show that all basic physical parameters depend considerably on frequency and voltage.

2 Experimental procedures

In the present study, Au/n-Si structures with (ZnCdS:GO) with (1:0.5) interlayer were fabricated onto an n-Si wafer which is a P-doped single crystal with 2" diameter, 100 orientation, 1 Ω cm resistivity, and ~300 µm thickness. Firstly, the wafer was cleaned by utilizing the standard RCA technique and dried with N₂ gas. Secondly, high-pure Al (99.999%) with 150 nm was thermally grown onto the back side Si substrate at 1µ Torr pressure and then sintered at 500 °C in nitrogen-ambient to get good ohmic contact. Thirdly, the prepared (ZnCdS:GO:PVP) solution was also thermally coated onto the front of the Si substrate with a 3000-rpm spin coater. Finally, the 99.999% pure Au Schottky contacts with 1 mm diameter were thermally grown onto the (ZnCds-GO:PVP) interlayer. A schematic diagram of the fabricated Au/(ZnCdS-GO:PVP)/n-Si (MPS) type structures and measured C-V-f and G-V-f systems were also represented in Fig. 1a, b respectively.

The fabricated samples were fixed on a copperholder via conductive silver paste to perform electrical measurements and connected to the sample by thin silver-coated Cu wires. The impedance measuring was realized by utilizing an impedance analyzer named HP-4192 A LF between 3 kHz and 3 MHz at RT in VPF-475 cryostat to obstacle any external effect at about 1 mTorr, and all measurements were controlled by a microcomputer via an AC–DC converter card of IEEE/488.

3 Experimental results and discussions

The values of C and G/ω versus voltage for various frequencies and versus frequency for various voltages are presented in Fig. 2a, b and Fig. 3a, b, respectively, accumulation, depletion, and inversion zones are clearly seen in Fig. 2a and 3a, which correspond to high, intermediate, and low bias voltages such as an MIS or MOS-type diode and capacitor. Obviously, the augmentation of *C* and *G* with decreasing biases was observed, particularly in the depletion zone. This increase or discrepancies in the C and G/ω versus V curves result from a special density distribution of N_{ss} and their τ . On the other, the observed broad peak behaviors in the forward bias *C*-*V* curves are the results of the series resistance of the structures. As can be observed by regions, while the N_{ss} are effectual, especially in depletion and weak inversion at lower frequencies, R_s is effectual only at accumulation at higher frequencies, respectively [1, 3, 7, 9]. Because interface traps can readily track an ac signal and so on, they make an additional



Fig. 1 a A schematic presentation of the fabricated Au/(ZnCdS-GO:PVP)/n-Si (MPS) structures and b the measured C-V-f and G-V-f system





Fig. 2 a The C - V curves at distinct frequencies and b C - lnf curves at the distinct biases



Fig. 3 a The G/ω - V curves at distinct frequencies and b G/ω - lnf curves at distinct biases

contribution to both the actual *C* and *G*/ ω values at lower and moderate frequencies [23–27]. Under an external electric field, the electronic charges at the surface states can be restructured and rearranged, especially at low frequencies, leading to a shift in the *C*/*G*-*V* plots.

Both the space charge (Q_{sc}) and depletion-layer capacitance (*C*) per unit area of the structure are given as follows [3]:

$$Q_{sc} = \sqrt{2q\epsilon_s\epsilon_0 N_D \left(V_D - V - \frac{kT}{q}\right)} \tag{1}$$

$$C = \frac{\left|\partial Q_{SC}\right|}{\partial V} = \sqrt{\frac{q\epsilon_s \epsilon_0 N_D}{2\left(V_D - V - \frac{kT}{q}\right)}}$$
(2)

Equation 2 can be rearranged as follows:

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$$1/C^2 = \frac{2(V_D - V - \frac{kT}{q})}{(q\varepsilon_s\varepsilon_0 A^2 N_D)}$$
(3)

Here, V_D (= $V_0 + kT/q$) is the diffusion potential, and V_0 is the point where the $1/C^2$ - V plot intersects the y-axis at zero. The density of donor atoms (N_D) can be extracted from the $1/C^2$ - V plot's slope as follow (Fig. 4):

$$N_D = \frac{2}{q\epsilon_s \epsilon_0 A^2 \left(\frac{dC^{-2}}{dV}\right)} \tag{4}$$

The Fermi energy (E_r) , depletion-layer thickness (W_D) , maximum electric field (E_m) at junction, and $\Phi_{\rm B}({\rm C-V})$ values were calculated by using intercept voltage (V_0) and slope of the $1/C^2$ - V plot (Fig. 4) by using following relations for each frequency, respectively [2, 28]:

$$E_F = \left(\frac{kT}{q}\right) \ln\left(\frac{N_c}{N_D}\right), W_D = \sqrt{\frac{2\epsilon_s \epsilon_0 V_D}{qN_D}}, E_m = \sqrt{\frac{2qN_D V_0}{\epsilon_s \epsilon_0}} and \Phi_{B(C-V)} = V_0 + \frac{kT}{q} + E_F$$
(5)



Fig. 4 The $1/C^2$ - V plots for distinct frequencies

Thus, the calculated electrical parameters of the structure between 10 kHz and 3 MHz are presented in Table 1.

As can be clearly seen from Table 1; Fig. 5a, while the value of N_D decreases with increasing frequency, E_m increases almost exponentially. Besides, both the W_D and Φ_B (C-V) rise with frequency increment almost linearly, as presented in Fig. 5b. Because the decrease of capacitance leads to an increase in the $1/C^2$ and so on, this plot gives a large intercept voltage. As shown in Fig. 5b, the barrier height is changed with $\ln f$ as $\Phi_{\rm B}$ $(C-V) = (3.9 \times 10^{-3}x + 0.5694)$ eV. It is clear that the frequency-dependent coefficient of BH (3.9×10^{-3}) eV/Hz.

The R_s of the structure is also strongly influential on the C-V and G/ω -V plots, especially at the

Table 1Some basicelectrical parameters of theAu/(ZnCdS-GO:PVP)/n-Si	f (kHz)	$N_{\rm D} ({\rm cm}^{-3}) {\rm x} 10^{16}$	V _D (eV)	E _F (meV)	$\Phi_{\rm B}\left({\rm eV}\right)$	W _D (cm) x10 ⁻⁵	E _m (V/cm) x10 ⁴
structure	10	1.689	0.444	193.0	0.606	1.31	7.658
	20	1.646	0.445	193.6	0.608	1.33	7.667
	30	1.592	0.446	194. 5	0.610	1.35	7.675
	40	1.592	0.447	194.6	0.611	1.35	7.684
	50	1.579	0.448	194.7	0.612	1.36	7.692
	70	1.566	0.449	194.9	0.613	1.37	7.701
	100	1.554	0.451	195.1	0.615	1.38	7.714
	200	1.518	0.453	195.7	0.618	1.40	7.735
	300	1.494	0.454	196.1	0.620	1.41	7.746
	400	1.483	0.455	196.3	0.621	1.42	7.755
	500	1.460	0.456	196.7	0.622	1.43	7.761
	700	1.460	0.457	196.7	0.623	1.43	7.766
	1000	1.450	0.458	196.9	0.624	1.44	7.775
	2000	1.418	0.460	197.5	0.626	1.45	7.791
	3000	1.418	0.461	197.6	0.628	1.46	7.803



Fig. 5 a The change in $E_{\rm m}$ and $N_{\rm D}$ values with frequency. b The change in $W_{\rm D}$ and $F_{\rm B}$ values with frequency

accumulation region for high frequencies. As seen in Fig. 3a and 4a, while *C* starts to decrease slightly at the accumulation region, G/ω increases sharply due to the decrement in series resistance with frequency increment (G = 1/R). Such behavior at accumulation or positive bias region is called "inductive behavior" and is usually attributed to R_s and interfacial layer [2, 3]. Therefore, the voltage-dependent profile of resistance (R_i) was extracted from the Nicollian and Brews [2] technique for each frequency by using Eq. 6 and is given in Fig. 6. As shown in Fig. 6a, the values of R_i

usually decrease with increasing voltage for each frequency up to -0.5 V and then give a peak between ±0.5 V due to a special distribution of N_{ss} in the bandgap of semiconductor. However, as shown in Fig. 6b, the value of R_i becomes voltage independent at high frequencies at accumulation region, which corresponds to the real value of R_s at higher frequencies. In other words, R_s decreases almost exponentially with frequency for all voltage levels due to the inability of the AC signal to follow N_{ss} at higher frequencies.



Fig. 6 a The R_s - V plot for distinct frequencies. b The R_s - lnf plot for distinct frequencies

$$R_i(V_i) = \frac{G_{mi}}{G_{mi}^2 + (\omega C_{mi})^2}$$
(6)

As explained above, R_i is the resistance of the sample for any applied bias voltage, but the real value of R_s is corresponding to the strong accumulation region (at about 1.5 V) at enough high frequencies. Therefore, Eq. 6 can be rewritten as following.

$$R_s(V_a) = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}$$
(7)

In other words, in Eq. 7; C_{ma} and G_{ma} are the measured capacitance and conductance values at strong accumulation region (V_a =1.5 V).

In order to see the R_s effects on the *C* and G/ω data for higher frequencies, the related plots for 1 MHz were adjusted to eliminate the R_s effect by utilizing Eq. 8. which was proposed by Nicollian and Brews [2]: If the R_s effect is not eliminated, especially at high frequency and forward bias, it can lead to incorrect calculations and interpretations of the electrical and dielectric properties of the structure. compared to $C_{m'}$ but the G_c/ω curve displays a distinctive peak at about 1 V. These results are indicated that R_s is quite effectual both on the *C* and G/ω data for higher frequencies and so R_s should be considered in the electric and dielectric parameters calculation or conduction mechanism of these devices [29–34]. On the other hand, the R_s effect can be ignored at lower frequencies in the inversion and depletion regions.

It is well known that in MS contacts with/without a thin interlayer, many surface states or traps may occur between the interlayer and the semiconductor, which have energy levels in the forbidden bandgap of the semiconductor. They can arise from various sources, such as the cleaning of wafer and/or fabrication processes, disorders in the periodic lattice, and non-saturated dangling bonds at the interlayer/semiconductor interface. Thus, they act like recombination centers that can capture or release positive/negative electronic charges and so leads to an addition/excess capacitance and conductance [1–7]. There are many techniques to calculate surface states, such as the forward bias *I-V* technique proposed by Card and Rhoderick [35], the high-low frequency capacitance technique, and the

$$C_{c} = \frac{\left[G_{m}^{2} + (\omega C_{m})^{2}\right]C_{m}}{(\omega C_{m})^{2} + a^{2}}, \ G_{c} = \frac{\left[G_{m}^{2} + (\omega C_{m})^{2}\right]a}{(\omega C_{m})^{2} + a^{2}} \ where \ a = G_{m} - \left[G_{m}^{2} + (\omega C_{m})^{2}\right]R_{s'}$$
(8)

Thus, corrected C_c and G_c/ω values were obtained from Eq. 8 and are presented in Fig. 7a and b, respectively, and there is a noticeable increase in C_c conductance or statistical model proposed by Nicollian-Goetzberger [1]. This method is based on measuring the capacitance (C_m) and conductance (G_m/ω) of



Fig. 7 a The measured and corrected capacitance at 1 MHz.b The measured and corrected conductance at 1 MHz

the structure as a function of voltage and frequency, and subsequently calculating the parallel conductance (G_p/ω) by solving a small signal equivalent circuit. Parallel conductance represents the loss mechanism occurring when the N_{ss} capture or emit charges, and is used to extract the Nss and their lifetimes. In addition, the most accurate/reliable one is the conductance technique [36] which is the frequency of applied bias voltage for a certain dc voltage in the depletion region is expressed as follows:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_i}{G_m^2 + \omega^2 (C_i - C_m)^2} = \frac{qAN_{ss}}{2\omega\tau} \ln(1 + (\omega\tau)^2)$$
(9)

In Eq. 9, τ is the lifetime of the charges at traps, which shows the characteristic time required to fill and empty these traps [37, 38]. As presented in Fig. 8, G_p/ω - ln*f* curve gives a peak for each bias and so N_{ss} and τ can be obtained from the peak value of parallel conductance by the following expressions [1, 2]:

$$N_{ss} = (G_p/w)_{\max} / (0.402qA) \quad wt = 1.98 \text{ ort} = 1.98/w$$
(10)

The conductance analysis of the structure was performed, and the voltage-dependent of the N_{ss} and their τ between 0.40 and 1.30 V were determined. The voltage-dependent of N_{ss} and τ values were presented as N_{ss} - V and τ - V plots by utilizing Eq. 10 and represented in Fig. 9. As shown in Fig. 9, N_{ss} were changed between 2.78 × 10¹² at 0.40 V and 2.61 × 10¹² eV⁻¹cm⁻²



Fig. 8 The G_p/w - lnf plots for distinct voltages



Fig. 9 The acquired voltage-dependent of N_{ss} and *t* by conductance method

at 1.3 V and also the N_{ss} -V curve has a two distinctive peaks which corresponds to the 0.5 V (2.87 × 10¹² eV⁻¹cm⁻²) and 1.2 V (2.68 × 10¹² eV⁻¹cm⁻²), respectively. On the other hand, the τ values were changed between 105 µs (at 0.4 V) and 15.3 µs (at 1.3 V) and also decreased with increasing voltage as almost exponentially [39]. It can be noted that the distribution of N_{ss} densities with an average value of 10¹² eV⁻¹cm⁻² is quite acceptable for MIS-type devices, and these low values are stemmed from the passivation effect of the interfacial layer used (ZnCdS-GO:PVP) [40, 41].

There is another way to acquire the voltage-dependent profile of N_{ss} , which can be performed by measuring the measured capacitance (C_m) at enough high frequency (≥ 1 MHz) and at enough low frequency (≤ 1 kHz), which is known as the (C_{HF} - C_{LF}) capacitance method. This technique is easier and faster when compared with the conductance method, and moreover, it gives accurate results close to it. According to the technique, at low frequency, N_{ss} can respond easily to the ac signal and so yield an excess *C* to the real value of them, but at higher frequency, tracking ac signal is not simple and so didn't contribute to the measured capacitance [1, 3, 42, 43]. Therefore, the N_{ss} values can be calculated from the difference between the C_{LF} and C_{HF} capacitance as given follow:

$$qAN_{\rm ss} = \left[\left(\frac{1}{C_{\rm LF}} - \frac{1}{C_i} \right)^{-1} - \left(\frac{1}{C_{\rm HF}} - \frac{1}{C_i} \right)^{-1} \right]$$
(11)

Here, C_i is the interfacial layer capacitance, C_{LF} is the measured *C* at low frequency (3 kHz), C_{HF} is the measured *C* at high frequency (3 MHz), and *A* is the



Fig. 10 The voltage-dependent curve of N_{ss} obtained from the low-high frequency capacitance technique

contact area of the rectifier. Thus, the voltage-dependent profile of N_{ss} was also extracted from Eq. 11. The N_{ss} -V plot gives a distinguishing peak nearly at 0.3 V due to a specific dispersion of N_{ss} in the forbidden bandgap of the semiconductor, as presented in Fig. 10.

Similar results on the interfacial pure and metal or metal-oxide doped organic/polymer interfacial layer, Nss and Rs effects both on the basic electrical parameters, conduction mechanism, and the nature of barrier height (BH) formed at Au/n-Si interface in wide range of frequency, temperature, and voltage have been reported in the literature in the last years [13, 42-48]. According to they, Rs is usually rooted from the ohmic/rectifier contacts, the used probe wires, bulk-resistance of the semiconductor, surface states/traps at interlayer/semiconductor surface, some impurities at surface of semiconductor, and non-uniform doped acceptor/donor atoms into semiconductor. On the other hand, interface states are usual rooted from the unsaturated dangling bonds, oxygen vacancies, doping energy level of donor/acceptor atoms, the defect in the crystal lattices, and some other impurities formed during fabrication processes. On the other hand, when the electrical measurements are taken only in a single or narrow frequency and voltage range, they cannot provide sufficiently reliable and accurate results on the electrical parameters, the nature of barrier height between metal and semiconductor, and conduction mechanisms. Therefore, admittance (Y = 1/Z)or impedance measurements, which include a set of C-V-f and G-V-f curves over a wide range of voltages (-4/1.5 V by 50 mV steps) and frequencies (from 3 kHz to 1 MHz) by using an HP 4192 A LF impedance meter for 19 different frequencies to get more accuracy and reliable results on the basic electrical parameters as a function of frequency and voltage, nature of barrier height at Au/n-Si interface, and conduction mechanism of the fabricated Au/(ZnCds-GO:PVP)/n-Si (MPS) type structures instead of congenital metal/insulator/semiconductor (MIS) type structures.

4 Conclusion

In this study, we prepared Au/(ZnCdS-GO:PVP)/n-Si (MPS) type structures instead of MOS-type structures. Both their frequency and voltage-dependent basic electrical parameters were acquired by the measured impedance spectroscopy method in the 3 kHz – 3 MHz interval and in the – 4.00 V to 1.50 V range, respectively. These values were found as 1.69×10^{16} cm⁻³, 0.444 eV, 0.193 eV, 0.606 eV, 1.31×10^{-5} cm, 7.66 × 10^4 V/cm for 10 kHz, and 1.42×10^{16} cm⁻³, 0.461 eV, 0.198 eV, 0.628 eV, $1.46 \times 10^{-5} \text{ cm}$, $7.80 \times 10^{4} \text{ cm}$ V/cm for 3 MHz, respectively. All of them were raised with rising frequency except for N_D . The voltage-dependent profile of the density of N_{ss} and their τ were extracted from the conductance techniques, and while the values of N_{ss} were changed between 2.78×10^{12} at 0.40 V and 2.61×10^{12} eV⁻¹cm⁻² at 1.3 V and the N_{ss} -V plot shows two distinctive peaks which are corresponding to 0.5 V ($2.87 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$) and 1.2 V (2.68 × 10¹² eV⁻¹ cm⁻²), respectively. Besides, τ decreases with voltage increment and varies between 105µs (at 0.4 V) and 15.3 µs (at 1.3 V). The voltagedependent profile of N_{ss} was also extracted from the $(C_{LF}-C_{HF})$ capacitance method as a second way. The calculated lower values of N_{ss} are indicated that (ZnCdS-GO:PVP) polymer interlayer leads to the passivation effect of the surface states.

Author contributions

Çiğdem Ş. Güçlü: Manufacturing, investigation, measurements, calculations, writing, reviewing & editing. Esra Erbilen Tanrıkulu: Investigation, calculations, writing, reviewing & editing. Murat Ulusoy: Investigation, measurements, calculations, reviewing & editing. Yashar Azizian-Kalandaragh: Manufacturing, investigation & measurements. Şemsettin Altındal: Review, editing & supervising.

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Data availability

The datasets generated and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest There are no conflicts to declare.

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References

 E.H. Nicollian, A. Goetzberger, The Si-SiO₂ Interface -Electrical properties as determined by the Metal-Insulator-Silicon Conductance technique. Bell Syst. Tech. J. 46, 1055–1033 (1967)

- E.H. Nicollian, J.R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology (Wiley, New Jersey, 2002)
- 3. S.M. Sze, K.K. Ng, *Physics of Semiconductor Devices* (Wiley, New Jersey, 2006)
- S. Alptekin, S.O. Tan, S. Altındal, Determination of Surface States Energy Density distributions and Relaxation Times for a Metal-Polymer-Semiconductor structure. IEEE Trans. Nanotechnol. 18, 1196–1199 (2019)
- İ Taşçıoğlu, S.O. Tan, Ş Altındal, Frequency, voltage and illumination interaction with the electrical characteristics of the CdZnO interlayered Schottky structure. J. Mater. Sci. 30, 11536–11541 (2019)
- V. Manjunath, V. Rajagopal Reddy, P.R. Sekhar Reddy, V. Janardhanam, C.-J. Choi, Electrical and frequency-dependent properties of Au/Sm₂O₃/n-GaN MIS junction with a high-k rare-earth Sm₂O₃ as interlayer. Curr. Appl. Phys. 17, 980–988 (2017)
- M. Sharma, S.K. Tripathi, Analysis of interface states and series resistance for Al/PVA:n-CdS nanocomposite metal– semiconductor and metal–insulator–semiconductor diode structures. Appl. Phys. A 113, 491–499 (2013)
- G. Ersöz Demir, İ Yücedağ, Ş Altındal, Investigation of effects on dielectric properties of different doping concentrations of Au/Gr-PVA/p-Si structures at 0.1 and 1 MHz at room temperature. J. Mater. Sci. 31, 16324–16331 (2020)
- E.E. Tanrıkulu, S. Demirezen, Ş Altındal, İ Uslu, On the anomalous peak and negative capacitance in the capacitance-voltage (C-V) plots of Al/(%7 Zn-PVA)/p-Si (MPS) structure. J. Mater. Sci. 29, 2890–2898 (2018)
- H. Xiao, S. Huang, Frequency and voltage dependency of interface states and series resistance in Al/SiO₂/p-Si MOS structure. Mater. Sci. Semicond. Process. 13, 395–399 (2010)
- D. Ata, S. Altındal Yeriskin, A. Tataroğlu, M. Balbası, Analysis of admittance measurements of Al/Gr-PVA/p-Si (MPS) structure. J. Phys. Chem. Solids. 169, 110861 (2022)
- H. Tecimer, H. Uslu, Z.A. Alahmed, F. Yakuphanoğlu, Ş. Altındal, On the frequency and voltage dependence of admittance characteristics of Al/PTCDA/p-Si (MPS) type Schottky barrier diodes (SBDs). Compos. B: Eng. 57, 25–30 (2014)
- M. Ulusoy, Y. Badali, G. Pirgholi-Givi, Y. Azizian-Kalandaragh, Ş. Altındal, The capacitance/conductance and surface state intensity characteristics of the Schottky structures with ruthenium dioxide-doped organic polymer interface. Synth. Met. 292, 117243 (2023)
- 14. H.G. Çetinkaya, S. Demirezen, S. Altındal, Yerişkin, Electrical parameters of Au/(%1Ni-PVA)/n-Si (MPS) structure:

surface states and their lifetimes. Phys. B Condens. Matter. **621**, 413207 (2021)

- S. Demirezen, Ş. Altındal, Y. Azizian-Kalandaragh, A.M. Akbaş, A comparison of Au/n-Si Schottky diodes (SDs) with/without a nanographite (NG) interfacial layer by considering interlayer, surface states (N_{ss}) and series resistance (R_s) effects. Phys. Scr. 97, 055811 (2022)
- W.A. Hill, C.C. Coleman, A single-frequency approximation for interface-state density determination. Solid State Electron. 23, 987–993 (1980)
- A. Feizollahi Vahid, S. Alptekin, N. Basman, M. Ulusoy, Y. Şafak Asar, Ş Altındal, The investigation of frequency dependent dielectric properties and ac conductivity by impedance spectroscopy in the Al/(Cu-doped Diamond Like Carbon)/Au structures. J. Mater. Sci. 34, 1118 (2023)
- Y. Şafak Asar, A. Feizollahi Vahid, N. Basman, H.G. Çetinkaya, Ş. Altındal, Frequency-dependent electrical parameters and extracted voltage-dependent surface states in Al/ DLC/p-Si structure using the conductance method. Appl. Phys. A **129**, 358 (2023)
- S. Altındal Yerişkin, E. Erbilen Tanrıkulu, M. Ulusoy, Dielectric properties of MS diodes with Ag:ZnO doped PVP interfacial layer depending on voltage and frequency. Mater. Chem. Phys. 303, 127788 (2023)
- J.A.M. Alsmael, N. Urgun, S.O. Tan, H. Tecimer, Effectuality of the Frequency Levels on the C&G/ω–V Data of the Polymer Interlayered Metal-Semiconductor Structure. Gazi Univ. J. Sci. Part. A: Eng. Innov. 9, 554–561 (2022)
- Ç.Ş Güçlü, E. Erbilen Tanrıkulu, A. Dere, Ş Altındal, Y. Azizian-Kalandaragh, A comparison of electrical characteristics of the Au/n-Si Schottky diodes with (ZnCdS:GO(1:1) and (ZnCdS:GO(1:0.5) doped PVP interlayer using current-voltage (I-V) and impedance-voltage (Z-V) measurements. J. Mater. Sci. 34, 1909 (2023)
- 22. R. Castagne, A. Vapaille, Apparent interface state density introduced by the spatial fluctuations of surface potential in an M.O.S. structure. Electron. Lett. **6**, 691 (1970)
- N. Kumar, A. Raman, Performance Assessment of the Charge-Plasma-Based Cylindrical GAA Vertical Nanowire TFET With Impact of Interface Trap Charges. IEEE Trans. Electron. Devices. 66, 4453–4460 (2019)
- M. Yıldırım, Characterization of the framework of Cu doped TiO₂ layers: An insight into optical, electrical and photodiode parameters. J. Alloys Compd. **773**, 890–904 (2019)
- Ö. Sevgili, L.B. Tasyürek, S. Bayındır, İ. Orak, E. Calışkan, The current transformer mechanism and structural properties of novel Al/BODIPY/pSi and Au/BODIPY/pSi

heterojunctions. Mater. Sci. Semicond. Process. 130, 105805 (2021)

- Y. Slimani, B. Unal, E. Hannachi, A. Selmi, M.A. Almessiere, M. Nawaz, A. Baykal, I. Ercan, M. Yıldız, Frequency and dc bias voltage dependent dielectric properties and electrical conductivity of BaTiO₃SrTiO₃/(SiO₂)x nanocomposites. Ceram. Int. 45, 11989–12000 (2019)
- A.R. Deniz, A.İ. Taş, Z. Çaldıran, Ü. İncekara, M. Biber, Ş. Aydoğan, A. Türüt, Effects of PEDOT:PSS and crystal violet interface layers on current-voltage performance of Schottky barrier diodes as a function of temperature and variation of diode capacitance with frequency. Curr. Appl. Phys. 39, 173–182 (2022)
- B. Akın, Ş. Altındal, On the frequency and voltage-dependent main electrical parameters of the Au/ZnO/n-GaAs structures at room temperature by using various methods. Phys. B Condens. Matter. 594, 412274 (2020)
- 29. S.O. Tan, I. Taşcıoğlu, S. Altındal, Frequency response of metal-semiconductor structures with thin-films sapphire interlayer by ALD technique. IEEE Trans. Electron. Devices. **68**, 5085–5089 (2021)
- İ. Taşçıoğlu, M. Soylu, Ş. Altındal, A.A. Al-Ghamdi, F. Yakuphanoğlu, Effects of interface states and series resistance on electrical properties of Al/nanostructure CdO/p-GaAs diode. J. Alloys Compd. 541, 462–467 (2012)
- Ç. Bilkan, Ş. Altındal, Y. Azizian-Kalandaragh, Investigation of frequency and voltage dependence surface states and series resistance profiles using admittance measurements in Al/p-Si with Co₃O₄-PVA interlayer structures. Phys. B Condens. Matter. **515**, 28–33 (2017)
- M.T. Güneşer, H. Elamen, Y. Badali, Ş. Altındal, Frequency dependent electrical and dielectric properties of the Au/(RuO₂:PVC)/n-Si (MPS) structures. Phys. B: Condens. Matter. 657, 414791 (2023). https://doi.org/10.1016/j. physb.2023.414791
- A. Nikravan, Y. Badali, Ş. Altındal, İ. Uslu, İ. Orak, On the Frequency and Voltage-Dependent Profiles of the Surface States and Series Resistance of Au/ZnO/n-Si Structures in a Wide Range of Frequency and Voltage. J. Electron. Mater. 46, 5728–5736 (2017)
- İ. Taşçıoğlu, Ö. Sevgili, Y. Azizian-Kalandaragh, Ş. Altındal, Frequency-Dependent Admittance Analysis of Au/n-Si Structure with CoSO₄-PVP Interfacial Layer. J. Electron. Mater. 49, 3720–3727 (2020)
- H.C. Card, E.H. Rhoderick, Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. J. Phys. D: Appl. Phys. 4, 1589 (1971)
- 36. O. Rejaiba, A.F. Braña de Cal, A. Matoussi, A comprehensive study on the interface states in the ECR-PECVD

SiO₂/p-Si MOS structures analyzed by different method. Phys. E: Low Dimens Syst. Nanostruct. **109**, 84–92 (2019)

- N. Fukuhara, F. Horikiri, T. Yamamoto, T. Osada, K. Kasahara, T. Inoue, T. Egawa, Admittance frequency dispersion in lateral AlGaN/GaN Schottky barrier diodes: Other origins of two *Gp*/ω peaks. J. Appl. Phys. **133**, 085702 (2023)
- A. Gaur, D. Chiappe, D. Lin, D. Cott, I. Asselberghs, M. Heyns, I. Radu, Analysis of admittance measurements of MOS capacitors on CVD grown bilayer MoS. 2D Mater. 6, 035035 (2019)
- E. Arslan, S. Ural, Ş. Altındal, E. Özbay, Determination of current transport and trap states density in AlInGaN/ GaN heterostructures. Microelectron. Reliab. 103, 113517 (2019)
- M. Ulusoy, Ş. Altındal, Y. Azizian-Kalandaragh, S. Özçelik, Z. Mirzaei-Kalar, The electrical characteristic of an MIS structure with biocompatible minerals doped (Brushite + Monetite:PVC) interface layer. Microelectron. Eng. 258, 111768 (2022)
- Z. Hosseini, Y. Azizian-Kalandaragh, S. Sobhanian, G. Pirgholi-Givi, M. Kouhi, Comparison of capacitancefrequency and current-voltage characteristics of Al/CdS-PVP/p-Si and Al/p-Si structures. Phys. B: Condens. Matter. 640, 413836 (2022)
- A. Türüt, A. Karabulut, K. Ejderha, N. Bıyıklı, Capacitance-conductance-current-voltage characteristics of atomic layer deposited Au/Ti/Al₂O₃/n-GaAs MIS structures. Mater. Sci. Semicond. Process. **39**, 400–407 (2015)
- Ş. Altındal, H. Kanbur, İ. Yücedağ, A. Tataroğlu, On the energy distribution of interface states and their relaxation time and capture cross section profiles in Al/SiO₂/p-Si

(MIS) Schottky diodes. Microelectron. Eng. **85**, 1495–1501 (2008)

- Ç.Ş. Güçlü, A.F. Özdemır, A. Kökce, Ş. Altındal, Frequency and Voltage-Dependent Dielectric Properties and AC Electrical Conductivity of (Au/Ti)/Al₂O₃/n-GaAs with Thin Al₂O₃ Interfacial Layer at Room Temperature. Acta Phys. Pol. A **130**, 325–330 (2016)
- I. Orak, A. Karabulut, Frequency and voltage dependence of electrical conductivity, complex electric modulus, and dielectric properties of Al/Alq3 /p-Si structure. Turkish J. Phys. 44, 85–95 (2020)
- N. Bıyıklı, A. Karabulut, H. Efeoğlu, B. Güzeldir, A. Türüt, Electrical characteristics of Au/Ti/n-GaAs contacts over a wide measurement temperature range. Phys. Scr. 89, 095804 (2014)
- Ş Altındal, A.F. Özdemir, Ş Aydoğan, A. Türüt, Discrepancies in barrier heights obtained from current–voltage (IV) and capacitance–voltage (CV) of Au/PNoMPhPPy/n-GaAs structures in wide range of temperature. J. Mater. Sci. 33, 12210–12223 (2022)
- E. Erbilen Tanrıkulu, I. Taşçıoğlu, Variation of the surface states and series resistance depending on voltage, and their effects on the electrical features of a Schottky structure with CdZnO interface. J. Electron. Mater. 52, 2432–2440 (2023)

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