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Characterisation of interface states of Al/p-Si Schottky diode by current–voltage and capacitance–voltage–frequency measurements

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ABSTRACT

In this study, the fabricated Al/*p*-Si Schottky diode is characterised at room temperature using current–voltage (*I–V*) and capacitance–voltage–frequency (*C–V–f*) techniques. The energy distribution profile of the diode's interface state density is generated using different diode parameters. In the *I–V* measurements, the variation in energy, charge, and density of the interface states is described in terms of the applied forward bias with respect to the zero Schottky barrier height. The capacitance measurements, on the other hand, are used to address a long-standing low-voltage capacitance peak in terms of the distribution of interface state charge. In general, both techniques complement each other, indicating that the space charge region (SCR) starts to be varied at a voltage of − 0.66 V, after the compensation of interface states by majority carriers. The findings presented here are critical for current and future research on junction-based devices for a variety of applications in which the SCR and bulk material properties are examined solely from metal-semiconductor (m–s) interface states.

1 Introduction

Schottky diodes are the simplest metal-semiconductor (m–s) contact devices that are used in opto-electronic [1–6] and radiation sensing applications [7–10]. The performance, reliability, and stability of the devices during operation are influenced by the interface layer [11–19], the distribution of interface states between metal and semiconductor [20, 21], as well as the defects and dopants in the semiconductor [22–25]. Among others, the interface states degrade the quality of the devices, resulting in a high leakage current and an ideality factor of the device higher than unity [21]. In addition, the interface states are responsible for the recombination of majority carriers, resulting in degradation of the device's performance. The interface states are formed between the metal contact and semiconductor either during the surface preparation or the evaporation of metal, and they are because of the interruption of the periodic

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lattice structure at the semiconductor surface [26]. As a result of the device fabrication process involving direct metal deposition on the semiconductor, the interface states are unavoidable, and a thorough study of them is necessary to suppress (minimize) their impact and understand the diode features that are only associated with them. The study would result in an improvement in the device's quality since the material bulk and junction properties would be studied exclusively for various applications.

Interface states at the m-s contacts have been studied using *I–V* and *C–V* techniques. Even though studies have been ongoing for a long time, the complementary factor of the techniques has not been understood or explained. The interface states are responsible for diode electronic properties such as, series resistance, ideality factor, and Schottky barrier height. In addition, low-voltage capacitance peak and negative capacitance, among other parameters, have long been a source of contention and are still poorly understood. Though not providing detailed information about their origin, the parameters have been presented in terms of the interface states. The parameters have been observed on Yb/*p*-Si [27] and on metal-insulating-semiconductor (MIS) devices [6], without reporting their origins.

The negative capacitance is ascribed to the injection of minority carriers in the bulk of the semiconductor, which is the property of the ohmic-back contact [24, 28–30]. Wu et al., [31, 32], on the other hand, describe the parameter in terms of the interface charge at occupied states, contrary to Butcher et al., [33] where the capacitance is explained in terms of the instrument used to characterise samples. Later, the result presented by McPherson [34] indicated that the parameters are due to defects that are generated in the bulk of the material. The recent data acquired on heavily irradiated silicon diodes also showed a very large negative capacitance that could not be explained [35].

A low-voltage capacitance peak, on the other hand, was explained in terms of the charge accumulation in the low-voltage range [30, 36]. Studies on the interface, is therefore still necessary to fully understand the properties of the m-s contact devices and the formed interface states. A comprehensive explanation of the interface states based on complementary data from *I–V* and *C–V* techniques would result in the suppression of the interface states, allowing their properties to be studied solely through SCR. Currently, the suppression of the interface states is only achieved by operating the diode at high frequencies. Since the capacitance is also dependent on voltage, it is important to know a voltage range at which the capacitance is due to the interface states.

In this work, the electrical properties of an Al/*p*-Si Schottky diode fabricated by the deposition method are studied by *I–V* and *C–V–f* techniques at room temperature. The data are analysed to obtain the ideality factor, Schottky barrier height, saturation current, and series resistance, parameters that are used to generate the energy distribution profile of the interface state density of the structure. The charge of the interface states has been used to explain a low-voltage capacitance peak, a feature that has been outstanding though m–s contact devices have been studied for so long. In addition, a lack of interface state response at low-frequency capacitance measurements of the devices is explained in this work. According to the best of our knowledge, the ordering of the interface state charge in equilibrium with the semiconductor and with respect to SCR is explained for the first time in this work. This work is important for junction-based devices where the interface states are inevitable and affect the performance of the devices for various applications.

2 Experimental details

One sided polished *p*-type Si (doped with boron) purchased from Semiconductor Wafer; Inc was used to fabricate the Schottky diodes. Using *I–V* and *C–V* techniques, the diodes have been characterized in a dark environment and at room temperature. The meters for the measurement of current and capacitance have been built in-house, and they rely on software to carry out their respective functions. A precise contact between the probe and the diode is identified by expanding the diode under a microscope. Furthermore, the test diode is kept in a test fixture for a voltage sweep during the measurements. A metallic shield is used to cover the test fixture to isolate the measuring system from external electromagnetic fields. The *I–V* measurements were taken from − 4.00 to 4.00 V to allow the tunnelling charge carriers to surpass the thermionic emission carriers. *C–V* measurements, on the other hand, were taken in reverse bias from 0.00 to − 4.00 V at different frequencies ranging from 1.00 to 220 kHz. The

measurements were unstable at frequencies outside the range. The layout of the fabricated diodes is shown in Fig. 1, and their fabrication process is detailed elsewhere [37] and would not be repeated here. Si was chosen in this study because, as an elemental semiconductor that has more advantages than other semiconductors in industrial applications, its surface is easily oxidized, resulting in a considerable interface state density, that affects the electrical properties of the junction-based devices.

3 Results and discussion

Figure 2a presents the forward and reverse bias I–V characteristics of the Al/p-Si Schottky diode on a semilogarithmic scale. The analysis in the figure is to show that the diode is well fabricated with acceptable parameters to generate the trend of interface state density in order to investigate the unexplained parameters. The current increases linearly with voltage at low forward voltages, but it deviates from linearity as the voltage increases due to the possible formation of an oxide layer on the Si surface, resulting in series resistance [5]. As a result, interface states are created between the layer and Si [16–19]. The diode current (I) is then given in terms of the applied voltage (V) [16] as.

$$I = I_s \left[\exp\left(\frac{q(V - IR_s)}{\eta kT} - 1\right)\right] \quad (1)$$

and

$$I_s = AA^*T^2 \exp\left(\frac{-q\phi_B}{kT}\right), \quad (2)$$

where A (= 2.83× 10^{-3} cm^2) is the diode active area, A^* (= 32.00 A cm^{-2} K^{-2}) is the effective Richardson constant for p-type Si [17], T is the temperature in Kelvin, k is the Boltzmann constant, q is the electronic charge, and ϕ_B is the zero Schottky barrier height. The ideality factor, η,

$$\eta = \frac{q}{kT}\left[\frac{dV}{d\ln(I)}\right] \quad (3)$$

is determined from the slope of the linear region of the forward bias ln (I)–V characteristics at $V > 3kT/q$. The evaluated values of η and ϕ_B of the diode are 2.52 and 0.61 eV, respectively. η greater than unity has also been reported on similar devices, and it is due to the voltage drop across the interfacial layer between the metal and the semiconductor [17, 18, 26]. The high value of η suggests the involvement of additional diode conduction mechanisms, such as tunnelling conduction mechanism, alongside the thermionic emission mechanism. The ϕ_B of 0.61 eV is the same as that evaluated before [19] on Ti/p-Si Schottky barrier diodes. Even after etching Si wafers with HF solution, a native oxide layer 1 – 3 nm thick is always found on the surface [38]. The interface layer is formed either during material preparation or during the device fabrication process. The values of η and ϕ_B evaluated in this work are, however, consistent with those reported in the literature for similar diodes, indicating that the diode is well fabricated.

The double logarithmic I–V plot presented in Fig. 2b is used to study the conduction mechanisms of the fabricated Al/p-Si Schottky diode. The current and voltage are related as $I \propto V^m$, where m is the slope of each region. The slopes identified from the plot are 1.19, 1.34, and 1.54 for regions i, ii, and iii (region i: $0.01 < V < 0.12$ V, region ii: $0.13 < V < 0.71$ V, and region iii: $0.72 < V < 4.00$ V), respectively. The slopes of regions i and ii are close to unity, suggesting that the regions are dominated by ohmic conduction mechanisms. In these regions, the effective density of the injected carriers is less than the thermal carrier density [15]. In the last region, the conduction is dominated by the space charge-limited current (SCLC) mechanism, showing that the density of injected free carriers is greater than that generated by temperature [39].

The values of R_s, η, and Φ_B are calculated using Cheung's method and compared to those obtained from the thermionic emission theory. According to

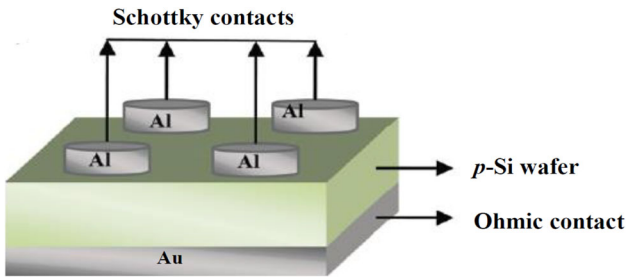

Fig. 1 Schematic diagram showing Al/p-Si Schottky diodes with circular Schottky contacts (top surface) and ohmic contact (bottom)

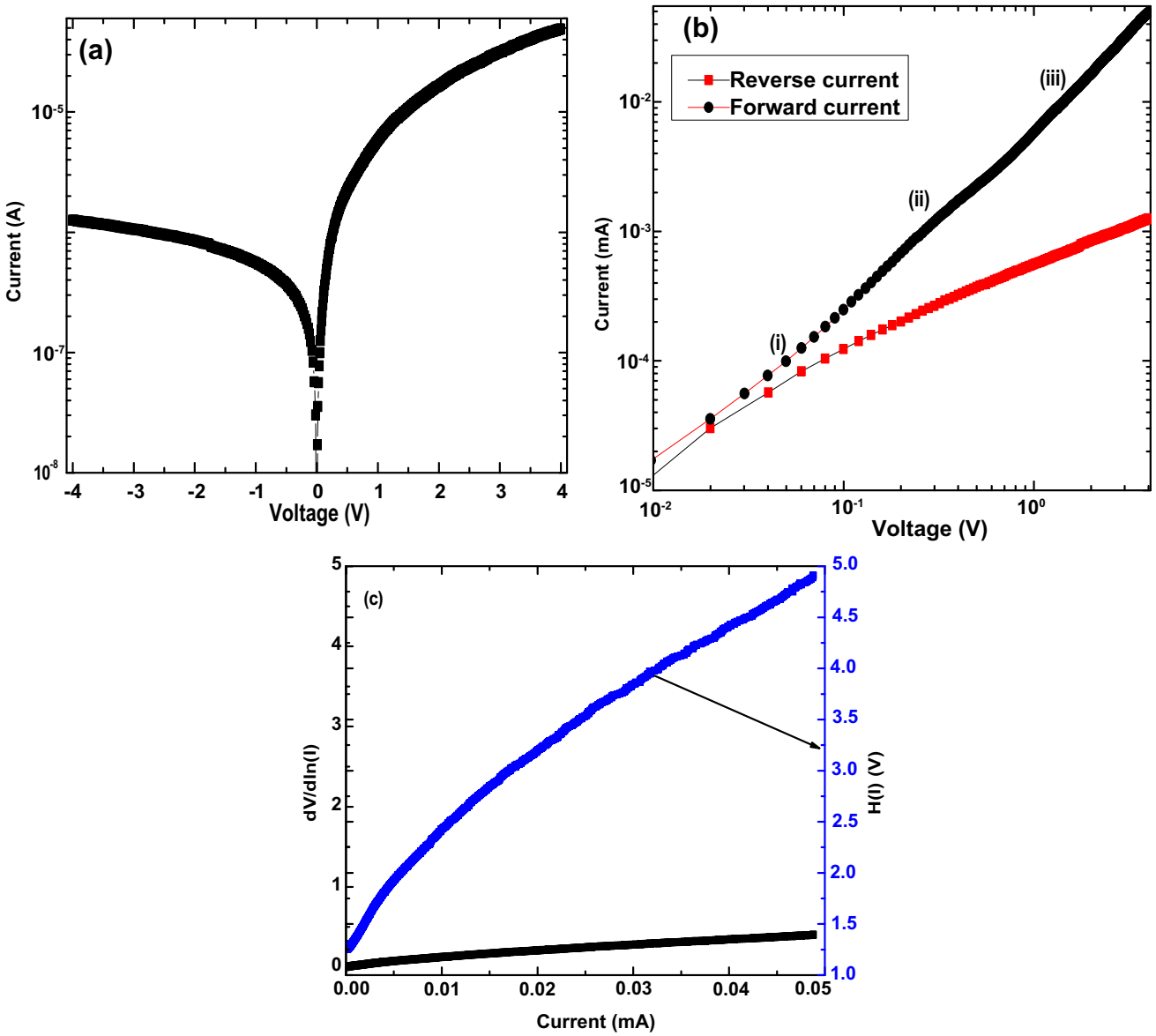

Fig. 2 **a** Forward and reverse bias semilogarithmic, **b** double logarithmic *I–V* characteristics and **c** dV/dln(I)-I and H(I)-I characteristics of Al/p-Si Schottky diode at room temperature

the Cheung's method, diode current is written [6; 21] as

$$\frac{dV}{d(\ln I)} = \left(\frac{\eta kT}{q}\right) + IR_s \tag{4}$$

$$H(I) = V - \left(\frac{\eta kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{5}$$

and $H(I)$ is given as

$$H(I) = \eta\Phi_B + IR_s, \tag{6}$$

where the IR_s term in the above equations represents the voltage drop across the diode's series resistance. As expected, the $\frac{dV}{d(\ln I)}$ - I and $H(I)$-I trends of Fig. 2c are linear, where the values of R_s and η are calculated from the slope and intercept of the $\frac{dV}{d(\ln I)} - I$ plot. The value of R_s is, 7.51 kΩ, greater than the 3.38 kΩ reported on Al/*p*-Si [40] and less than the 13.96 kΩ reported on Cu/*n*-Si [21]. The evaluated η is 1.92, greater than the 1.85 reported on Al/MEH-PPV/*p*-Si [41] but less than the 3.68 reported on Cu/*n*-Si [21]. The value of η obtained from Eq. (4) is inserted into Eq. (5) to obtain the $H(I)$-I plot, where the values of R_s and Φ_B are evaluated from the slope and intercept

of the $H(I)$-I plot, using Eq. (6). The value of Φ_B is, 0.80 eV, greater than the 0.75 eV reported before [41] on Al/p-Si but the same as the one reported on Al/MEH-PPV/p-Si [42] using the Cheung method, further confirming the presence of the layer between Al and p-Si. These parameters are within the range of those reported before, confirming that the diode is well fabricated. The parameters can, therefore, be used to generate a trend of interface state density to explain a low-voltage capacitance peak. Device parameters evaluated using thermionic emission and Cheung's methods are different (Table 1). This difference is attributed, among others, to the voltage dependence of the ideality factor and the Schottky barrier height due to the interface states [18] as

$$\eta = \frac{q}{kT}\left(\frac{V - IR_s}{\ln\left(\frac{I}{I_s}\right)}\right) \tag{7}$$

and

$$\phi_e = \phi_B + \left(1 - \frac{1}{\eta(V)}\right)(V - IR_s), \tag{8}$$

where ϕ_e is the effective barrier height. The dependence of η and ϕ_B is shown in Fig. 3. In this case, the ideality factor is greater than unity (2.52) and it is given [18] as.

$$\eta = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right], \tag{9}$$

where δ is the thickness of the interfacial layer, ε_i is the dielectric permittivity of the interfacial layer, ε_s is the dielectric permittivity of the semiconductor, W_D is the width of space charge region (SCR) and $N_{ss}(V)$ is the density of the interface states. The variation of the barrier height with voltage is attributed to the electric field present in the SCR and the change in the interface state charge. This variation of the charge with voltage is explained later in the text.

The energy of the interface states, E_{ss},(for p-type semiconductor) with respect to the top of the valence band, E_V, at the surface of the semiconductor is related to the applied forward voltage [6, 18] as.

$$E_{ss} - E_V = q\phi_e - qV. \tag{10}$$

The energy of the interface states against voltage and the energy distribution profiles of N_{ss} are presented in Fig. 4a and b, respectively. The interface states are biased-dependent due to the barrier inhomogeneities. The interface states are at the energy below the valence band at voltages higher than the zero Schottky barrier height, shown as region II in Fig. 4a.

It is interesting to investigate the interface states at $E_{ss} - E_V > 0$eV, where the voltage is lower than 0.67V, shown as the inset in Fig. 4b. The oscillation of N_{ss} trend at $E_{ss} - E_V$ between 0.59 and 0.67eV demonstrates that the majority carriers compensate interface states that have different reactivity at the energy above the intrinsic Fermi energy. The different reactivity is possibly due to a change in charge states with the applied voltage. This unusual trend of N_{ss} has not been explained in the literature, though observed before only on Au/n-GaN and Au/ZrO_2/n-GaN Schottky diodes [42]. The trend is now studied in terms of the interface charge in this work.

The trend in Fig. 4 seems complex. It is, however, interesting to interpret it in terms of the schematic diagram shown in Fig. 5. The diagram in Fig. 5a shows the energy band diagrams of the Al/p-Si structure with interface states between the interfacial layer and the Si interface. As shown in Fig. 5b the states are on the Si side of the SCR. To interpret the trend in Fig. 4b, five domains can be distinguished and discussed separately in Fig. 5b. These domains are used to explain a change in the interface state charge with the applied forward bias with respect to the zero Schottky barrier height. The charge-neutrality condition at the m–s interface is satisfied because the negative ionised acceptors are compensated by the positive majority carriers on the side of the semiconductor in the SCR [7]. As a result of this charge-neutrality, the interface state charge changes with bias to show that there is a polarisation in the interface states.

Domain (1): at the interface state energy range of 0.64 – 0.67 eV. At low forward voltage range of 0.06 –

Table 1 Device parameters evaluated using Thermionic emission and Cheung's methods for the fabricated Al/p-Si diodes

	Thermionic emission method			Cheung's method			
	ln(I)-V			$dV/d\ln(I)$-I		$H(I)$-I	
Al/*p*-Si	η	ϕ_B (eV)	I_s (μA)	R_s (kΩ)	η	R_s (kΩ)	Φ_B (eV)
	2.52	0.61	0.40	7.51	1.92	75.2	0.80

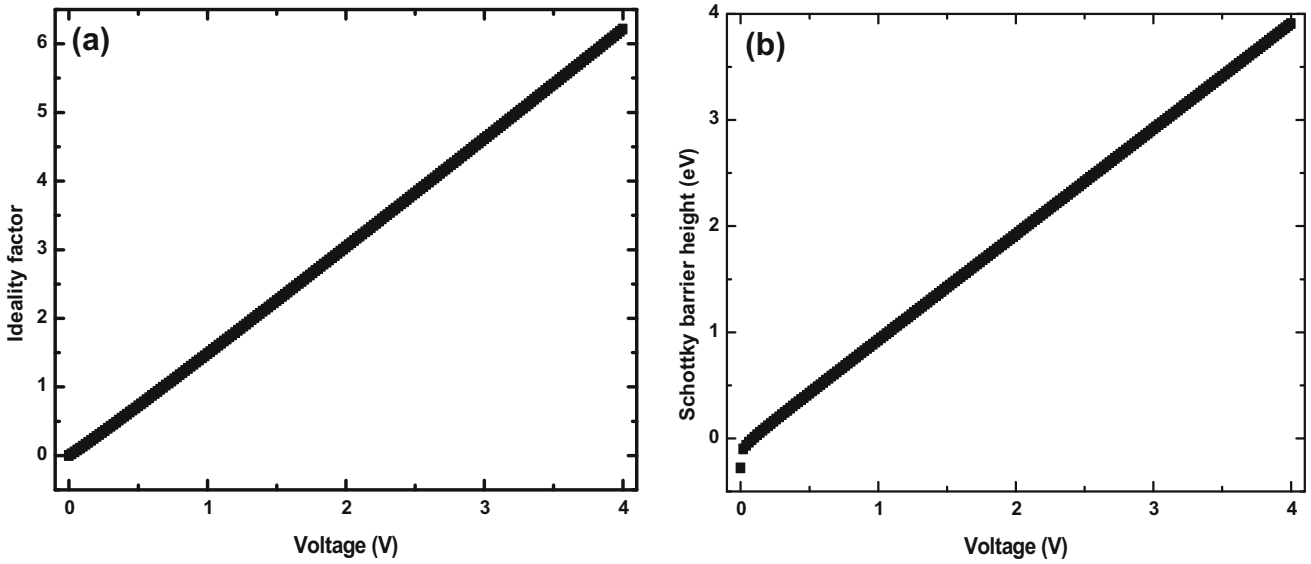

Fig. 3 **a** Voltage dependence of the ideality factor and **b** the Schottky barrier height of Al/p-Si Schottky diode at room temperature

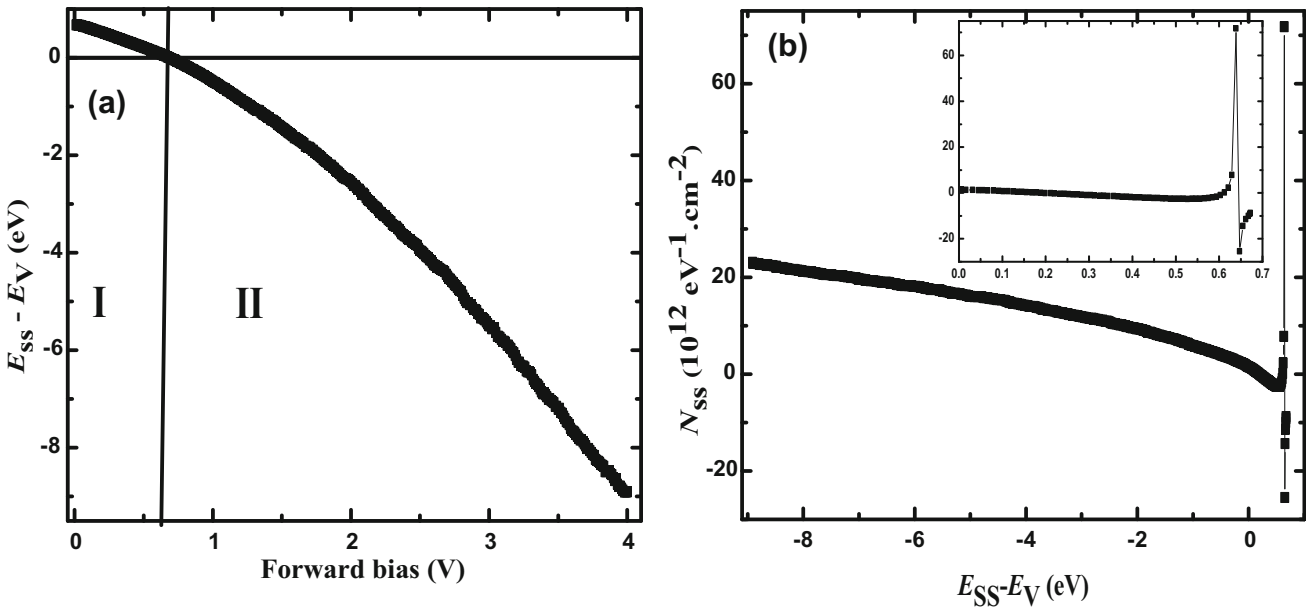

Fig. 4 **a** The energy of the interface states ($E_{ss} - E_V$) against forward bias (F_B). Two domains labelled I and II are distinguished which are studied in this article. **b** The density of interface states (N_{ss}) as a function of $E_{ss} - E_V$ obtained from the forward bias *I–V* data for Al/p-Si diode at room temperature

0.00 V, which is much lower than ϕ_B, where the charge of the interface states is dominated by metal electrons, resulting in a negative interface state charge. The high density of electrons could also be due to the minority carriers generated by temperature since it is at a voltage range lower than $3kT/q$, thermal energy.

Domain (2): at $E_{ss} - E_V$ (Forward bias) range of 0.59 – 0.64 eV (0.11 – 0.07 V), lower than φ_B, the interface state energy decreases and the charge of the states is positive because the majority carriers dominate and compensate the ionised acceptor in this region.

Domain (3): at $E_{ss} - E_V$ (Forward bias) range of 0.00 – 0.59 eV (0.67 – 0.11 V), slightly lower than the zero Schottky barrier height, the N_{ss} is constant at $\sim$ 0 $eV^{-1}.cm^{-2}$, indicating that a full interface state

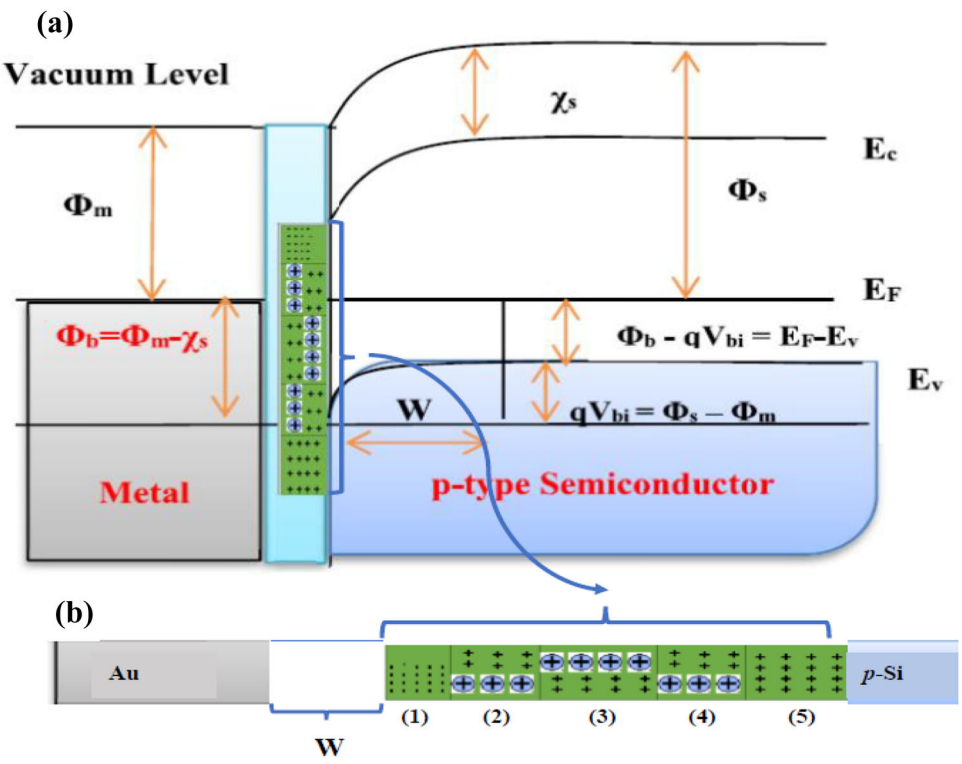

Fig. 5 **a** The energy band diagrams of Al/p-Si structure with interface states between interfacial layer and Si interface. **b** The interface states are located on the Si side of the SCR. Prior to the equilibrium, charge transfer between electrons (−), hole (+) and ionised acceptors(⊕) has taken place through interface

charge compensation by majority carriers is attained when the density of states is low.

Domain (4): at $E_{ss} - E_V$ (Forward bias) of 0 eV (0.67 V), slightly higher than the zero Schottky barrier height of the diode, the interface state energy is at the valence band edge and the charge of the interface state is neutral, indicating the densities of ionised donors and majority carriers are equal (full compensation), like in domain 3.

Domain (5): at $E_{ss} - E_V < 0.00\text{eV}$ ($F_B > 0.67\text{eV}$), higher than the zero Schottky barrier height, the N_{ss} increases gently from 0 at $E_{ss} - E_V = 0.00$ to $\sim 23.0 \times 10^{12}\text{eV}^{-1}.\text{cm}^{-2}$ at $E_{ss} - E_V = -9.00\text{eV}$. This increase confirms the existence of the interface states responsible for diode series resistance, as shown by the deviation of ln(*I*)-*V* plot at high voltages in Fig. 2a. In this region, the majority carriers are mobile, and freely contribute to the measured current. However, not, all majority carriers contribute to measured current since others compensate these interface states, resulting in the series resistance.

The fabricated Al/*p*-Si structure is characterised by *C*–*V*–*f* measurements at room temperature to further investigate the interface states formed in the SCR. Figure 6, the *C*–*V* characteristics of *p*-Si Schottky diodes, shows a rapid decrease in capacitance at low reverse voltages followed by a gentle decrease as the SCR attains its full depletion width. The presence of the interface states is confirmed by the capacitance peak at low voltages. Usually, the peak decreases with an increase in the measurement frequency [27, 43]. However, the opposite case is observed in Fig. 6a, where the peak is only observed at high measurement frequencies (> 50 kHz). The peak intensity increases with frequency and shifts gently

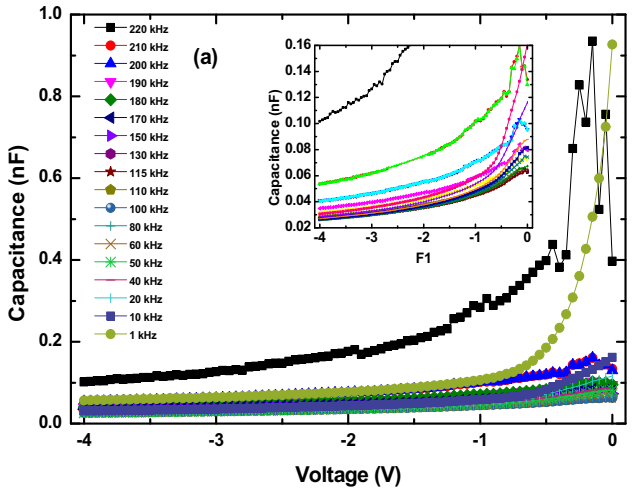

Fig. 6 *C*–*V* characteristics of the Al/p-Si Schottky diode for various measurement frequencies at room temperature

to higher voltages. This rare diode behaviour is explained by the interface state charge. The peak is not observed at low measurement frequencies because of the low-mobility majority carriers that are active to compensate for the negatively charged interface states in this frequency range. However, as the frequency increases, the capacitance is due to the negative charge interface states, electrons, since the majority carriers are inactive, hence the initial increase in the capacitance. The high density of the mobile electrons, results in negative charge states, so the capacitance increases with frequency. As the reverse voltage increases, however, the SCR extends from domain (1) to other domains in Fig. 5b, and the majority carriers are withdrawn from the SCR, resulting in a decrease in the capacitance. The low-voltage peak is therefore due to the negative interface state charge.

Figure 7a shows the plot of the capacitance-frequency measurements at various reverse voltages. A strong capacitance dependence on frequency is observed by its drastic decrease at low measurement frequencies for all voltages. This decrease confirms the existence of the interface states [44, 45], which are in equilibrium with the semiconductor as demonstrated in Fig. 5. The interface states follow the ac signal because the majority carriers are active to compensate for the relatively high mobility electrons at low frequencies. A well-known [27, 46] capacitance independence of frequency is observed at high measurement frequencies ranging from 20 to 150 kHz to show that the interface states do not respond to the ac signal in this range. The states do not respond to the frequency at this range possibly due to the full compensation of electrons by the majority carriers. As the frequency increases, however, the majority carriers become immobile because of their relatively low mobility, resulting in a high concentration of uncompensated electrons contributing to the diode capacitance. Figure 7a also shows the increase in capacitance at the highest frequency range. This capacitance is more pronounced for low-voltage trends because of the high density of electrons at low voltages as demonstrated by domain (1) in Fig. 5.

The variation of the interface state charge is explained in terms of the plot of the interface state density as a function of the reverse bias shown in Fig. 7(b). The plot is generated using the evaluated high- and low-frequency capacitance for each reverse voltage [46] as

$$N_{ss} = \frac{1}{qA}(C_{LF} - C_{HF}), \tag{11}$$

where C_{LF} is the capacitance at low frequency, which is the sum of the interface state capacitance and SCR capacitance and C_{HF} is the capacitance at high frequency. Since the C_{HF} is the SCR capacitance, the $C_{LF} - C_{HF}$ term in Eq. 11 is the interface state capacitance. The C_{LF} and C_{HF} was read at the maximum

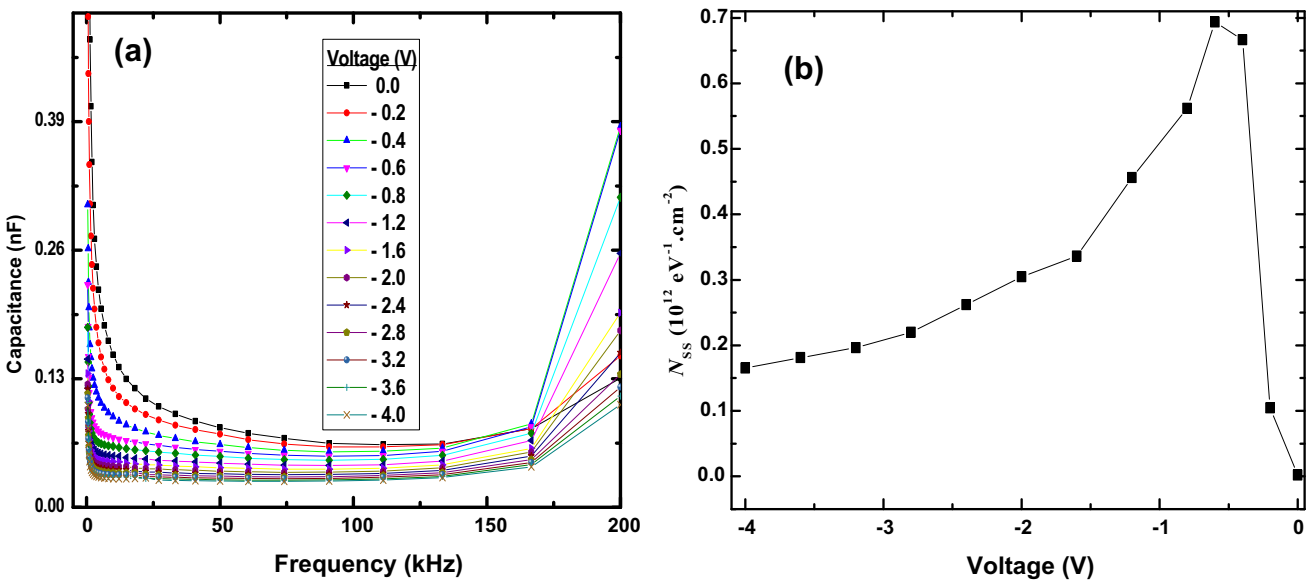

Fig. 7 **a** Experimental capacitance-frequency characteristics of Al/p-Si diode for different reverse bias at room temperature and **b** The density of interface states density (N_{ss}) as a function of reverse bias

capacitance and minimum capacitance, respectively, for the frequencies of 1 and 130 kHz. Since the reverse bias results in the widening of SCR as the majority carriers are withdrawn from the region, the variation of the voltage with the interface state density is used to analyse the interface state charge as the SCR width varies. It can be seen from Fig. 7b that at low reverse voltages, the majority carriers compensate the interface state charge before being withdrawn from the SCR, indicating that the SCR starts to be depleted at a reverse voltage of − 0.66 V. As a result, an increase in N_{ss} at low voltages in Fig. 7b indicates that the interface state charge at this region is negative, possibly due to the high-density electrons in the domain (1) of Fig. 5b. As the reverse voltage further increases, the interface state density decreases, indicating a decrease in the density of the electrons to be compensated as the majority carriers are withdrawn and SCR extends to other domains, hence an increase in SCR width after this domain. Though not well explained, the trend in Fig. 7b has previously been reported on Ni/*p*-GaN [46] and Au/PVA(B-doped)/*n*-Si [47] Schottky diodes. Figure 7b shows that the SCR width starts to be widened at 0.66 V, after the compensation of the negative interface state charge.

4 Conclusion

In this study, a well-fabricated Si-based Schottky diode is characterised using *I–V* and *C–V–f* techniques. The parameters evaluated are found to be consistent with those reported in the literature for similar diodes and are used to analyse the interface states at the *m-s* interface of the diode. As a result of different charges and its density, the interface states are in equilibrium with the material, due to electrons generated by temperature and those from metal contact, ionised acceptors, and the majority carrier holes. The energy, density, and charge of the states were found to change with forward bias. At voltages lower than the zero Schottky barrier height, the interface state energy is above the valence band and their density and charge states vary with the applied bias explaining the arrangement of the interface state charge. The density of the interface increases with voltages and their charge state is positive at the energy below the valence band (voltages higher than the zero Schottky barrier height). At the voltage range of 0.11 – 0.67 V, around the zero Schottky barrier height, the energy of the interface states is close to the valence band and their density is zero as the majority carriers compensate electrons to make the charge interface state neutral.

A capacitance peak and a change of its height with measurement frequency at low reverse voltages confirm the existence of these interface states and their charge states. At high frequencies, the negative interface states participate in the ac signal, resulting in an initial increase in the capacitance. The density of these negative charge states is high at low voltages, possibly due to the minority carriers. At low frequencies, however, the high density of majority carriers is active to compensate for these negative interface states. After charge compensation of the interface states, the SCR is varied (widened) at a reverse bias of − 0.67 V. As a result, for SCR properties derived solely from interface states, the devices should be studied at voltages greater than 0.67 eV.

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Author contribution

SJM: supervision, conceptualization, methodology, writing-reviewing, and editing. JOB:data acquisition.

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Data availability

The data presented in this study are available within this article.

Declarations

Competing interest The authors declare that they have no known competing financial interest or personal relationships that could have appeared to influence the work reported in this paper.

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