The origin of constant phase element in equivalent circuit of MIS (n) GaAs structures

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ABSTRACT

The Au/Pd/Ti-SiO₂-(n) GaAs properties have been analyzed via impedance spectroscopy (IS), as well as DLTS and ICTS, to identify the origin of electron processes responsible for existence of constant phase elements (CPE) in an equivalent circuits of that structure. We showed that CPEs connected in series with resistance represents the electron processes associated with deep levels in GaAs and/or interface states at SiO₂-(n) GaAs interface, depending on the value of n of CPE parameter. CPE with n close to 1 characterize the electron processes associated with EL2 deep level, and CPE with $n = 0.5$ – 0.65 the complex electron processes associated with EL3 deep level and interface states together. We stated that constant phase elements in equivalent circuits of MIS-GaAs structures with large frequency dispersion of electrical characteristics can be the result of more than one electron process.

1 Introduction

The metal–insulator–semiconductor (MIS) and the metal–oxide–semiconductor (MOS) structures are both the basic components of complex electronic systems and good tool for characterizing the insulator–semiconductor (I–S) interface properties of different materials. The use of MIS/MOS structures in electronics strongly depends on their I–S interface properties, which are determined by the localized electronic states (interface states) and semiconductor bulk states (deep states). It is well known that the high density of interface states prevent for a long time a fabrication of field effect devices based on III–V semiconductor compounds in 90s. However, since the beginning of the twenty-first century, renewed

interest in such devices has been observed [1–15]. It is associated with the development of new passivation technologies, the construction of new metal–insulator–semiconductor field effect transistors (MISFET), and a number of issues related to silicon device scaling [16–18].

In general, the MIS/MOS capacitance and conductance measurements, vs. gate voltage and frequency, can be used to characterize electron processes at the I–S interface and determination of interfacial parameters [19]. Unfortunately, these measurements cannot be simply used in MIS-GaAs systems because of many peculiarities observed in their electrical characteristics, including the large capacitance and conductance frequency dispersion,

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hysteresis effects, Fermi level pinning, and difficulties in recording high-frequency characteristics [20–23].

In systems with a large frequency dispersion of electrical characteristics, the impedance spectroscopy is widely used. The idea of IS is a measurement of a linear electrical response of system to a small AC signal varying over a wide frequency range, and the analysis of this response to obtain specific information about the investigated system [24]. The goal of the analysis is to find the simplest electrical circuit(s) (including resistance (R), capacitance (C), and inductance (L) elements, and eventually constant phase elements (CPE)) to describe the impedance system (i.e., the equivalent circuit). Such circuit(s) is applied for simulation of the physical phenomena occurring in the various areas of the system. The CPE has admittance defined as, $Y_{CPE} = Q_o(i\omega)^n$ where Q_o and n ($0 < n < 1$) are frequency independent. CPE is frequently used for phenomenological description of a system with a broad spectrum of time constants. Originally, it was used in electrochemistry to characterize solid-electrolyte systems. For analysis of MIS-GaAs systems it was proposed for the first time in the paper [25], wherein the authors attributed the CPE (with $n = 0.53$ – 0.57) to complex electron processes evoked by insulator-semiconductor interface states and calculated their time constants. A similar approach was applied in their later works as well [26–28]. It has been shown that impedance spectroscopy is a relatively simple as compared with other methods which employed very complex formulae to analyze experimental characteristics [29]. The equivalent circuits with CPE components are also used in analysis of other semiconductor-insulator systems, such as MIS AlGaIn/GaN [30] or FET AlGaIn/GaN [31], solar cells based on CdTe [32], CIGS [33–35], or CZTSe [36], and other NiO–SiO₂–Si [37], Au/n-CdS/p-porous GaAs/p⁺⁺-GaAs [11]. However, to date, there is no experimental data concerning the origin of the CPEs used in the equivalent circuits of those systems. Only preliminary results are presented in the paper [38].

Several well-established methods for determining the time constants of semiconductor electron states involve deep level transient spectroscopy (DLTS) [39–41] and isothermal capacitance transient spectroscopy (ICTS) [42]. These techniques are highly sensitive to both the bulk states and the interfacial states, and provide quantitative information about their energy, electron (hole) capture cross section,

and their density. The DLTS involves temperature scanning; therefore, some problems may occur when the parameters related to electron states are temperature dependent. The advantage of the ICTS is a constant measurement temperature and the fact that the values of the emission time constants are determined directly from the ICTS spectra.

The purpose of this work is to identify the source of electron processes responsible for the existence of constant phase elements in equivalent circuits of MIS-GaAs structures. The Au/Pd/Ti-SiO₂-(n) GaAs structure is investigated using impedance spectroscopy method, as well as ICTS and DLTS data, in order to identify the bulk states and insulator-semiconductor interface states in this system and determine their time constants. The parameters of the equivalent circuit and the time constants of the electron processes related to the frequency behavior of the MIS structure admittance are also assessed. Finally, the relationship between the time constants obtained from admittance characteristics and from transient capacitance spectra is analyzed.

2 Experimental

The Au/Pd/Ti-SiO₂-GaAs MIS structures with SiO₂ layers were obtained by a plasma-enhanced chemical vapor deposition (PECVD) process (SiH₄ with NH₃, N₂O, N₂, $p = 50$ Pa, 13.56 MHz, $T = 583.15$ K) in a GIR 200 ALCATEL apparatus). The n-type GaAs wafer with a doping concentration of $(1\text{--}4) \times 10^{22} \text{ m}^{-3}$ and crystallographic orientation of (100) was used as a substrate. No special treatment was applied to the GaAs surface prior to SiO₂ deposition. The wafers were cleaned with H₂SO₄ and successively rinsed with deionized water, trichloroethylene, acetone, and isopropanol with ultrasonic at all steps. The SiO₂ thickness was 0,16 μm , Au 150 nm, Pd 15 nm and Ti 15 nm.

The capacitance C and conductance G vs. frequency f (from 200 Hz to 5 MHz), at different gate voltages U_G (from -10 to 20 V) and temperatures T (300 K, 320 K, 340 K, 360 K, 380 K) were recorded using an Agilent 4294A precision impedance analyzer. The AC signal was kept at 25 mV. The SULA Technologies DLTS spectrometer with Temperature Controller 311 from Lake Shore Cryogenics was used for recording DLTS and ICTS spectra. The sample was placed on the cold finger in the liquid N₂

Cryostat Janiss VPF-700 connected to a vacuum pump. The DLTS scanning was performed with a heating rate of 0.2 K/s. The ICTS spectra were obtained by averaging 50 capacitance transients (measured under the same conditions). The DLTS and ICTS spectra were recorded at a low filling pulse amplitude (1 V), and with a 10 ms pulse duration. These parameters were carefully chosen in preliminary experiments, as suggested in [41].

3 Results and discussion

The capacitance vs. frequency (C - f) and normalized conductance vs. frequency (G/ω - f) spectra for different gate voltages at different temperatures are shown in Fig. 1. The broadened, unsymmetrical normalized conductance peaks are observed for all measured temperatures, and their positions depend on the gate voltage (i.e., higher voltage leads to peaks at higher frequency). Additionally, complex peaks are observed for some negative gate voltages at 360 K and 380 K. In general, the capacitance dispersion and the maximum of the normalized conductance occur

in the same frequency range, and a significant increase in conductance occurs at the high-frequency range.

The equivalent circuits displayed in Fig. 2 were used to fit the spectra (Fig. 1) using ZView 3.1c software. The (a) circuit was used for fitting the spectra recorded from 300 to 340 K, and (b) was used to fit the spectra at 360 K and 380 K. These circuits consist of insulator capacitance (C_{ox}), the capacitance of semiconductor space charge layer (C_{sc}), constant phase elements (CPE1 and CPE2), resistances (R_1 and R_2), series resistance (R_s), and inductance (L). All circuit parameters were free during the computation and were fitted simultaneously. The best fitting values of circuit parameters are presented in Fig. 3 and the calculated capacitance and conductance curves in Fig. 1. The estimated inductance $L = 0.3 \mu\text{H}$, resulting from the connection of wires in the measurement chamber, was also used in the calculations. The circuit parameters were fitted with errors under a few percent, and all the capacitance and normalized conductance spectra are very well reproduced by the model circuits, as shown in the Fig. 1. This fact, followed by monotonous dependence on the gate

Fig. 1 The Au/Pd/Ti-SiO₂(*n*) GaAs structure's capacitance, C , and normalized conductance, G/ω , vs. frequency, f , at different gate voltages, and temperatures, T , $\omega = 2\pi f$ (symbols, the

experimental data; solid lines represent the best fit of experimental data using the circuits from Fig. 2; fitted circuit parameters are presented in Fig. 3)

Fig. 2 The electrical equivalent circuits of the Au/Pd/Ti-SiO₂-(n) GaAs structure (C_{ox} insulator capacitance; R_s series resistance; L_s inductance; C_{sc} space charge layer capacitance; CPE1 constant phase element; R_1 resistance; CPE2 constant phase element; R_2 resistance)

voltage at different temperatures, confirm correctness of the equivalent circuits. Further, it means that their elements (i) can be associated with the physical phenomena occurring in the different regions of the investigated structure and (ii) can be used to calculate the appropriate parameters of these processes.

As expected, the C_{ox} is independent of the gate voltage, U_G (Fig. 3a). The series resistance, R_s , can arise from different sources (e.g., resistance of the semiconductor material, contacts, and/or electrical connection resistance [19]), and leads generally to increase of normalized conductance at high frequencies (Fig. 1). The CPE1, with $n_1 = 0.55$ – 0.65 , and CPE2, with $n_2 = 0.92$, in series with resistances, R_1 and R_2 , simulate the processes resulting in frequency dispersion of capacitance and conductance shown in Fig. 1. These processes are characterized by the time constants of $\tau_1 = (R_1 Q_1)^{1/n_1}$ and $\tau_2 = (R_2 Q_2)^{1/n_2}$ [43] presented in Fig. 4. A completely different dependence of τ_1 and τ_2 on the gate voltage suggests that

Fig. 3 Values of parameters of the equivalent circuits from Fig. 2, obtained at different gate voltages, U_G , and temperatures for the Au/Pd/Ti-SiO₂-(n) GaAs structure

Fig. 4 τ_1 and τ_2 time constants vs. gate voltages, U_G , at different temperatures, T , calculated using the Q_1 , n_1 , R_1 and Q_2 , n_2 , R_2 parameter values presented in Fig. 3

the nature of τ_1 is different from that of τ_2 . The τ_2 time constant is relevant for the electron processes evoked by deep levels (bulk traps, deep traps) [44] in GaAs. The admittance of monoenergetic deep traps is represented by a capacitor connected in series with resistance. The estimated value of $n_2 = 0.92$ shows the “capacitive” character of CPE2 (for a capacitor, $n_{CPE} = 1$), and suggests some distribution of these traps. The CPE1, with $n_1 = 0.55$ – 0.65 , can be attributed to the electron processes at the GaAs-SiO₂ interface region. According to the surface disorder model [45], there are localized electron states distributed in energy and in space at the semiconductor-insulator interface. The electrons are exchanged via tunneling between the semiconductor and those spatially distributed states. Their effective electron capture cross section exponentially decreases with tunneling distance, therefore, a large spectrum of time constants exists. As a consequence, a significant frequency

Fig. 5 **a, b** ICTS spectra recorded at different temperatures and gate voltages, U_G ; **c, d** DLTS spectra recorded at different time constants and gate voltages, U_G , for the Au/Pd/Ti-SiO₂-(n) GaAs structure

Fig. 6 **a, b** Deconvolution of ICTS spectra at selected temperatures, T , and gate voltages, U_G , into Gaussian components, α , β , γ , δ , and ϵ ; **c** deconvolution of the DLTS

spectrum at selected time constant, τ_e , and gate voltage, U_G , into Gaussian components A, B, C, D, E, and F for the Au/Pd/Ti-SiO₂-(n) GaAs structure

dispersion of MIS-GaAs capacitance and conductance is observed. In next, the time constants, τ_1 and τ_2 , are compared with data obtained from DLTS and ICTS spectra in order to verify the conclusions presented above.

The recorded DLTS and ICTS spectra at different gate voltages and temperatures (Fig. 5) display more complex behavior than the capacitance and normalized conductance data. They both contain a number of composite peaks; therefore, deconvolutions of the spectra were performed prior to further analysis. Some results obtained with Origin Pro 9.0 software using the Gauss function are shown in Fig. 6. The five peaks were identified in the ICTS spectra, two at low temperatures (α , β ; Fig. 6a), and three at high temperatures (γ , δ , ϵ ; Fig. 6b), and six peaks were found in the DLTS spectra (Fig. 6c), three below 225 K (A, B, C), and three at higher temperatures (D, E, F). In

order to determine the nature of these peaks, the evolution of the ICTS and DLTS spectra with gate voltage (pulse baseline) were performed, and the results are presented in Fig. 7. Since the behavior of the γ , ϵ , and A, C, and D peaks is clearly visible, an additional figure (Fig. 8) has been attached to highlight these peaks. Considering both figures, it is clear that the A, B, C, D, and F peaks positions, as well as the α , β , γ , and ϵ peaks, are not dependent on the gate voltage, but significant dependency of the δ and E peaks on U_G is observed. This fact suggests that the peaks A, B, C, D, F, and α , β , γ , ϵ are associated with deep level processes, whereas δ and E are attributed to insulator-semiconductor interface states. Continuous distribution of energy density in GaAs-insulator interface states is generally observed. Despite this fact, the sharp peaks in the DLTS and ICTS spectra

Fig. 7 **a, b** ICTS spectra at different gate voltages and selected temperature T ; **c** DLTS spectra at different gate voltages and selected time constant, τ_e , for the Au/Pd/Ti-SiO₂(n) GaAs structure

occur at high densities of interface states for the “small pulse” conditions, as shown in [41].

Based on the time constant values obtained from the ICTS and DLTS spectra, the Arrhenius analyses were performed. The activation energy ($E_c - E_T$) and electron capture cross section (σ_n) of deep traps were estimated. An effective value of $\gamma_n = 1.9 \times 10^{24} \text{ m}^{-2} \text{ s}^{-1} \text{ K}^{-2}$ was used for these calculations [46], and the exemplary plots are presented in Fig. 9. The energy and capture cross section values obtained at different gate voltages have been averaged and summarized in Table 1. The trap densities (N_t) were estimated with typical formulae for DLTS [46] and ICTS [47], and are also presented. The Arrhenius plot analysis was not performed for the ϵ and F peaks, because of the dependence of these peaks amplitudes on temperature and time constant, respectively. Such tendencies suggest the further capture cross section's dependence on temperature [48, 49], which is a basic limitation of Arrhenius analysis. A similar problem

was identified in the case of interface states associated with δ and E peaks.

Similar values of capture cross section and activation energy for α and B, β and C, and γ and D levels (Table 1) suggest their common nature. For this reason, no differences between the similar levels (identified in ICTS and DLTS spectra) will be discussed, and different labels will not be used. The A level has no equivalent in the ICTS data because its time constant is out of the range of the method, regardless of the temperature. Comparing the calculated deep level parameters with literature data, it was found that all levels are associated with point defects, which are typical for GaAs. The A, B, C, D, and F levels corresponding to electron traps, EL9, EL6, EL5, EL3, and EL2 defects, respectively [50–55]. The origin of the EL9 level was not specified because this information was not determined. It is worth noting that the nature of the F level was deduced, despite the lack of its parameters. It was stated that the

Fig. 8 **a** γ and ϵ ICTS peak position dependence on gate voltage, U_G , at selected temperature, T ; **b** A, C, and D DLTS peak position dependence on gate voltage, U_G , at selected time constant, τ_e , for the Au/Pd/Ti-SiO₂(n) GaAs structure

temperature-dependent position of the F peaks corresponds to the EL2 level, although this trap is generally a difficult to investigate. A strong dependence of the capture cross section on the temperature, high concentration (comparable to dopant concentration), heterogeneous distribution in the semiconductor, and presence of deep levels with similar activation energies, prevents the use of standard methods of analysis (also for DLTS) and is a source of results discrepancies in the literature [54]. For example, the activation energy of the EL2 trap changes from 0.58 to 0.83 eV, depending on the determination method used [54].

In order to ascertain the frequency and temperature ranges in which the identified deep levels

Fig. 9 **a** Arrhenius plots of α , β , and γ levels identified in ICTS spectra at selected gate voltage, U_G ; **b** Arrhenius plots of A, B, C, and D levels identified in DLTS spectra at selected gate voltage, U_G , for the Au/Pd/Ti-SiO₂(n) GaAs structure

contribute to the impedance spectra in Fig. 1, the frequency responses of these traps were calculated (Fig. 10). The frequency responses of the EL3 and EL6 traps were obtained using the data from Table 1 and the equation, $f = 1/(2\pi\tau_e)$, where $\tau_e = (1/\gamma_n\sigma_nT^2) \cdot \exp((E_c - E_T)/k_B T)$ [46]. The τ_e values of the EL2 trap have been determined from the peak positions in the ICTS spectra recorded at different temperatures. The contributions of the EL5 and EL9 traps have not been considered due to their relatively low concentrations compared to others. As shown in Fig. 10, the EL2 trap should be present in the lower frequency range for the conductance spectra recorded at 360 K and 380 K (Fig. 1h, j), whereas the EL6 trap should appear in the upper frequency range for spectra recorded above 360 K (Fig. 1h, j). The EL3 trap contribution may appear in the lower and middle frequency range for

Table 1 Estimated deep levels parameters and corresponding literature data

Experimental data				Literature data				
	σ_n, cm^2	$E_C - E_T, \text{eV}$	N_t, cm^{-3}	Symbol	σ_n, cm^2	$E_C - E_T, \text{eV}$	Origin	Refs.
A	$(3.1 \pm 1.1) \times 10^{-15}$	0.23 ± 0.01	5.0×10^{13}	EL9	6.8×10^{-15}	0.225	No data	[50]
B	$(7.3 \pm 0.6) \times 10^{-14}$	0.34 ± 0.01	3.9×10^{14}	EL6	1.3×10^{-13}	0.35	AsGa – VGa or AsGa – VAs	[50]
C	$(9.1 \pm 2.2) \times 10^{-14}$	0.41 ± 0.01	1.1×10^{14}	EL5	$(0.5\text{--}2) \times 10^{-13}$	0.42	VGa – VAs	[50]
D	$(1.6 \pm 0.4) \times 10^{-13}$	0.57 ± 0.01	3.7×10^{14}	EL3	$(0.8\text{--}1.7) \times 10^{-13}$	0.57	VGa – VAs or GaAs – VGa – GaAs	[50]
F	–	–	–	EL2	Temperature dependent	0.58 – 0.83	AsGa or AsGa – IAs	[50–53]
α	$(1.2 \pm 0.2) \times 10^{-13}$	0.34 ± 0.01	5.8×10^{14}	The same as B				
β	$(7.1 \pm 1.0) \times 10^{-13}$	0.40 ± 0.1	1.7×10^{14}	The same as C				
γ	$(1.4 \pm 0.3) \times 10^{-13}$	0.56 ± 0.02	4.7×10^{14}	The same as D				
ε	–	–	–	The same as F				

V_{As} and V_{Ga} —arsenic and gallium atomic vacancies, As_{Ga} and Ga_{As} —substititlual atoms, I_{As} —arsenic interstitial atom

Fig. 10 Frequency response, f , of identified deep levels vs. temperature, T , for the Au/Pd/Ti-SiO₂-(n) GaAs structure (dashed lines, range of frequency measurement)

conductance spectra recorded below 340 K and above 340 K, respectively (Fig. 1f). However, only the EL2 trap is clearly visible in the specified range, visible in spectra recorded at -7.5 V and -5 V at 360 K, and -10 V, -7.5 V, and -5 V at 380 K. In the MIS equivalent circuits, the EL2 trap contribution is represented by the CPE2- R_2 branch. The comparison of time constants estimated from impedance data (τ_2 , Figure 4) with time constants of the EL2 trap obtained from ICTS spectra at 360 K ($\tau_{\text{EL2}} = 1.2 \times 10^{-3}$ s) and 380 K ($\tau_{\text{EL2}} = 3.0 \times 10^{-4}$ s), confirmed this fact. However, detailed analysis of the

Fig. 11 τ_1 and τ interface states time constants vs. gate voltage, U_G , at selected temperatures, obtained from impedance spectroscopy (open symbols) and ICTS data (filled symbols), respectively, for the Au/Pd/Ti-SiO₂-(n) GaAs structure

normalized conductance spectra shows that the influence of the other traps is present but not clearly visible. The increase of normalized conductance in the high-frequency range can be also related to the series resistance, R_s , with the influence of the EL6 trap. The contribution of this trap characteristics measured at 300 K has been observed also in the paper [38]. The asymmetrical broadening of the G/ω peaks (visible in Fig. 1) is associated with the influence of the EL3 trap, and this fact was confirmed by comparing the interface states time constants

obtained from ICTS data with the time constants calculated from impedance spectroscopy (τ_1 in Fig. 4), as shown in Fig. 11. The values of τ_1 have been determined using the Q_1 , n_1 , and R_1 parameters obtained at 360 K and 380 K. At these temperatures, the contribution of EL2 trap to the measured MIS capacitance and conductance spectra was separated in the CPE2- R_2 branch of the equivalent circuit. The significant difference of two orders of magnitude between the compared time constants suggests that τ_1 (of CPE1) is not a parameter describing the processes evoked by interface states, as it was previously interpreted, but rather, an effective parameter which characterizes the complex contributions of electron processes from both the EL3 trap and interface states. In fact, it means that the CPE1, with $n_1 = 0.55\text{--}0.65$, is an effect of the superposition of electron processes evoked by interface states and deep levels. In this case, the Q_1 and n_1 , and calculated on their basis τ_1 , are the parameters characterizing these processes together.

In general, the results showed that the constant phase elements in equivalent circuits of MIS systems with large frequency dispersions of electrical characteristics can represent by more than one electron process. Therefore, the use of single impedance spectroscopy for characterizing such systems can lead to incomplete information regarding the analyzed phenomena.

4 Conclusions

The aim of this study was to identify the origin of constant phase elements in equivalent circuits of Au/Pd/Ti-SiO₂-(*n*) GaAs structures. It has been shown that the frequency behavior of the capacitance and normalized conductance of the structure, measured over a wide range of temperatures and gate voltages, can be very well reproduced by an equivalent circuit with CPE1, with $n_1 = 0.55\text{--}0.65$, at all temperature range, and with the addition of CPE2, with $n_2 = 0.92$, at some (higher) temperatures. These elements, connected in series with resistances, R_1 and R_2 , determine the characteristic time constants of the electron processes (τ_1 and τ_2), leading to the frequency dispersion of measured capacitance and conductance. Based on their gate voltage dependence, τ_1 seems to be connected to the electron processes evoked by insulator-GaAs interface states, whereas τ_2 is

attributed to GaAs deep levels. The deconvolution of the complex ICTS and DLTS spectra revealed signals from five deep levels and interface states. Based on the activation energy and capture cross sections of these levels, it was associated with point defects typical for GaAs, including EL2, EL3, EL5, EL6, and EL9. Furthermore, the deep level represented by the CPE2- R_2 branch in the equivalent circuit of the structure has been identified as EL2 traps. A discrepancy between the interface states time constants obtained from ICTS spectra and those obtained from impedance spectroscopy (τ_1) was observed, demonstrating that the CPE1, with $n_1 = 0.55\text{--}0.65$, represents not only interface states, but also the complex electron processes evoked by interface states and EL3 levels together. Finally, it was shown that constant phase elements in equivalent circuits of MIS-GaAs structures with large frequency dispersion of electrical characteristics can be the result of more than one electron process. In this case, the Q_1 and n_1 of CPE1 as well as τ_1 are the effective parameters characterizing these processes together.

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