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REVIEW

Scientific complications and controversies noted in the field of CdS/CdTe thin film solar cells and the way forward for further development

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Abstract

Cadmium telluride-based solar cell is the most successfully commercialised thin film solar cell today. The laboratory-scale small devices have achieved ~ 22%, and commercial solar panels have reached ~ 18% conversion efficiencies. However, there are various technical complications and some notable scientific contradictions that appear in the scientific literature published since the early 1970s. This review paper discusses some of these major complications and controversies in order to focus future research on issues of material growth and characterisation, post-growth processing, device architectures and interpretation of the results. Although CdTe can be grown using more than 14 different growth techniques, successful commercialisation has been taken place using close-space sublimation and electrodeposition techniques only. The experimental results presented in this review are mainly based on electrodeposition. Historical trends of research and commercial successes have also been discussed compared to the timeline of novel breakthroughs in this field. Deeper understanding of these issues may lead to further increase in conversion efficiencies of this solar cell. Some novel ideas for further development of thin film solar cells are also discussed towards the end of this paper.

1 Introduction

Acceleration of photovoltaic (PV) research started from the early 1970s with the first oil crisis and CdS/CdTe hetero-junction solar cell became one of the major thin film solar cells under intense research. Out of the two materials from the II–VI family, intrinsic CdS is inherently an n-type semiconductor and CdTe can exist in both n- and p-type electrical conduction intrinsically. However, since the CdS/CdTe hetero-junction showed good rectification properties, CdTe was assumed to be p-type in electrical conduction to form a p–n junction rectifying device with its n-CdS partner. Therefore, all the experimentally observed results were analysed and interpreted as a simple p–n hetero-junction [1–8]. In parallel, theoretical calculations and simulations were also carried out for this solar cell assuming principles of p–n junction diodes [9–12]. This is a classic example of following the same ideas in scientific research without critically testing the existing wisdom.

By the end of the 1980s, the conversion efficiency of this device gradually entered into double digits and Britt et al. [13] in 1993 reported 15.8% for a laboratory-scale device. The development progress became slow, and it took nearly another decade to increase the efficiency only by 0.7–16.5% by Wu et al. [14]. In parallel to this scientific research, BP Solar initiated a scaling up process in the mid-1980s using electroplated CdTe and successfully manufactured 0.96-m^2 solar panels with an efficiency of 10.6% [15]. Although BP Solar was in the forefront of this technology, termination of this manufacturing work together with other solar energy activities around 2000 was a real setback for the development of CdS/CdTe solar cells. Although scientific research continued in academic and research institutes, the highest solar energy conversion efficiency was stagnated at 16.5% for another decade until ~ 2013.

While these solar cell development activities were taking place, electrical contacts to II–VI semiconductors were also

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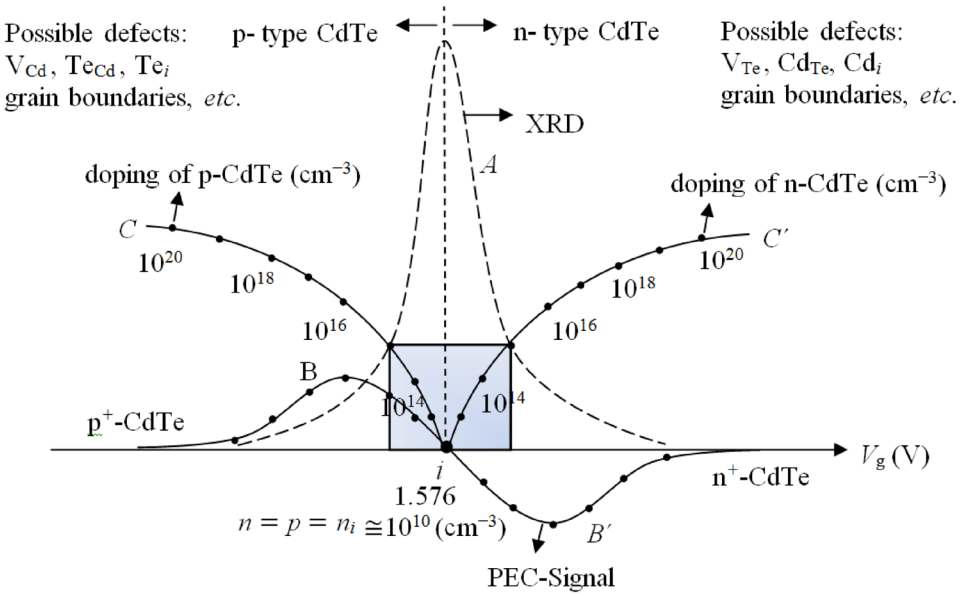

Fig. 1 Graphical presentation of the summary of the main results obtained for electrodeposited CdTe layers. The inversion point, V_i, produces stoichiometric and highly crystalline CdTe (curve A—the intensity of (111) XRD peak). The variation in electrical conduction type and doping concentration is shown by the curves BiB' and CiC', respectively. Electronic device quality materials can be grown in the shaded region, and possible native defects in both p- and n-CdTe thin films are also indicated in the two regions

progressed from mid-1980s [16–18]. Metal contacts to vacuum cleaved, air cleaved and chemically etched n-CdTe bulk materials showed a unique feature of Fermi level (FL) pinning at several experimentally observed defect levels [18]. Furthermore, the chemically etched and Cd-rich CdTe surfaces produced excellent rectifying diodes when compared to Te-rich CdTe surfaces [16]. Further work on polycrystalline CdTe thin films also showed similar behaviour and FL pinning at the same defect levels [19]. As a result of this work, an alternative device architecture of n–n + Schottky Barrier (SB) was proposed in 2002 [19] to describe the properties of TCO/CdS/CdTe/metal solar cells.

Around 2013, First Solar Company in the USA started to report rapid progress in the development of this device. The laboratory-scale efficiencies rapidly rose from reported 16.5 to ~ 22% in ~ 2017 [20–22] within a short period of 4 years. First Solar is now producing ~ 18% efficient solar panels becoming the largest thin film solar panel manufacturer in this field [23].

It is clear from the literature that the progress has been stagnated over a period of more than two decades before FirstSolar's achievements in the field and there are several areas needing research attention. There are also some scientific disputes in the published works on this technologically important device. The main aim of this review paper is to identify these areas so that future research can be focussed to improve the understanding of materials and device issues. A better understanding of these issues will lead to further development of CdS/CdTe-based solar cell.

2 Noted contradictions and areas needing research attention

2.1 Materials growth and characterisation

2.1.1 Stoichiometry and electrical conductivity of CdTe

The literature shows that there are several different growth techniques used for the growth of CdS layers. Most popular techniques are the chemical bath deposition (CBD), close-space sublimation (CSS), sputtering and electrodeposition (ED). For the growth of CdTe layers, there are about 14 different growth techniques [24], but the commercially successful methods have been CSS and electrodeposition (ED). First Solar Company is successfully using modified CSS to produce high-efficiency devices, and the manufacturability of ED-CdTe has also been successfully proven by BP Solar [15]. Because of the comprehensive research carried out by the authors of this article on electrodeposition of semiconductors, most of the examples given in this paper will be based on ED-CdTe thin films [25, 26], but the principles can also be applied to CdTe layers grown by other techniques.

The main results explored to date for electroplated CdTe are summarised in Fig. 1 [27]. An electrolyte containing Cd-ions and Te-ions can be used for electroplating CdTe thin films using either 2-electrode or 3-electrode systems and both methods produce key features shown in Fig. 1 [28]. Figure 1 summarises the variation in crystallinity (XRD), electrical conduction type (photoelectrochemical (PEC) signal), doping concentrations and possible defects as a function of the growth voltage (V_g). Since the redox potential (E°) with respect to hydrogen electrode, E° values for Te is + 0.59 V

and Cd is −0.40 V; the easiest element to electrodeposit is Te. At a certain voltage (V_i) for a given electrolyte, stoichiometric CdTe (Cd:Te = 1:1) is produced showing the highest crystallinity as shown by curve A. The curve A shows the variation in the intensity of the strongest XRD peak (111) of CdTe layers as a function of growth voltage, V_g. The V_i for this particular electrolyte is 1.576 V (for a 2-electrode deposition set-up), and this value changes according to the composition of the electrolyte and the number and nature of electrodes used. As shown by the curve BiB', produced using the photo-electro-chemical (PEC) cell results, the materials grown at V_g less than V_i are rich in Te and produce p-type CdTe. The layers grown at V_g greater than V_i are rich in Cd and produce n-type CdTe. Therefore, CdTe is a material that can be intrinsically doped during growth by changing the stoichiometry of the material. This intrinsic property is not only limited to electroplating but also should be valid for any CdTe growth technique. Curve CiC' indicates some possible doping concentrations as a function of growth voltage, V_g, and possible native defects are also indicated in Fig. 1, for two types of different CdTe layers. These trends have been observed and repeated numerous times by authors' group using different precursors in the ED bath. This phenomenon of variable conduction properties based on compositional ratio is eminent in CSS-grown CdTe too, as discussed in the later sections.

Since Te is the easier element to electrodeposit, it has been identified that Te-precipitation takes place at nanoscale, and this has been reported before for electroplated CdTe thin films [29]. Not only in ED-CdTe thin films, but also in CSS-CdTe thin films and melt-grown bulk CdTe, Te-precipitation has been observed [30–32]. This indicates that the Te-precipitation in CdTe is a natural feature and tends to produce p-type CdTe layers. As presented in later sections of this paper, n-type CdTe is more suitable for fabricating high-efficiency devices, and therefore, methods to prevent the formation of Te-precipitation should be established. Fernandez et al. [32] have shown that the incorporation of Ga removes Te-precipitates from CdTe. The positive effects of Ga incorporation on thin film CdTe solar cell efficiencies have been reported by Ojo et al. [33]. Though this is not particularly a controversy, yet related research on preventing Te-precipitation in CdTe layers should be encouraged to develop CdS/CdTe solar cells further.

2.1.2 Intrinsic and extrinsic doping of CdTe

Intrinsic doping of CdTe is described using Fig. 1, in the above section by changing the Cd and Te compositions in ppm level. Another method to improve the electrical conduction in CdTe is extrinsic doping by adding selected external dopants into the material. For example, group-III (B, Al, Ga, In, …) and group-VII (halogens—F, Cl, Br, I) elements are suitable n-type dopants for CdTe [34]. The positive results have been certainly observed with Ga and halogens (Cl, F and I). Similarly, group-I (Li, Na, K, Ag, Cu,…) and group-V (P, As, Sb, Bi,…) elements are suitable p-type dopants for CdTe [22]. The literature reports ~ 10^{13}–10^{15} cm^{-3} doping concentration for high-efficiency CdS/CdTe solar cells [13, 35–37]. Future research should be directed to increase these doping concentrations to ~ 10^{15}–10^{16} cm^{-3} to improve CdS/CdTe solar cell performance, and extrinsic doping can play a vital role here. But unfortunately, the self-compensation mechanism due to native defects is high in CdTe, and therefore, the addition of these dopants does not always behave according to solid-state physics principles. Therefore, extrinsic doping of CdTe, if necessary, should be carried out with thorough understanding.

2.1.3 Chloride treatment and defects reduction

Cadmium chloride treatment or the activation step is a well-known processing step to increase the efficiency of CdS/CdTe thin film solar cells [38–41]. Numerous publications are available on this treatment that includes the introduction of $CdCl_2$ on to the CdTe surface and heat treatment in air at an optimised temperature for optimised time period. After a suitable chemical etching, an electrical contact is deposited to complete the glass/TCO/CdS/CdTe/electrical contact, solar cell. The research community agrees on changes such as grain growth, defects removal, grain boundary passivation and interactions at the CdS/CdTe interface during this $CdCl_2$ heat treatment. As a result of this processing step, a drastic improvement in the device efficiency has been observed. However, the fine details of this processing step are not yet fully understood. More focussed research should be carried out in order to understand the fine details of these named areas.

The following section summarises the authors' work on "defects removal" in ED-CdTe thin films. Photoluminescence (PL) has been used in the past to identify defects in the material. However, due to instrumental limitations, most of the PL systems detect defect levels close to the band-to-band transitions. In our previous work [42], a wider energy range from (E_c–0.50) to E_v was explored for defects structure using PL. Figure 2 shows the PL spectra and the defect structure for as-deposited (AD) and $CdCl_2$ treated CdTe layers in this wide energy range. It is clear that the bandgap of AD-CdTe is full of defects and most of these reduce during $CdCl_2$ treatment. More importantly, the mid-gap defect level at ~ 0.74 eV is the most responsible one for recombination and generation (R&G) process within the devices and should be minimised or completely removed to increase the device performance. Future research should be focussed, on reduction or if possible removal of these defects completely. This is a major step to improve the device performance further.

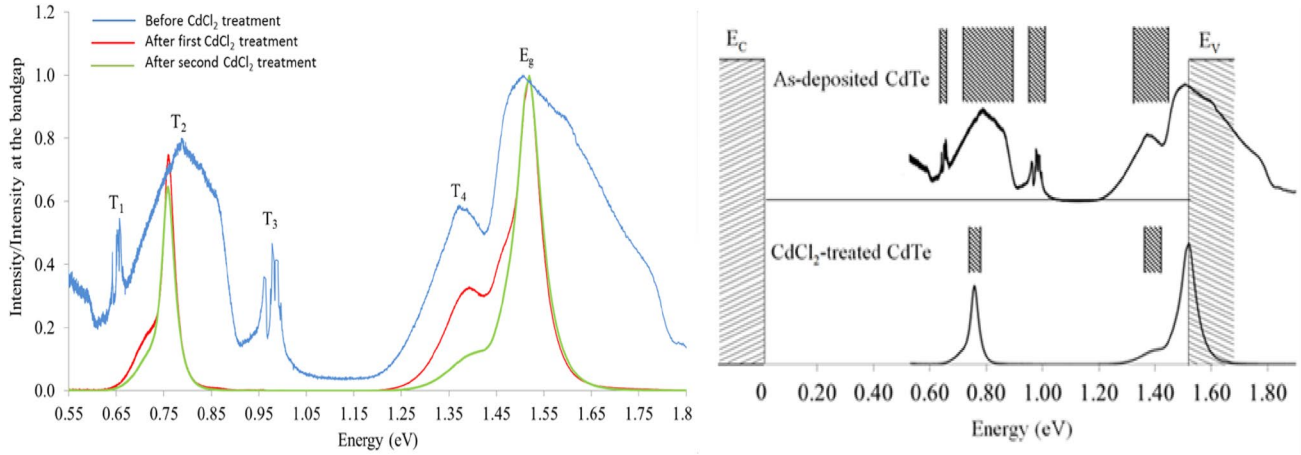

Fig. 2 PL spectra of as-deposited CdTe layers, grown from $CdCl_2$ precursor and the effects of subsequent $CdCl_2$ treatment in two steps [42], and the representation of defects distribution in as-deposited and $CdCl_2$-treated CdTe thin films. Note the drastic removal of defects from the bandgap of CdTe during $CdCl_2$ treatment

This work shows that the $CdCl_2$ treatment reduces a very broad mid-gap defects distribution to a comparatively narrow mid-gap defect level ~ 0.74 eV. The origin of these defects is not very clear, and these could be due to intrinsic defects or extrinsic defects due to inclusion of an unknown impurity into the crystal lattice. However, the PL work reported in ref. [17] for chemically etched CdTe surfaces indicates that these mid-gap defects level appears for Te-rich CdTe surfaces. This is helpful in drawing conclusions on mid-gap defects at ~ 0.74 eV that are mainly due to intrinsic defects. Since the surfaces are Te-rich, the possible native defects must be Cd-vacancies, Te-interstitials or Te-in Cd sites. Clearly, in order to remove this mid-gap defect level, CdTe should be grown with Cd-richness. According to the results reported in ref [17], mid-gap defects at ~ 0.74 eV are completely removed for Cd-rich CdTe surfaces. Therefore, without any doubt, high-efficiency CdTe solar cells will be produced when Cd-rich CdTe or n-type CdTe is used in CdS/CdTe solar cells.

2.1.4 Chloride treatment and positive contributions from grain boundaries

The literature also broadly reports the "grain boundary passivation" during $CdCl_2$ treatment. This needs deep investigations and understanding. Our preliminary thoughts were published before [27], and following is the summary of our current understanding of positive contributions from grain boundaries for the PV activity.

The secrets of $CdCl_2$ treatment and the involvement of grain boundaries after this treatment are the most interesting and need a deeper discussion. This needs consideration of both solid-state chemistry and physics principles. As reported in one of our publications [27], the melting point of pure CdTe crystal is 1092 °C. The reduction in the melting point of a material or a compound upon adding impurities is a well-established solid-state chemistry principle. During $CdCl_2$ treatment, the addition of numerous impurities on to the CdTe surface takes place. Some of these are namely excess Cd and Cl from $CdCl_2$, O from air annealing and also excess elemental Te deposited during growth. In addition to these, amorphous CdTe or crystallites of CdTe will be there in the grain boundaries. All the above impurities will drastically reduce the melting point of grain boundary materials to heat treatment temperature range of ~ 350–450 °C. Therefore, the grain boundary materials will melt into a liquid, while large CdTe crystals remain as solid material. This melting temperature has been identified as 385 ± 5 °C [27, 43] before, and suddenly the thin film becomes a collection of CdTe crystals floating on a thin film of liquid formed along grain boundaries. This is the main reason for the sudden collapse of the (111) XRD peak and appearance of other intense XRD peaks (220) and (311). The CdTe layers grown with (111) preferred orientation suddenly change due to floating of crystals in a liquid phase showing random nature of crystalline orientation, when heat treated and subsequently cooled down. After this process, most of the CdTe crystals extend across the thin film thickness showing columnar nature (Fig. 3a). During the heating, the liquid flows freely along grain boundaries due to convection currents and all elements mix up well, chemically react and excess elements could even evaporate from the liquid. Excess Cd from $CdCl_2$ and any elemental Te present can form CdTe compound [29] within grain boundaries and other elements present (Cl, O, etc.) dope this material to provide a certain electrical conductivity. Upon cooling, the CdTe crystals remain as solids, and the grain boundary material becomes a "melt-grown" material based on CdTe.

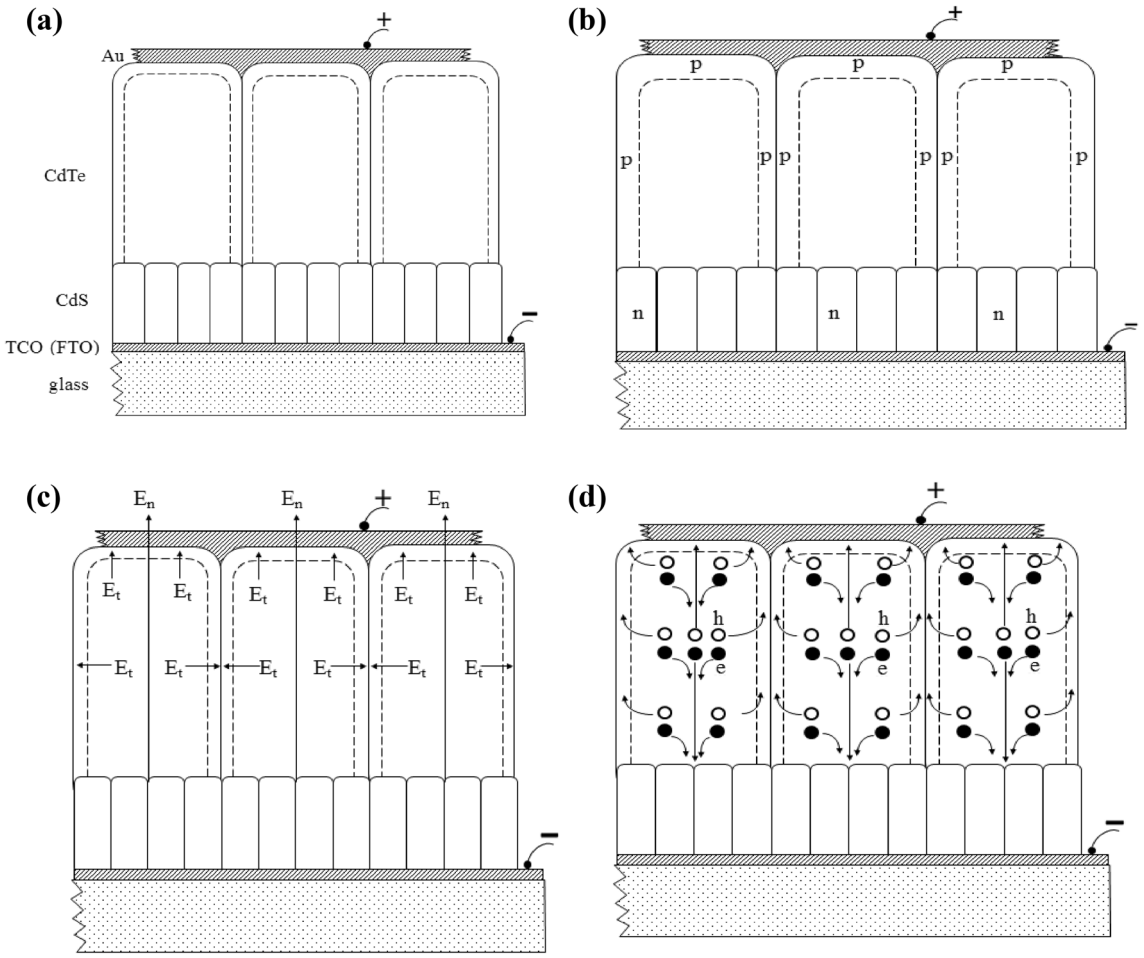

Fig. 3 Schematic diagram of **a** columnar-type n-CdS/n-CdTe solar cell; **b** doping effects on grains after $CdCl_2$ treatment in the case of n-CdTe layers; **c** creation of lateral electric fields (E_t) in addition to the main electric field (E_n) within the device; and **d** photo-generated charge carrier creation, separation and collection with high current densities along grain boundaries

To produce better solar cells, the grain boundary materials should solidify without forming any pinholes across the thin film. This certainly depends on the wetting properties of the composite material formed. Now, the two CdTe materials in crystals and in grain boundaries have different electrical conductivities and hence form lateral potential barriers as shown in Fig. 3b. This will happen with both n-type and p-type CdTe thin films and therefore establish lateral electric fields, E_t, along the crystal surfaces. Figure 3c shows the directions of E_t in the case of n-type CdTe thin films in addition to the main electric field of E_n across the solar cell. In this situation, photo-generated electron–hole (e–h) pairs are separated by two electric fields E_t and E_n. As a result, holes will mainly travel along the grain boundaries and electrons will travel in the opposite direction along the middle of CdTe crystals (see Fig. 3d). This motion has two advantages, minimising e–h annihilation and high mobility across the thin film normal to the TCO layer. Therefore, PV activity is enhanced with the positive contribution from grain boundaries. This is far beyond the grain boundary passivation and, in fact, enhancing the PV activity with the help of grain boundary activation effects. This type of PV activity will produce performance better than that of solar cells fabricated with epitaxial thin films. In this grain boundary activated situation, since photo-generated charge carriers are equal in number, the current densities along grain boundaries are much higher. The cross sections of grain boundaries surrounding the CdTe crystals are much smaller since they are simply "thin skin-like" boundaries. These high current densities along grain boundaries have been experimentally shown by two research groups using cross-sectional electron beam-induced current (EBIC) [44, 45], and one research group using Kelvin probe force microscopy (KPFM) [46].

With reference to the above discussion, it is now worth a comparison of two growth techniques: electrodeposition (ED) and close-space sublimation (CSS). ED is a low-temperature (< 100 °C) growth method, and CSS is a high-temperature (> 450 °C) growth technique. Therefore, the

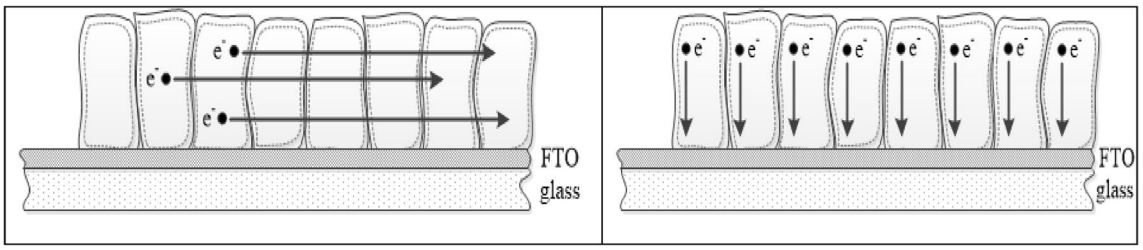

Fig. 4 Main difference in electron flows during Hall effect measurements and during the PV action of thin film solar cells. Because of the scattering from grain boundaries, usually reported $\mu_{||}$ can be few orders of magnitude smaller than $\mu_{\perp}$

as-grown CdTe layers are very different; ED materials have grains in the nanoscale, and CSS materials have grown in μm scale. Therefore, the $CdCl_2$ treatment for these two materials shows some differences. According to the above discussion, $CdCl_2$ treatment provides two major changes: (i) formation of large crystals in the μm-scale covering the whole thickness of the film and (ii) the formation and/or enhancement of the transverse electric field (E_t) across grain boundaries. During $CdCl_2$ treatment of ED-CdTe, both these properties are introduced, and hence, the effect is drastic. However, in the case of CSS-CdTe, high-temperature grown materials have already formed large crystals in the μm-scale. Therefore, $CdCl_2$ treatment introduces or enhances the value of E_t showing a comparatively lower effect. But still there is a positive effect from the $CdCl_2$ treatment.

2.1.5 Measurement of charge carrier mobility in CdTe thin films

The above understanding on $CdCl_2$ treatment invokes revisiting of charge carrier mobility measurements in thin film CdTe solar cell material. Usual mobility measurements along the thin films (i.e. parallel to TCO surface) yield charge carrier mobilities parallel to TCO ($\mu_{||}$) and therefore subjected to a large number of grain boundary scattering (see Fig. 4). Therefore, these values can be very small due to the columnar nature of CdTe grains. However, during the PV action, photo-generated charge carriers move normal to the TCO ($\mu_{\perp}$) surface. In the case of large grains extending from CdS to the back contact, charge carriers mostly travel within one crystal and grain boundary scattering is minimum or non-existent. Similarly, the opposite carriers travel through the melt-grown grain boundary material approximately normal to the TCO surface. Therefore, $\mu_{\perp}$ could be much larger than usually measured $\mu_{||}$ values. This difference could be even several orders of magnitude, and hence, future research should focus on methods to determine $\mu_{\perp}$ rather than $\mu_{||}$ values. These new mobility values will help in accurate theoretical simulations to predict maximum possible efficiencies with grain boundary-enhanced PV effect in CdS/CdTe system.

The above discussion has been limited only to CdTe material and its solar cells. However, the observation of the large body of scientific publications on almost all polycrystalline PV materials shows columnar growth of these material layers. In particular, the low-temperature grown materials like CIGS, kesterites and perovskite materials show columnar growth and these columns extend throughout the device thickness. Therefore, the reported mobility values ($\mu_{||}$) should be much lower than the real mobility values ($\mu_{\perp}$) applicable when the device is operating. For the same reason, the theoretical calculations carried out with $\mu_{||}$ should be revisited using more realistic $\mu^{\perp}$ values. Hence, the theoretical predictions for device efficiencies are expected to increase.

2.2 Electrical contacts to CdTe

A comprehensive study on electrical contacts to II–VI compounds (CdTe, CdS, ZnSe) has been carried out by the main author of this article, focussing on CdTe bulk materials. All three possible surfaces: vacuum-cleaved, air-cleaved and chemically etched surfaces have been used for fabricating electrical contacts and studying their properties. Main findings have been published in several papers and summarised in a review article published in 1998 [47]. Chemical etching is the relevant method for cleaning thin films and in thin film solar cell development. Therefore, it is appropriate to discuss the main features of these surfaces and electrical contacts fabricated on them.

2.2.1 Chemical etching of CdTe surfaces

Chemical etching of mechanically polished n-CdTe wafers clearly showed that the top layers can be easily modified by using chemical etchants. Acidic solutions preferentially remove Cd-element and leave a Te-rich surface. On the other hand, alkaline solutions preferentially remove Te-element and leave a Cd-rich surface. This chemical nature is identical for thin films of CdTe, and native oxides like TeO_2 and $CdTe_xO_y$ compounds are also usually found on these chemically etched surfaces.

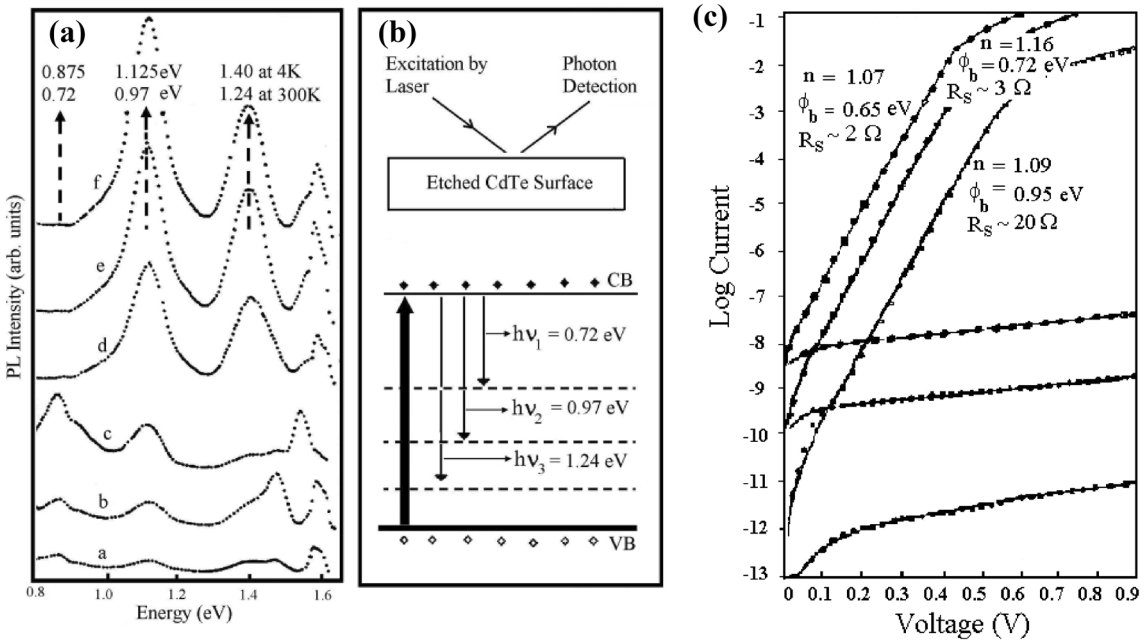

Fig. 5 **a** Photoluminescence spectra for chemically etched CdTe surfaces with Te-richness (a–c) and CdTe surfaces with Cd-richness (d–f), **b** electron transition process during PL measurements and **c** I–V curves of discrete Schottky barriers obtained from differently etched CdTe surfaces with the same electrical contact (Au)

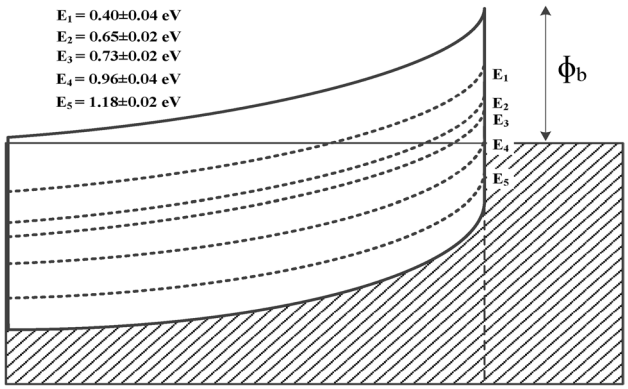

Fig. 6 Experimentally observed possible Fermi level pinning positions (E_1, E_2,…E_5) at n-CdTe/metal interface. E_1, E_2 and E_3 are dominant when the surface is Te-rich, and E_4 and E_5 are dominant when the surface is Cd-rich. Note that the formation of high Schottky barriers is possible when the CdTe surface is rich in Cd

The defect levels corresponding to these chemically etched CdTe surfaces have also been studied using PL measurements [17] (see Fig. 5). Five defect levels (E_1,…,E_5) have been identified as shown in Fig. 6, and E_1, E_2 and E_3 are dominant for Te-rich surfaces [47]. When the CdTe surfaces are produced with Cd-richness, E_1, E_2 and E_3 disappear and E_4 and E_5 become dominant defects (see Fig. 5a). These different properties obviously affect the properties of electrical contacts fabricated on them.

2.2.2 Fermi level pinning at n-CdTe/metal interfaces

The presence of high concentrations of defects at experimentally observed defect levels seriously affects the n-CdTe/metal contacts formed on chemically etched surfaces (see Figs. 5a and 6). A large number of metal contacts fabricated on these surfaces show the Fermi level pinning at one of these defect levels. Pinning position depends on the history of materials and the nature of the chemically etched surface. Te-rich n-CdTe surfaces tend to pin the FL at E_1, E_2 or E_3 producing Schottky barriers (SB) with low-potential barrier heights (E_c–E_1) ~0.40 (E_c–E_2) ~0.65 or (E_c–E_3) ~0.73 eV. Cd-rich n-CdTe surfaces show FL pinning at E_4 or E_5 yielding high-potential barrier heights (E_c–E_4) ~0.96 or (E_c–E_5) ~1.18 eV. When one of the defects has high concentrations, the SB formed is independent of the metal or the electrical contact material used. If the material used for the electrical contact induces drastic interface interactions, the barrier height could change due to the removal of FL pinning. In order to produce excellent rectifying contacts on n-CdTe surfaces, Cd-rich CdTe surfaces should be used with unreactive metals or electrical contact materials (see Fig. 5c). This FL pinning possibility introduces reproducibility issues for n-CdTe/metal interfaces. In summary, if large SBs with excellent rectifying contacts are desired, the n-CdTe surface should be prepared with Cd-richness and a non-reactive material like Sb or any other conducting material should be used (see Ref. [16]).

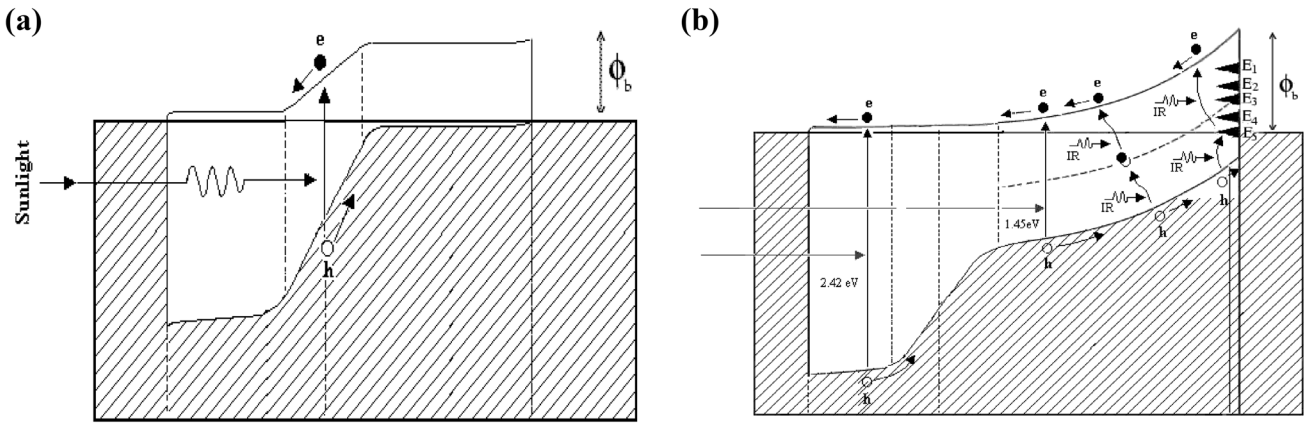

Fig. 7 Two possible device architectures for CdS/CdTe-based solar cell since intrinsic CdS is always n-type and CdTe can exist in both **a** p-type and **b** n-type electrical conduction

2.3 Device architecture

In order to analyse and interpret electrical characteristics of CdS/CdTe hetero-junction-based devices, scientists must know the electrical conductivity of both materials without any ambiguity. The case for CdS is very clear due to its inherent n-type nature. But CdTe can exist in both n- and p-conduction types very easily. As shown in Sect. 2.1.1, the electrical conductivity can be changed simply by changing its composition or stoichiometry in ppm level. This is therefore highly applicable to any CdTe growth technique, and slight variation in growth parameters can change its electrical conductivity type. Always considering CdTe as a p-type material and interpreting the device results assuming an n-CdS/p-CdTe solar cell has been a serious issue in the past, and therefore, knowing the correct device architecture is essential in interpreting the experimental results and developing this device further.

2.3.1 p–n configuration

Without any doubt, the formation of p–n junction takes place if the CdTe layer is grown with p-type electrical conduction. Since the CdTe layer can easily exist in both conduction types, researchers must test its electrical conductivity during device development research without making any "assumptions". Interpretation of the results highly depends on the device architecture. This is the main controversial issue in this field over the past few decades as most of the device outcomes have been always explained with simple p–n junction device architecture. Material studies of CdTe layers carried out by Shah et al. [48] using CSS growth showed that Te-rich CdTe results in p-type electrical conduction. But this research project is incomplete without testing Cd-rich CSS-CdTe. But to our knowledge, despite CSS being the most widely used technique, there is no published report on experimentally finding the electrical conduction type of CdTe layer used for CSS-grown PV device while explaining the device structure. If the material grown is indeed p-type, the CdS/CdTe hetero-junction is without doubt an n-p junction as shown in Fig. 7a, and the results can be interpreted and developed using this model.

2.3.2 n–n + SB configuration

If the CdTe layer is grown as n-type in electrical conduction due to variation in growth conditions, then the CdS/CdTe hetero-junction is an n–n-type weak rectifying contact. During the fabrication of metal contacts to n-CdTe, the FL pinning effects described as in Fig. 6 apply. To form a device with the highest slope or an intense internal electric field, the FL should be pinned at E_5 or forced to a place close to the VB maximum. In this situation, the device is an n–n + large SB at the back as shown in Fig. 7b. Now there are two rectifying interfaces: a weak rectifying junction at the n–n interface and a strong SB of ~ 1.18 eV at the back contact. These two junctions support each other adding currents, and therefore, the two junctions are connected in parallel. Since the SB is extremely large, even exceeding the potential barrier of CdTe p–n junction, and the whole device has a two-junction architecture, this device can perform better than the simple p–n junction. But unfortunately, optimisation of the device parameters by trial-and-error method, forming an n–n + SB device and then attempting to interpret the results using a simple p–n junction based on popular assumption, has been a real confusion in this field for several decades.

2.3.3 New experimental evidence for device architecture

In order to experimentally test the situation, we have grown a series of CdTe layers covering p-CdTe, i-CdTe and n-CdTe ranges as shown in Fig. 1. These layers have been treated in

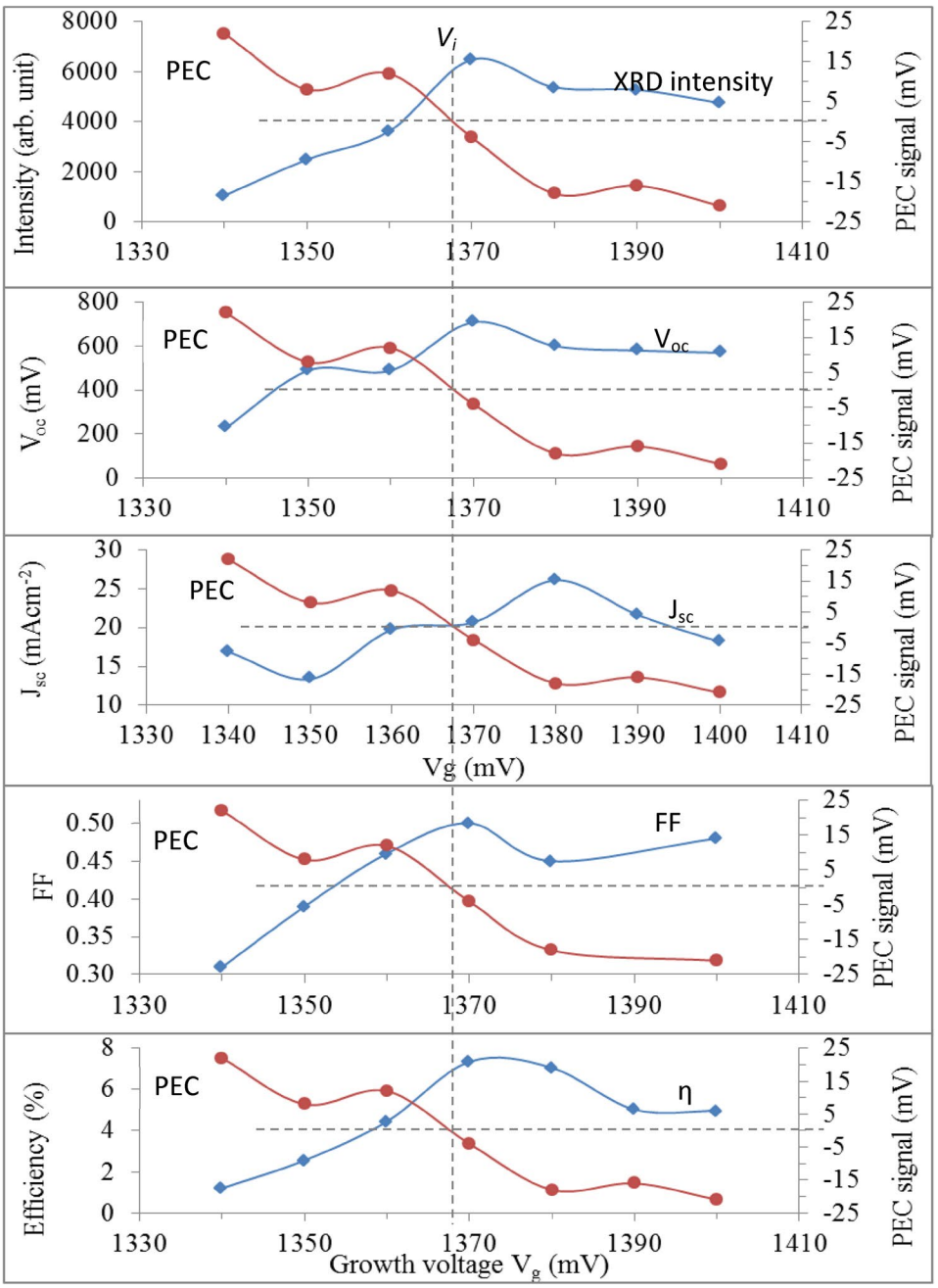

Fig. 8 Typical variation in the PEC signal (in red) for $CdCl_2$-treated CdTe is shown in each frame to separate the p-type and n-type regions. The positive PEC signal represents p-type CdTe layers and negative PEC signal represents n-type CdTe material. The intensity of (111) XRD peak is shown in the first frame indicating best crystallinity around V_i. The device parameters for glass/FTO/CdS/CdTe/Au solar cells fabricated with CdTe layers grown in the vicinity of the transition voltage, and $V_i = 1368$ mV are shown in the other four frames. Note that all device parameters are higher when the CdTe layers are rich in Cd and n-type in electrical conduction (Color figure online)

the same way, and devices were fabricated with the same electrical contact material. The device parameters, V_{oc}, J_{sc}, FF and η have been investigated in two recent series of experiments [49, 50]. Figure 8 shows the latest set of results [50], and both p-CdTe and n-CdTe layers produce PV active devices, but the high performance comes from n-CdTe layers. This experiment has been repeated, and the results are consistent [49, 50]. Therefore, the highest performing devices arise from n-CdTe layers, and the device architecture is n–n + SB for high-efficiency devices.

The device architecture shown in Fig. 7b was first published in 2002 [19] for high-performing CdS/CdTe solar cells, and the CdTe used in this device is reported as an n-type material. Soon after, in 2003, Jaegermann's group reported [51] a surprising result of n-CdTe solar cells producing highest efficiencies. Their comprehensive work on surfaces and interfaces investigated the CdS/CdTe solar cell efficiency as a function of the position of the Fermi level in CdTe. They obtained highest efficiencies with n-type CdTe and reported "This surprising result does not correspond to the accepted model of the device physics of the CdS/CdTe solar cell," i.e. the p–n junction model. More recently in 2013 [52] and 2015 [53], comprehensive works on both theoretical and experimental work by NREL group reported

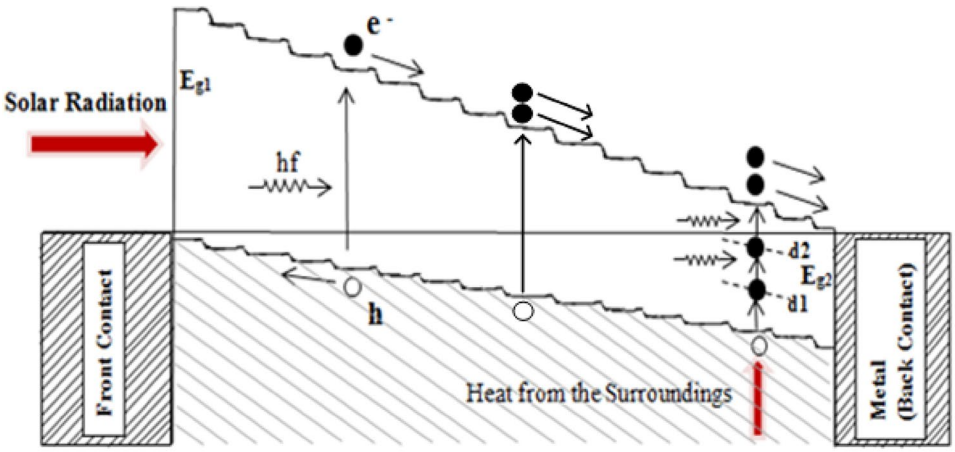

Fig. 9 Graded bandgap solar cell device which can benefit from band-to-band impact ionisation and the combination of impurity PV effect and impact ionisation to create more photo-generated charge carriers. Note that there are two photon inputs to such devices

that Cd-rich CdTe surfaces are more suitable for solar cell fabrication. Clearly, the Cd-rich CdTe material is n-type in electrical conduction, and therefore, the device architecture shown in Fig. 7b is more appropriate to describe the highest efficient CdS/CdTe solar cells.

2.4 High J_{sc} values

Short circuit current density (J_{sc}) values of CdS/CdTe present another scientific controversy in this field. Shockley & Quiesser (S&Q) have calculated the possible efficiency limit for one-bandgap, p–n junction with CdTe [54]. Loferski et al. [55] have also calculated the maximum J_{sc} values from one-bandgap CdTe p–n junction to be ~ 26 mA cm^{-2}. In these calculations, only the photons with energy greater than the bandgap of CdTe have been considered for absorption and creation of e–h pairs. Although S&Q publication clearly stated that this value can be increased by including several bandgaps to absorb other low-energy photons, PV community has been adamant to accept any J_{sc} values greater than ~ 26 mA cm^{-2} for novel devices incorporating CdTe and other bandgap materials. The J_{sc} values can be increased well beyond the above value due to enhanced harvesting of photons using several other mechanisms.

If a device is designed and fabricated to absorb all photons in the solar spectrum, J_{sc} can be increased to achieve ~ 54 mA cm^{-2} [56]. However, this cannot be achieved simply by adding consecutive material layers with smaller bandgaps, since the V_{oc} depends on the smallest bandgap material used in the device. Therefore, other mechanisms should be introduced or activated in order to harvest low-energy photons and create more photo-generated charge carriers.

2.4.1 Impurity PV effect

Impurity PV effect can be used by devices as shown in Fig. 9. These have large bandgap in the front, and bandgap value gradually reduces towards the rear of the device. In order to keep large V_{oc} values above 1.00 V, the smallest bandgap should be limited to ~ 1.40 eV. Then, the photons with energy less than the smallest bandgap used can be absorbed utilising native defects via multi-step absorption process or impurity PV effect. This is shown in Fig. 9, and this process can be used to absorb almost all photons available in the solar spectrum.

In addition, the heat from the surrounding can also contribute to the multi-step absorption process providing another input of photons to this kind of devices. All these processes contribute to the increase in J_{sc}, when the right conditions exist in this type of devices. When the multi-step absorption process is dominant, the recombination process is suppressed in such devices.

2.4.2 Impact ionisation

In the type of devices shown in Fig. 9, the probability of impact ionisation also increases and takes place via two different mechanisms. The photo-generated electrons in the front of the device accelerate towards the back contact and travel through smaller bandgap materials. When the electron achieves kinetic energy greater than the bandgap of the absorbing material, an additional e–h pair is created by band-to-band transition (see Fig. 9).

The second type of impact ionisation is more attractive and highly possible. Towards the rear of the devices, native defects are filled by infrared (I-R) photons coming from both the solar spectrum and the surroundings. The accelerating photo-generated electrons from the front will have enough energy to transfer trapped electrons from defect levels to the conduction band. This combined process of impurity PV effect and impact ionisation has a high probability of creating more charge carriers, and this will be an avalanche effect. Since both impurity PV effect and impact ionisation are built into this device, and with an additional input from

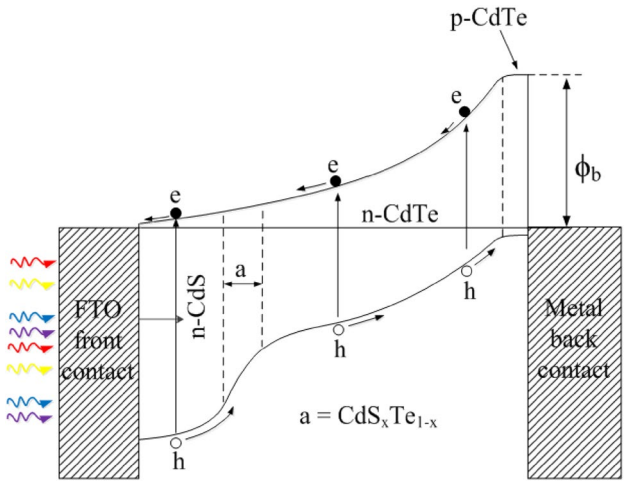

Fig. 10 Energy band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au thin film solar cell

the surrounding I-R radiation, the J_{sc} can achieve very high values beyond ~ 26 mA cm^{-2} for CdTe solar cells. There are many publications with high J_{sc} values, and First Solar has also reported 31.69 mA cm^{-2} for CdS/CdTe solar cells [57] which is certainly exceeding 26 mA cm^{-2}.

3 The way forward

As described in the above sections, CdS/CdTe solar cell development has been hampered due to a lack of understanding in both materials and device issues. Even the n–n + SB structure could suffer from reproducibility issues due to FL pinning at the back n-CdTe/metal interface. If the FL pins at E_5, when the CdTe is Cd-rich and n-type in electrical conduction, high-efficiency device is formed. If the FL pins at E_1, E_2 or E_3, mainly when the CdTe is Te-rich and p-type in electrical conduction, a low-efficiency solar cell is formed. This can only be avoided by forcing the FL to be placed close to the VB maximum, using additional methods. In our recent work, we have used a thin p-CdTe layer to remove FL pinning effect and improve the reproducibility effect as shown in Fig. 10. The laboratory-scale devices have shown 15.3% efficiency [58] from this device, and this type of approach can be used to further develop this device in the future.

3.1 Graded bandgap cells on p- and n-type windows

Next generation solar cells can be developed using multilayer graded bandgap structures incorporating many bandgap materials to harvest all photons available and introducing additional mechanisms such as impurity PV effect and impact ionisation within the same device [59, 60]. These can be produced starting from p-type and n-type window materials as shown in Fig. 11.

The main features of these devices are (i) presence of wide bandgap window material in the front, (ii) gradual reduction in the bandgap towards the back absorber material, (iii) slow change of electrical conductivity from p- to n- or n- to p-, and by keeping the smallest bandgap used at ~ 1.40 eV to achieve V_{oc} values above 1.00 V, when optimised. The devices fabricated on p-windows are more attractive to achieve high performance.

Solar cells based on wide bandgap p-window materials have several advantages. (a) Potential barrier height created depends on the bandgap of the p-window material, and therefore, internal electric field created is high for separation of e–h pairs, and high V_{oc} values are possible. (b) Photo-generated electrons in the front of the device accelerate across the device and see decreasing bandgaps towards the rear of the device increasing band-to-band impact ionisation. In

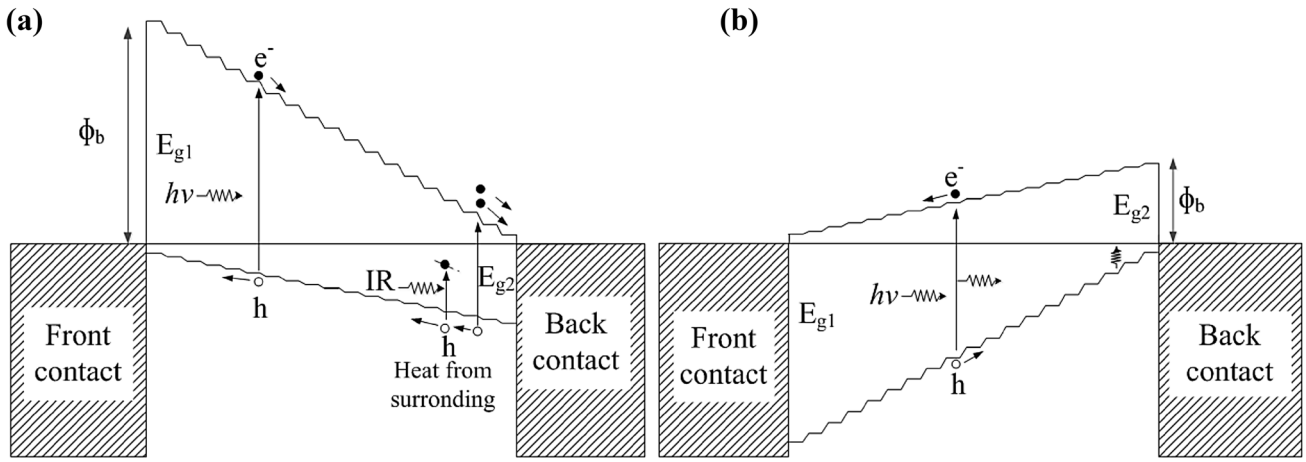

Fig. 11 Graded bandgap device structures **a** on p-type window material and **b** on n-type window material

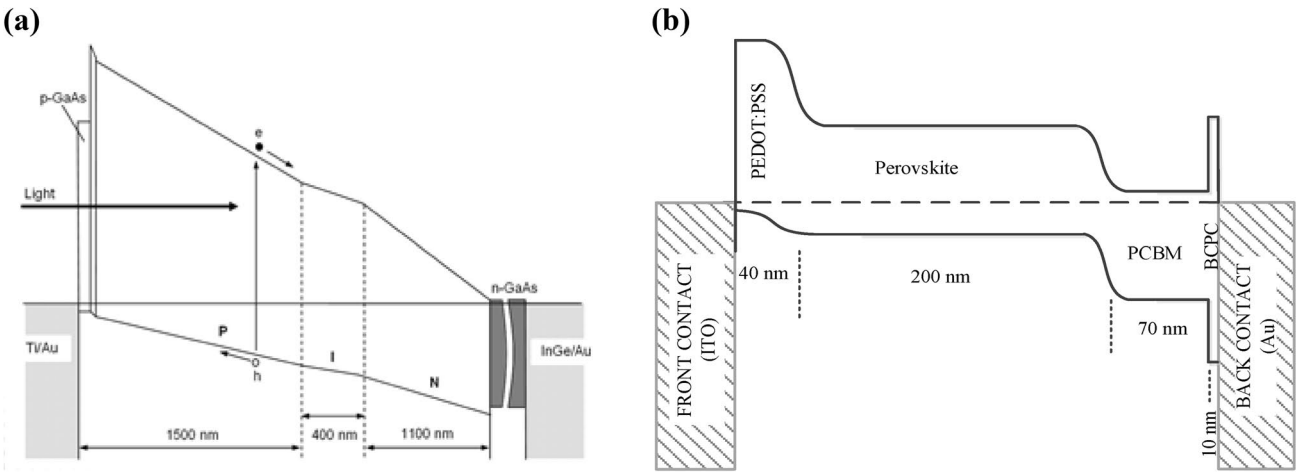

Fig. 12 Examples of graded bandgap devices based on p-type window materials using **a** GaAs/AlGaAs and **b** perovskite materials. Both devices have produced V_{oc} values greater than 1.10 V

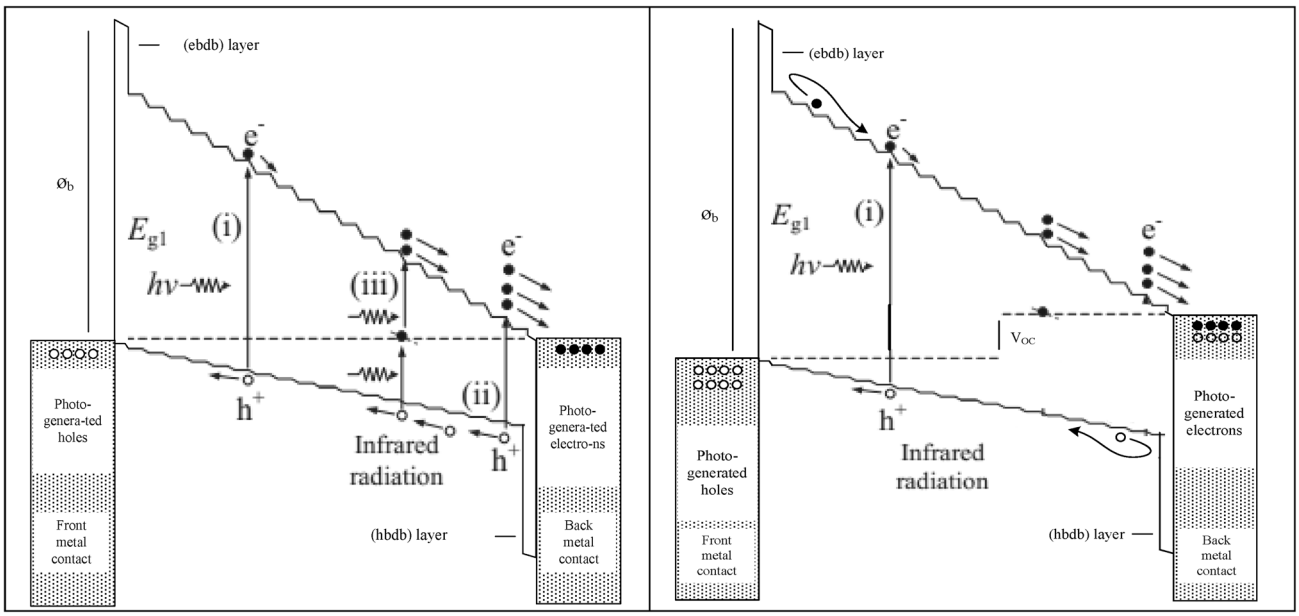

Fig. 13 Energy band diagram of a graded bandgap solar cell fabricated on a p-type window material in both short circuit and open circuit modes. Note the addition of (ebdb) layer and (hbdb) layer to enhance charge separation in the device

both cases, V_{oc}-limiting, smallest bandgap should be kept at ~ 1.40 eV to achieve V_{oc} greater than 1.00 V.

Two good examples of the above devices are now already in the literature [62–63]. The band diagrams of these two devices based on GaAs/AlGaAs [61] and perovskite solar cells [62, 63] are shown in Fig. 12. Both devices have p-type window materials in the front, and bandgap grading is achieved using several material layers. Both devices produce high V_{oc} and conversion efficiencies: V_{oc} ~ 1.175 and η ~ 20% for GaAs/AlGaAs [59] and $V_{oc} > 1.00$ V and $\eta > 20\%$ for perovskite solar cells [64].

3.2 Addition of ebdb and hbdb layers

Introduction of two additional layers, electron back diffusion barrier (ebdb) layer and hole back diffusion barrier (hbdb) layer as shown in Fig. 13 are extremely important to enhance the device performance of solar cells. This is shown in Fig. 13, for a graded bandgap device fabricated on p-window material, in both short circuit and open circuit modes. Photo-generated e–h pairs should be readily separated and transported to the electrical contacts at both ends of the device. However, the tendency is for separated

electrons and holes to recombine by any means. A p^+-layer (ebdb) allows holes to transport easily to the front contact but prevent electrons moving to the front contact. Therefore, the layer is accurately labelled as electron back diffusion barrier layer. Similarly, an n^+-layer (hbdb) allows electrons to transport easily to the back contact, but prevents holes moving in that direction. Therefore, the layer is labelled as hole back diffusion barrier layer. Instead of p^+ and n^+ layers for (ebdb) and (hbdb), highly resistive insulating layers can also be used, only if their thicknesses are low enough for charge carriers to tunnel through. These layers then act as pin-hole plugging layers, improving especially the thin film solar cell performance. Although this description is given in Fig. 13, for a graded bandgap device based on p-window material, use of ebdb and hbdb layers is identical for p–n, p–i–n or any other hetero-junction solar cell.

Therefore, considering the prospects of thin film solar cells based on p-type window layer and inclusion of ebdb and hbdb layers, scientific community should further be focusing on implementing these ideas for CdTe-based devices and other thin film solar cells. Authors' group has already conceptualised CdTe-based devices incorporating both of these ideas and aiming for further developments [65, 66].

4 Concluding remarks

Although CdS/CdTe hetero-junction-based solar cell has achieved ~22% efficiency for laboratory-scale devices and ~18% efficiency for modules, there are many areas that exist those required deeper understanding. Improving deep understanding through focussed research will help in further development of this solar cell, bringing the manufacturing cost further down. A summary of scientific complications and controversies discussed, and the ways forward for development of next generation solar cells are given below.

(a) The main controversy is the systematic determination of electronic conduction type of CdTe layers used in the highest efficiency CdS/CdTe solar cells instead of interpreting the outcomes relying on the popular assumption. Once the electronic conduction type is known, the relevant device architecture can be decided from the two possible situations, and then, the experimental results can be interpreted accurately and devices can be further developed according to solid-state physics principles.

(b) Te-precipitation in CdTe material is an inherent property that can be detrimental for the device and should be resolved using relevant methods during growth and device processing steps. Further research on this matter is essential.

(c) Charge carrier mobilities normal to the TCO layer ($\mu_{\perp}$) should be measured instead of mobilities parallel to the TCO layer ($\mu_{||}$). $\mu_{\perp}$ could be much higher than $\mu_{||}$ due to scattering from grain boundaries in the case of $\mu_{||}$ and therefore could make a huge difference in the simulation work on this device.

(d) In order to reduce the R&G process, the mid-gap defects in CdTe observed at ~0.74 eV should be minimised or completely removed. Extensive research attention is necessary in this front.

(e) The highest efficiency devices reported to date have CdTe doping concentration in the range ~$(10^{13}$–$10^{15})$ cm^{-3}. Research should be directed to increase this to ~$(10^{15}$–$10^{16})$ cm^{-3}, in order to achieve better performance.

(f) Next generation solar cells should be developed based on multilayer graded bandgap device structures. Therein, impurity PV effect and impact ionisation should be built into the same device to achieve the highest possible performance parameters.

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References

1. K.W. Mitchell, A.L. Fahrenbruch, R.H. Bube, Evaluation of the CdS/CdTe heterojunction solar cell. J. Appl. Phys. **48**, 4365 (1977)
2. R.N. Bhattacharya, K. Rajeswar, Heterojunction CdS/CdTe solar cells based on electrodeposited p-CdTe thin films: fabrication and characterisation. J. Appl. Phys. **58**(9), 3590 (1985)
3. T.L. Chu, S.S. Chu, S.T. Ang, Electrical properties of CdS/CdTe heterojunctions. J. Appl. Phys. **64**, 1233 (1988)
4. B.M. Basol, Processing high efficiency CdTe solar cells. Int. J. Sol. Energy **12**, 25–35 (1992)
5. S.K. Das, G.C. Morris, Preparation and characterisation of electrodeposited n-CdS/p-CdTe thin film solar cells. Sol. Energy Mater. Sol. Cells **28**, 305–316 (1993)

6. T.A.M. Fiducia, B.G. Mendis, K. Li, C.R.M. Grovenor, A.H. Munshi, K. Barth, W.S. Sampath, L.D. Wright, A. Abbas, J.W. Bowers, J.M. Walls, Understanding the role of selenium in defect passivation for highly efficient selenium-alloyed cadmium telluride solar cells. Nat. Energy **4**, 504–511 (2019)
7. S. Varadharajaperumal, M.S. Ilango, G. Hegde, M.N. Satyanarayan, Effect of CuPc and PEDOT:PSS as hole transport layers in planar heterojunction CdS/CdTe solar cell. Mater. Res. Express **6**, 095009 (2019)
8. H. Bayhan, E.T. Dağkaldıran, J.D. Major, K. Durose, M. Bayhan, Regimes of current transport mechanisms in CdS/CdTe solar cells. Semicond. Sci. Technol. **34**, 075013 (2019)
9. A. Bosio, G. Rosa, N. Romeo, Past, present and future of the thin film CdTe/CdS solar cells. Sol. Energy **175**, 31–4332 (2018)
10. M. Lingg, S. Buecheler, A.N. Tiwari, Review of $CdTe_{1-x}Se_x$ thin films in solar cell applications. Coatings **9**, 520 (2019)
11. A. Kuddus, M.F. Rahman, S. Ahmmed, J. Hossain, A. Bakar, M. Ismail, Role of facile synthesized V_2O_5 as hole transport layer for CdS/CdTe heterojunction solar cell: validation of simulation using experimental data. Superlattices Microstruct. **132**, 106168 (2019)
12. A. Niemegeersa, M. Burgelman, Effects of the Au/CdTe back contact on IV and CV characteristics of Au/CdTe/CdS/TCO solar cells. J. Appl. Phys. **81**(6), 2881–2886 (1997)
13. J. Britt, C. Ferekides, Thin film CdS/CdTe solar cell with 15.8% efficiency. Appl. Phys. Lett. **62**, 2851–2852 (1993)
14. X. Wu, J. C. Keane, R. G. Dhere, C. DeHart, D. S. Albin, A. Duda, T. A. Gessert, S. Ashar, D. H. Levi and P. Sheldon, 16.5%-efficient CdS/CdTe polycrystalline thin film solar cells, in *Proceedings of 17th European PVSEC* (2001), pp. 995–1000
15. D. Cunningham, M. Rubcich, D. Skinner, Cadmium telluride PV module manufacturing at BP Solar. Progr. Photovolt. Res. Appl. **10**, 159–168 (2002)
16. I.M. Dharmadasa, J.M. Thornton, R.H. Williams, Appl. Phys. Lett. **54**(2), 137 (1989)
17. Z. Sobiesierski, I.M. Dharmadasa, R.H. Williams, Appl. Phys. Lett. **53**(26), 2623–2625 (1988)
18. I.M. Dharmadasa, Recent developments and progress on electrical contacts to CdTe, CdS and ZnSe with special reference to barrier contacts to CdTe. Invited review paper. Progr. Cryst. Growth Charact. **36**(4), 249–290 (1998)
19. I.M. Dharmadasa, A.P. Samantilleke, N.B. Chaure, J. Young, New ways of developing glass/conducting glass/CdS/CdTe/metal thin-film solar cells based on a new model. Semicond. Sci. Technol. **17**, 1238–1248 (2002)
20. E. Wesoff, First Solar on the Future of Photovoltaics: Part 2. In order to thrive, First Solar must deploy 65 GW of photovoltaic panels over the next decade. Available online: http://www.greentechmedia.com/articles/read/First-Solar-on-the-Future-of-Photovoltaics-Part-2/. Accessed 20 March 2014
21. First Solar CdTe 18.7% Efficient cell breaks record. Compound semiconductor website. https://investor.firstsolar.com/news/press-release-details/2013/First-Solar-Sets-New-World-Record-for-CdTe-Solar-Cell-Efficiency/default.aspx
22. https://www.greentechmedia.com/articles/read/first-solar-hits-record-22-1-conversion-efficiency-for-cdte-solar-cell
23. http://www.firstsolar.com/en-EMEA/-/media/First-Solar/Sustainability-Documents/Sustainability-Peer-Reviews/CRSES2015_06_First-Solar-CdTe-Module-Technology-Review-FINAL.ashx
24. T.M. Razykov, C.S. Ferekides, D. Morel, E. Stefanakos, H.S. Ullal, H.M. Upadhyaya, Solar photovoltaic electricity: current status and future prospects. Sol. Energy **85**, 1580–1608 (2011)
25. I. M. Dharmadasa, *Advances in Thin-Film Solar Cells*, 1st edn-2012, 2nd edn-2018 (Pan Stanford Publishing Pte. Ltd, Boulevard, 2018)
26. A. A. Ojo, W. M. Cranton, I. M. Dharmadasa, Next generation multilayer graded bandgap solar cells. Monogragh published by Springer (2018)
27. I.M. Dharmadasa, P.A. Bingham, O.K. Echendu, H.I. Salim, T. Druffel, R. Dharmadasa, G.U. Sumanasekera, R.R. Dharmasena, M.B. Dergacheva, K.A. Mit, K.A. Urazov, L. Bowen, M. Walls, A. Abbaas, Fabrication of CdS/CdTe-based thin film solar cells using an electro-chemical technique. Coatings **4**, 380–415 (2014). https://doi.org/10.3390/coatings4030380
28. I.M. Dharmadasa, M.L. Madugu, O.I. Olusola, O.K. Echendu, F. Fauzi, D.G. Diso, A.R. Weerasinghe, T. Druffel, R. Dharmadasa, B. Lavery, J.B. Jasinski, T.A. Krentsel, G. Sumanasekera, Electroplating of CdTe thin films from cadmium sulphate precursor and comparison of layers grown by 3-electrode and 2-electrode systems. Coatings (2017). https://doi.org/10.3390/coatings7020017
29. I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, O.I. Olusola, H.I. Salim, M.L. Madugu, A.A. Ojo, Improvement of composition of CdTe thin films during heat treatment in the presence of $CdCl_2$. J. Mater. Sci. Mater. Electron. **28**(3), 2343–2352 (2017). https://doi.org/10.1007/s10854-016-5802-9
30. S.H. Shin, J. Bajaj, L.A. Moudy, D.T. Cheung, Characterisation of Te precipitates in CdTe crystals. Appl. Phys. Lett. **43**, 68–70 (1983)
31. P.M. Amirtharaj, F.H. Pollak, Raman scattering study of the properties and removal of excess Te on CdTe surfaces. Appl. Phys. Lett. **45**, 789–791 (1984)
32. P. Fernández, Defect structure and luminescence properties of CdTe based compounds. J. Optoelectron. Adv. Mater. **5**, 369–388 (2003)
33. A.A. Ojo, I.O. Olusola, I.M. Dharmadasa, Effect of the inclusion of Galium in normal Cadmium chloride treatment on electrical properties of CdS/CdTe solar cell. Mater. Chem. Phys. **196**, 229–236 (2017)
34. K. Zanio, *Cadmium Telluride, in Semiconductors and Semimetals*, vol. 13 (Academic Press, Cambridge, 1978)
35. T. Potlag, L. Ghimpu, P. Gashin, A. Pudov, T. Nagle, J. Sites, Influence of annealing in different chlorides on the photovoltaic parameters of CdTe/CdS solar cells. Sol. Energy Mat. Sol. Cell **80**, 327–334 (2003)
36. R.G. Dhere, M. Bonnet-Eymard, E. Charlet, E. Peter, J.N. Ducnow, J.V. Li, D. Kuciauska, T.A. Gessert, CdTe solar cell with industrial Al:ZnO on soda-lime glass. Thin Solid Films **519**, 7142–7145 (2011)
37. J. M. Woodcock, A. K. Turner, M. E. Ozsan, J. G. Summers, Thin film solar cells based on electrodeposited CdTe. In Conference Record of the Twenty Second IEEE Photovoltaic Specialists Conference-1991, Las Vegas, pp. 7–11 October 1991
38. N. Nakayama, H. Matsumoto, K. Yamaguchi, S. Ikagami, Y. Hioki, Ceramic thin film CdTe solar cell. J. Appl. Phys. **15**, 2281–2282 (1976)
39. V. Komin, B. Tetali, V. Viswanathan, S. Yu, D.L. Morel, C.S. Ferekides, The effect of the $CdCl_2$ treatment on CdTe/CdS thin film solar cells studied using deep level transient spectroscopy. Thin Solid Films **431–432**, 143–147 (2003)
40. D. Cunningham, M. Rubcich, D. Skinner, Cadmium telluride PV module manufacturing at BP Solar. Prog. Photovolt. **10**, 159–168 (2002)
41. S. Mazzamuto, L. Vailant, A. Bosio, N. Romeo, N. Armani, G. Salviati, A study of the CdTe treatment with a Freon gas such as CHF2Cl. Thin Solid Films **16**(7), 079–7083 (2008)
42. I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, H.I. Salim, T. Druffel, R. Dharmadasa, B. Lavery, Effects of $CdCl_2$ treatment on deep levels in CdTe and their implications on thin film solar cells. A comprehensive photoluminescence study. J. Mater. Sci. Mater. Electron. **26**(7), 4571–4583 (2015). https://doi.org/10.1007/s10854-015-3090-4

43. M. Kim, S. Sohn, S. Lee, Reaction kinetics study of CdTe thin films during CdCl2 heat treatment. Sol. Energy Mater. Sol. Cells **95**, 2295–2301 (2011)
44. O. Zywitzki, T. Modes, H. Morgner, C. Metzner, B. Siepchen, B. Spath, C. Drost, V. Krishnakumar, S. Frauenstein, Effect of chlorine activation treatment on electron beam induced current signal distribution of cadmium telluride thin film solar cells. J. Appl. Phys. **114**, 163518-1–163518-5 (2013). https://doi.org/10.1063/1.4827204
45. C. Li, Y. Wu, J. Poplawsky, T.J. Pennycook, N. Paudel, W. Yin, S.J. Haigh, M.P. Oxley, A.R. Lupini, M. Al-Jassim, S.J. Pennycook, Y. Yan, Grain-boundary-enhanced carrier collection in CdTe solar cells. Phys. Rev. Lett. **112**, 156103-1–156103-5 (2014)
46. C. Li, G. Chen, W. Wang, J. Zhang, L. Wu, X. Hao, L. Feng, Grain boundary passivation by $CdCl_2$ treatment in CdTe solar cells revealed by Kelvin probe force microscopy. J. Mater. Sci.: Mater. Electron. **29**(24), 20718–20725 (2018)
47. I.M. Dharmadasa, Recent developments and progress on electrical contacts to CdTe, CdS and ZnSe with special reference to barrier contacts to CdTe. Invited review paper. Prog. Cryst. Growth Charact. **36**(4), 249–290 (1998)
48. N.A. Shah, A. Ali, Z. Ali, A. Maqsood, A.K.S. Aqili, Properties of Te-rich cadmium telluride thin films fabricated by closed space sublimation technique. J. Cryst. Growth **284**, 477–485 (2005)
49. D.G. Diso, F. Fauzi, O.K. Echendu, O.I. Olusola, I.M. Dharmadasa, Optimisation of CdTe electrodeposition voltage for development of CdS/CdTe solar cells of CdS/CdTe solar cells. J. Mater. Sci.: Mater. Electron. **27**, 12464–12472 (2016)
50. I.M. Dharmadasa, A.A. Ojo, Unravelling complex nature of CdS/CdTe based thin film solar cells. J. Mater. Sci.: Mater. Electron. **28**, 16598–16617 (2017)
51. T. Schulmeyer, J. Fritsche, A. Thiben, A. Klein, W. Jaegermann, M. Campo, J. Beier, Effect of in situ UHV $CdCl_2$-activation on the electronic properties of CdTe thin film solar cells. Thin Solid Films **431–432**, 84–89 (2003)
52. J. Ma, D. Kuciauskas, D. Albin, R. Bhattacharya, M. Reese, T. Barnes, J.V. Li, T. Gessert, S. Wie, Phys. Rev. Lett. **111**, 067402 (2013)
53. M.O. Reese, C.L. Perkins, J.M. Burst, S. Farrell, T.M. Barnes, S.W. Johnston, D. Kuciauskas, T.A. Gessert, W.K. Metzger, Intrinsic surface passivation of CdTe. J. Appl. Phys. **118**, 155305 (2015)
54. W. Shockley, H.J. Queisser, Detailed balance limit of efficiency of p-n Junction solar cells. J. Appl. Phys. **32**, 510 (1961). https://doi.org/10.1063/1.1736034
55. M'baye A 1980 Donnees solaires pour differentes caracteristiques atmospheriques, CNRS, Sophia antipolis, BPI-06560 Valbonne., 23
56. I.M. Dharmadasa, N.D.P.S.R. Kalyananaratne, R. Dharmadasa, Effective harvesting of photons for improvement of solar energy conversion by graded bandgap multilayer solar cells. J. Natl. Sci. Found. Sri Lanka **41**(2), 73–80 (2013)
57. M.A. Green, Y. Hishikawa, E.D. Dunlop, D.H. Levi, J. Hohl-Ebinger, M. Yoshita, A.W.Y. Ho-Baillie, Solar cell efficiency Tables (version 53). Prog. Photovolt. (2019). https://doi.org/10.1002/pip.3102
58. A.A. Ojo, I.M. Dharmadasa, 15.3% efficient graded bandgap solar cells fabricated using electroplated CdS and CdTe thin films. Sol. Energy **136**, 10–14 (2016)
59. I.M. Dharmadasa, Third generation multi-layer tandem solar cells for achieving high conversion efficiencies. Sol. Energy Mater. Sol. Cells **85**, 293–300 (2005)
60. A. A. Ojo, W. M. Cranton, I. M. Dharmadasa, Next generation multilayer graded bandgap solar cells. Monogragh published by Springer, August (2018)
61. I.M. Dharmadasa, J.S. Roberts, G. Hill, Third generation multilayer graded bandgap solar cells for achieving high conversion efficiencies—II. Sol. Energy Mater. Sol. Cells **88**, 413–422 (2005)
62. I.M. Dharmadasa, Y. Rahaq, A.A. Ojo, T.I. Alanazi, Perovskite solar cells: a deep analysis using current-voltage and capacitance-voltage techniques. J. Mater. Sci.: Mater. Electron. **30**, 1227–1235 (2019)
63. I.M. Dharmadasa, Y. Rahaq, A.E. Alam, Perovskite solar cells: short lifetime and hysteresis behaviour of current-voltage characteristics. J. Mater. Sci.: Mater. Electron. **30**(14), 12851–12859 (2019)
64. N.J. Jeon, H. Na, E.H. Jung, Y.G. Tae-Toul Yang, G.Kim Lee, S.I. Hee-Won Shin, J.Lee Seok, J. Seo, A fluorene-terminated hole-transporting material for highly efficient and stable perovskite solar cells. Nat. Energy **3**, 682–689 (2018)
65. A. Alam, A. Ojo, J. Jasinski, I.M. Dharmadasa, Magnesium incorporation in n-CdTe to produce wide bandgap p-Type CdTe: Mg window layers. ChemEngineering **2**(4), 59 (2018)
66. A.E. Alam, W.M. Cranton, I.M. Dharmadasa, Electrodeposition of CdS thin-films from cadmium acetate and ammonium thiosulphate precursors. J. Mater. Sci. Mater. Electron. **30**(5), 4580–4589 (2019)