Journal of Materials Science: Materials in Electronics (2019) 30:11493–11498
https://doi.org/10.1007/s10854-019-01502-x

A stress sensor based on a silicon field effect transistor comprising a piezoelectric AlN gate dielectric

H. Winterfeld[1] · L. Thormählen[2] · H. Lewitz[2] · E. Yarar[2] · T. Birkoben[1] · N. Niethe[1] · N. Preinl[1] · H. Hanssen[3] · E. Quandt[2] · H. Kohlstedt[1]

Received: 6 February 2019 / Accepted: 11 May 2019 / Published online: 21 May 2019
© The Author(s) 2019

Abstract

Piezoelectric materials have been introduced to transistor gate stacks to improve MOSFET behaviour and develop sensor applications. In this work, we present an approach to a partly industrial field effect transistor, with a gate stack based upon low temperature AlN. Using the piezoelectric effect of the nitrogen-polar AlN, we are able to drive the transistor by inducing strain across the device. To ensure maximum sensitivity, the piezoelectric material is placed as closely to the transistor channel as possible and the transistor is operated in the most sensitive part of the sub-threshold regime. This allows the detection of different magnitudes of force applied to the device and to easily distinguish between them. The created sensor was analysed using XRD, current–voltage and specific force application measurements. Furthermore, the continuous response to periodic low frequency stimulation is investigated. Therefore, we introduce a highly scalable device with a wide range of application possibilities, ranging from varying sensor systems to energy harvesting.

1 Introduction

Driven by the downscaling of silicon (Si) based semiconductor devices, there have been tremendous efforts to establish alternative gate dielectrics as gate materials during the last decades [1, 2]. Representative dielectric materials include nitrides and oxides such as, Si_3N_4, AlN, ZrO_2, HfO_2 or $HfSiO_4$ [3–7]. Besides the research on non-polar high-k dielectrics, gate stacks comprising ferroelectric complex oxide materials (e.g. $PbZr_xTi_{1-x}O_3$ (PZT) or $SrBiTaO_9$ (SBT)) attract considerable interest for non-volatile memory applications [8–10]. Therefore, a matured ferroelectric field-effect transistor (FeFET) technology is envisioned in the near future, comprising HfO_x compounds as a ferroelectric gate stack [11, 12]. Besides the above-mentioned silicon related development strand, novel devices and dielectric materials are used in various applications besides the traditional semiconductor information technology (IT). Examples include thin film transistors (TFTs), smart sensor systems utilizing piezotronics and piezo-phototronics, biomechanical CMOS and health care [13–16]. Due to the CMOS compatibility, AlN could be a promising material for piezo-based applications [17, 18]. Researchers widely investigate the possibility of using AlN in energy harvesting devices, ultrasonic transducers, power semiconductor devices and magneto electric sensors [19, 20]. Even though other piezoelectric materials (in the form of polymers or complex oxides) offer higher piezoelectric coefficients, AlN allows the incorporation of the proposed sensor into state-of-the-art silicon technology.

In this manuscript we present results obtained from Si field-effect transistors comprising alternative gate piezoelectrics [21–26] made from AlN [27]. The transistors were integrated on silicon cantilevers [28]. By bending the cantilever, the mechanosensitive response was measured recording the channel current (I_{DS}) over time [29, 30]. We believe that this sensor based on a piezoelectric transistor has the potential to become a valid alternative in fields like accelerometers, piezoelectric microphones, tactile sensors or magneto electric sensors.

✉ H. Winterfeld
hewi@tf.uni-kiel.de

✉ H. Kohlstedt
hko@tf.uni-kiel.de

[1] Nanoelektronik, Technische Fakultät, Christian-Albrechts-Universität zu Kiel, 24143 Kiel, Germany

[2] Inorganic Functional Materials, Technische Fakultät, Christian-Albrechts-Universität zu Kiel, 24143 Kiel, Germany

[3] Fraunhofer-Institut für Siliziumtechnologie, 25524 Itzehoe, Schleswig-Holstein, Germany

2 Device fabrication

The devices were fabricated in a two-part process, with the first half being produced at the Fraunhofer Institute for Silicon Technology in Itzehoe (ISIT), 25524 Itzehoe, Germany and the final steps undertaken in the Nanolaboratory at the Faculty of Engineering at Kiel University. In the first part of the fabrication, the channel, source, drain and bulk regions were defined by local oxidation of silicon (LOCOS). Subsequently, the source and drain regions were doped with 5.0×10^{15} cm^{-3} As, the bulk region with 5.0×10^{15} cm^{-3} B and the substrate (and thus the channel region) with 2.1×10^{12} cm^{-3} B. The length of the resulting channel was 10 µm and the width was 25 µm. The gate oxide was grown thermally to a thickness of 13 nm (cf. Figure 1a) in a state-of-the-art silicon Fab line. The 8 inch wafer was cut into 1 cm^2 pieces and the wiring (150 nm Ti) was added (cf. Figure 1b). Following this, the gate stack (bottom to top: 10 nm Ta/100 nm Pt/500 nm AlN/300 nm Pt) was deposited over the surface of the entire sample (cf. Figure 1c). For all steps,standard UV lithography (Karl Süss MA6 Mask Aligner) was used. The Ti thin films were deposited by sputtering and patterned by lift-off. The nitrogen-polar AlN layer was deposited using the method introduced by Yarar et al. [27]. The polarity was not specifically chosen, but is given by the growth conditions during sputtering. TEM analysis on additional samples showed a (0001) orientation of the polycrystalline thin film AlN. Afterwards, the gate stack was patterned by ion beam etching (Oxford Instruments PC3000 and a Hiden Analytical mass spectrometer for end-point detection). A cross-sectional schematic of the final device is shown in Fig. 1d). Additionally, for a better understanding of the device layout and dimensions, a SEM picture is displayed in Fig. 1e). The highlighted area shows a cross-sectional view of the gate stack after structuring. In a final step, the samples were polished from 725 µm down to 485 µm thickness and cut into 2 mm × 10 mm cantilevers to allow reasonable flexibility.

As the piezoelectric layer plays a crucial part in the setup of the device, the characteristic numbers were measured to ensure high quality performance (cf. Table 1). These measurements were performed on an additional sample with a capacitive structure, fabricated alongside the transistor devices.

For this work, two different types of samples were prepared. The piezoelectric samples make use of the full gate stack consisting of the SiO_2 gate oxide, the Ta/Pt seedlayer,

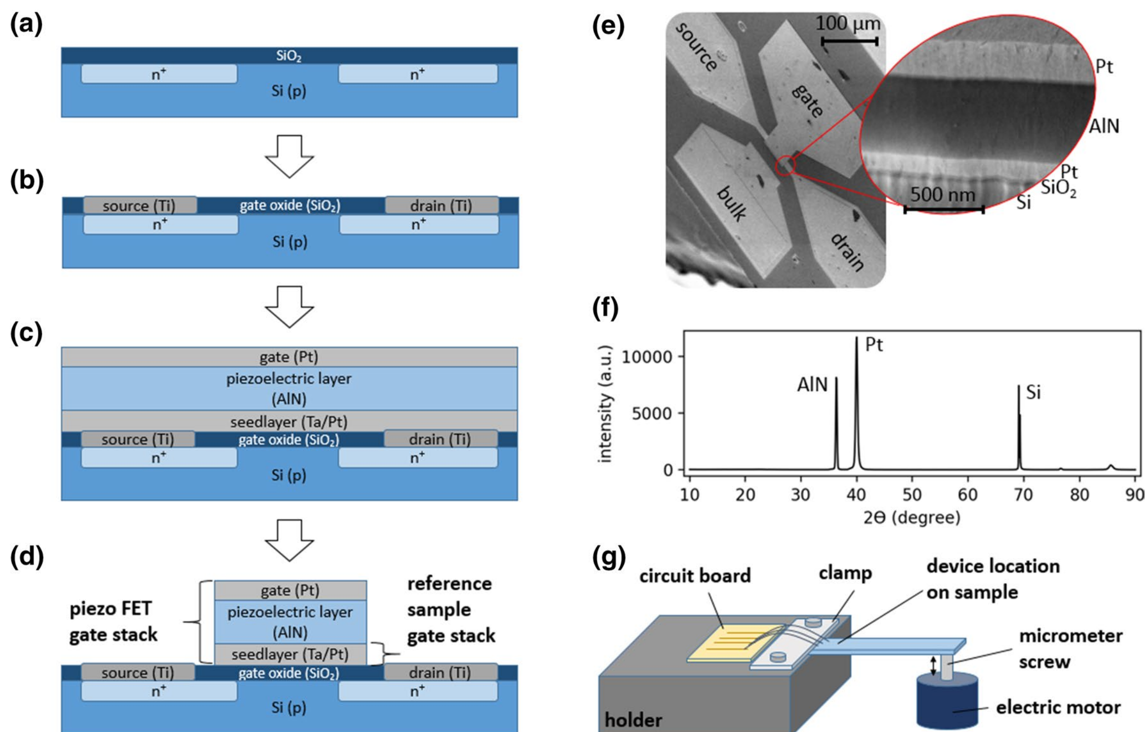

Fig. 1 **a–c** Cross-sectional schematic view of the fabrication process of the piezoelectric MOSFET structure. **d** Schematic cross-section view of the final devices, highlighting the different gate stacks for both sample types (piezoelectric-FET and reference sample). **e** SEM image of the final piezoelectric transistor device on the cantilever structure, with the gate stack highlighted in the cross-sectional view. **f** XRD measurement results for the gate stack of the piezoelectric FET, comprising AlN as the piezoelectric material in this sensor. **g** Graphic representation of the measurement setup for the proposed sensor

Table 1 Measured piezoelectric and dielectric properties of the AlN thin films used in this work

$e_{31,f}$ (C/m^2)	$d_{33,f}$ (pm/V)	ε_r	tan δ (%) (10^5 V/m)
− 1.40	5.96	10	0.9

the AlN and the Pt top electrode (see Fig. 1d). We would like to emphasize that the Ta/Pt seedlayer combines two important features: Firstly, the Ta and Pt thin films serve as an adhesion layer and a seedlayer for the columnar growth of the AlN, respectively [27]. XRD analysis of the seedlayer revealed a (111) orientation of the Pt which aids the growth of AlN with a high piezoelectric coefficient [27]. Results of an XRD measurement are displayed in Fig. 1f). Secondly, the Ta/Pt layer can as well be considered as a buffer to separate the electrically important SiO_2 gate oxide from the AlN during sputtering.

In addition to the AlN gate stack samples, reference samples were fabricated in the same way as the piezoelectric samples without the AlN layer and top electrode (gate) (cf. Figure 1d). Therefore, they function as a reference during the measurements, to ensure that the effects originate in the additional piezoelectric AlN layer and are not due to an underlying non-polar film or the piezo resistance of the Si substrate [31].

3 Results and discussion

All measurements were performed using the setup schematically shown in Fig. 1g. The samples were mounted on the holder and clamped from the top. This ensures that the cantilevers may only be bend in the desired direction. The forces were applied to the cantilever in an upwards direction, using a computer controlled micrometer screw. Further, a wire-bonder was used to connect the transistors to a circuit board. The circuit board is connected to the Hewlett-Packard 4145A Semiconductor Parameter Analyzer, used for all measurements. To guarantee reproducible results the cantilever was bend by a micrometer screw, driven by an electric motor.

The transistor's characteristic output and transfer curves were recorded. Figure 2a shows the output characteristics of a reference sample. The reference sample has the expected MOSFET output characteristics. In comparison, the output curves of a piezoelectric sample are displayed in Fig. 2b, showing no saturation after $V_{DS} > V_{GS} - V_{Th}$ (here $V_{Th} \approx 3$ V is the threshold voltage). This is due to the floating gate structure of the device, which makes the channel current dependent upon the drain-source voltage V_{DS}, even in this voltage region [32, 33]. For a floating gate transistor, the channel current in the saturation region is given by the following equation:

$$I_D = \frac{\beta_n}{2} V_{Dsat}^2 \left(1 + \alpha_D \frac{V_{DS} - V_{Dsat}}{V_{Dsat}}\right)^2. \quad (1)$$

Here β_n is the transmittance factor, V_{Dsat} is the saturation voltage and α_D is the coupling coefficient to the drain. With this dependency on the drain voltage, the steady current increase of the output characteristics can be explained. Consequently, the transfer characteristics of the piezoelectric sample shift to the left with increased V_{DS}, since the threshold voltage V_{Th} is influenced by V_{DS} and the capacitive divider, defined by the classical MOSFET capacitances (C_{GS}, C_{GB}, C_{GD}; with G: gate, S: source, B: bulk and D: drain) and the additional capacitance (C_{GCo}; with Co: control gate) created by the addition of a floating gate into the gate stack. The transfer characteristics of the reference sample

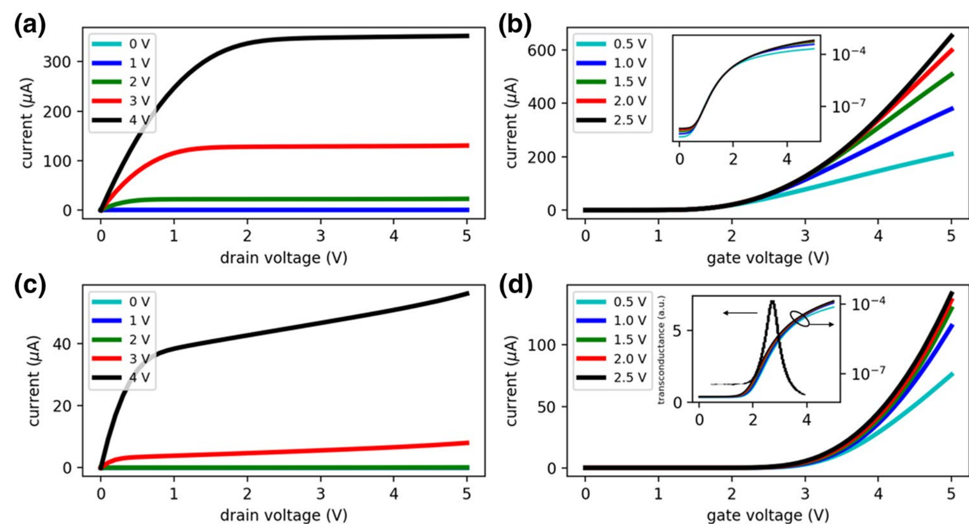

Fig. 2 Measured output characteristics of the **a** piezoelectric FET and the **b** reference sample used in this work. **c** Measured transfer characteristics of the **c** piezoelectric FET and the **d** reference sample. Insets: semi-logarithmic representation of the corresponding transfer curves, highlighting the sub-threshold regions of the devices. Furthermore, the transconductance in relation to applied gate voltage is shown in the inset in d)

and the piezoelectric sample are shown in Fig. 2c and d, respectively. From the comparison of these characteristics, an increase in threshold voltage from $V_{T,ref} \approx 2$ V for the reference sample to $V_T \approx 3$ V for the piezoelectric sample is seen. This increase is reflected in the channel current values reached in the output characteristics. The addition of a capacitive structure in the gate stack of the transistor reduces the electric field across the gate oxide and consequently the current through the semiconductor. Furthermore, for floating gate transistors the threshold voltage partly depends on the floating gate charge, which explains the shift experienced by the transfer characteristics of the piezoelectric field-effect transistor.

Moreover, the transfer curves are shown on a semi-logarithmic scale in the corresponding insets. Considering the field effect transistor is to be driven by a change in charge in the piezoelectric layer, a large response to a small change in charge is desired. Therefore, points of operation located on the sub-threshold slope of the transfer curve are used. To this end, the transconductance of a piezoelectric device is given in the inset of Fig. 2d, identifying the operation region offering the highest output. The transconductance (shown here for an additional piezoelectric FET) was recorded in dependence of the applied gate voltage, using a Stanford sr830 Lock-In Amplifier. In the subthreshold region, a change in the gate voltage of 450 mV leads to an increased current of one order of magnitude. The transconductance for the piezoelectric device was determined to be $g_m = 107\ \mu AV^{-1}$.

Initially, the response to a force of the piezoelectric sample, as well as the reference sample was investigated. Therefore, the samples were mounted to the holder and gate voltages of $V_{GS} = 1.5$ V and source-drain voltages of $V_{DS} = 2.0$ V were applied. When initially applying the voltages to the device, an increase in the channel current can be observed. The capacitive structure of the piezoelectric sample under constant external voltages leads to the witnessed initial rise in current. Additionally, this current increase corresponds to a shift in the transfer curve, resulting in lower voltages needed to operate the sensor at the steepest part of the subthreshold swing. Therefore, the electric motor was programmed to raise the micrometer screw 20 µm after sample stabilization. The resulting force F applied to the tip of the cantilever can be calculated using $F = 3\delta EI/L^3$ [34]. Here, δ is the deflection of the cantilever tip, E is the modulus of elasticity ($E = 125 \times 10^9$ Pa [35]), I is the moment of inertia ($I = bh^3/12$, with $b = 2$ mm and $h \approx 485$ µm) and L is the length of the free-standing cantilever ($L \approx 7.5$ mm).

The result of a deflection of 20 µm (equivalent to a force of 340 mN) on both types of samples is shown in Fig. 3a). The force is applied after about 3000 s and results in an increase in current for the piezoelectric sample only. Appling a force to the reference sample has no effect on the current response, underlining that the piezoelectric layer is responsible for any current change. From the conducted comparison of the two devices, we are convinced that no stress induced effects in the semiconductor, such as strained silicon, contribute to the changes in the channel current. The deflection is kept constant until the current dropped back to a relaxed state. Since the force applied does not change during this time, a charge equalization must take place, which is caused

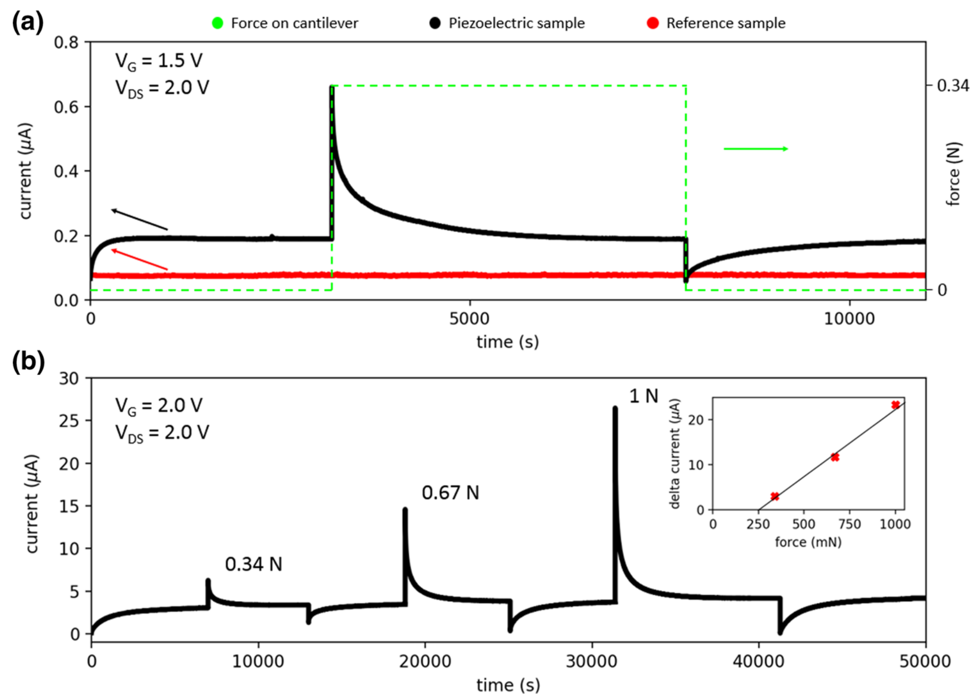

Fig. 3 **a** The current response of the piezoelectric sample (black) and the reference sample (red) to a force of 340 mN applied to the tip of the cantilever. Additionally, the applied force is shown (green). **b** Current response of the piezoelectric sample to applied forces of 340 mN, 670 mN and 1 N. Inset: Change in channel current in response to applied forces (red) (Color figure online)

by a leakage current across the AlN. When the equalized state was reached, the force on the cantilever was lifted. The result is a current peak in the opposite direction and once more, a relaxation period. This relaxation characteristic is a result of leakage currents across the piezoelectric AlN.

Additionally, the response to varying forces on the cantilever was investigated. Therefore, the piezoelectric sample was exposed to a gate voltage of $V_{GS} = 2.0$ V and source-drain voltage of $V_{DS} = 2.0$ V. Thereafter, the tip of the cantilever was deflected 20 µm, 40 µm and 60 µm by the micrometer screw. After each deflection, the relaxation of the device was awaited before returning it to its initial state by detaching the micrometer screw. Increasing deflection, i.e. applying a greater force, leads to a linear rise in the initial current response (cf. Figure 3b). The linearity of the current response is highlighted in the inset of Fig. 3b, where the increase in current is displayed against the corresponding forces applied to the cantilever. From this, the smallest detectable force ($F_{min} = 250$ mN) and the sensitivity ($S = 60$ µA/N) of the device can be determined. However, the detectable force is strongly dependent on the cantilever geometry, which could be changed to optimize these characteristic values. Nonetheless, the magnitude of the force applied, as well as the duration of the excitation signal, can be qualitatively deduced from the output signal of the sensor. In comparison to other transistor based approaches, the proposed sensor shows higher sensitivity in similar force ranges [36]. Additionally, the sensor setup utilized in this work consist of a single sensor device and is not amplified by a subsequent circuit [37].

Lastly, the device response to a periodic signal (cf. Figure 4a) was investigated. When the cantilever was deflected 20 µm for $\Delta T_1 = 10$ s, the characteristic current increase was seen. Afterwards, the cantilever was released and returned to its initial position for $\Delta T_2 = 10$ s. This action was repeated 100 times and the results are shown in Fig. 4b. Over the course of the measurement it can be seen that stabilization takes place. Even though the change in current stays the same during the measurement, initially, a fall in the maximum and minimum current values can be observed. This stabilization manner can most likely be linked to a charging of traps in the isolating layers, which were probably created during the plasma processes used in the fabrication of the device. Using modern silicon technology, additional processing steps such as an annealing step could be introduced to alleviate this problem in the future. However, we cannot be sure in which layer these traps are located exactly. The stabilized periodic behavior is highlighted in the inset in Fig. 4b. Here, the continuous response to the same stimulation over a larger period of time is shown. These measurements show the reliability of the sensor, producing the same stable output signal in response to an unchanged input.

4 Conclusion

The possibility of creating a CMOS compatible piezoelectrically driven MOSFET, based upon low temperature sputtered AlN was shown. Placing the sensing material on top of a field-effect-transistor brings the sensor as closely to an amplifier as possible and thus reduces noise. Additionally, we were able to show that the magnitude of force applied to the cantilever can be determined from the current response. It could further be determined that the change in channel current in response to an applied force follows a linear trajectory, simplifying future application of this sensor. Moreover, we showed that a periodic stimulation of the device results in a continuous, invariant response. Since a partly industrial fabrication process was used, we believe that the device performance can be improved by moving to

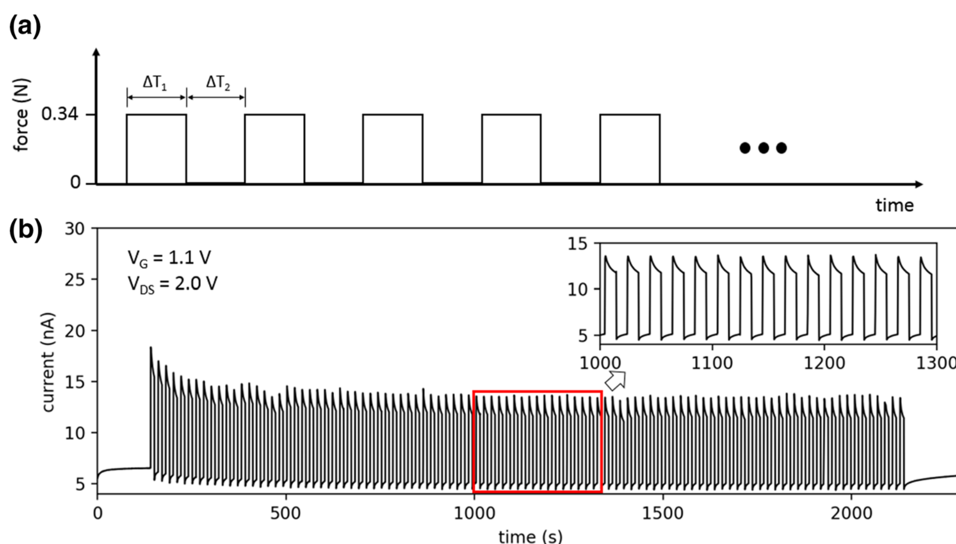

Fig. 4 **a** Pulse train applied to the cantilever in order to investigate current responses to periodic stimulation. **b** Current response to periodic stimulation (deflection of the cantilevers tip of 20 µm, 100 times). Inset: Magnification of the highlighted part of the current response (Color figure online)

a state-of-the-art fabrication process. This could improve the subthreshold swing of the transistor, resulting in a larger change in channel current for the same applied forces and thus improving sensitivity. Therefore, we believe that this device has great application possibilities within sensors, energy harvesting or other areas.

Acknowledgement We thank the German Research Society (DFG) for financial support through the Research Unit 2093.

Open Access This article is distributed under the terms of the Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made.

References

1. A.I. Kingon, J.-P. Maria, S.K. Streiffer, Nature **406**, 1032 (2000)
2. G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. **89**, 5243 (2001)
3. K. Yim, Y. Yong, J. Lee, K. Lee, H.-H. Nahm, J. Yoo, C. Lee, C. Seong Hwang, S. Han, NPG Asia Mater. **7**, e190 (2015)
4. D.R. Clark, Materials **7**, 2913–2944 (2014)
5. Sanjeev Kumar Gupta, in *Physics and Technology of Silicon Carbide Devices*, edited by Jitendra Singh (IntechOpen, Rijeka, 2012), p. Ch.-8
6. J. Efavi, T. Mollenhauer, T. Wahlbrink, H.D.B. Gottlob, M. Lemme, H. Kurz, *Tungsten Work Function Engineering for Dual Metal Gate Nano-CMOS* (2005)
7. B.H. Lee, J. Oh, H.H. Tseng, R. Jammy, H. Huff, Mater. Today **9**, 32 (2006)
8. J.F. Scott, *Ferroelectric Memories* (Springer, Berlin, 2000)
9. R. Waser, *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications* (Wiley, Weinheim, 2016)
10. H. Kohlstedt, Y. Mustafa, A. Gerber, A. Petraru, M. Fitsilis, R. Meyer, U. Böttger, R. Waser, Microelectron. Eng. **80**, 296 (2005)
11. M. Hoffmann, U. Schroeder, T. Schenk, T. Shimizu, H. Funakubo, O. Sakata, D. Pohl, M. Drescher, C. Adelmann, R. Materlik, A. Kersch, T. Mikolajick, J. Appl. Phys. **118**, 072006 (2015)
12. U. Schroeder, C. Richter, M.H. Park, T. Schenk, M. Pešić, M. Hoffmann, F.P.G. Fengler, D. Pohl, B. Rellinghaus, C. Zhou, C.-C. Chung, J.L. Jones, T. Mikolajick, Inorg. Chem. **57**, 2752 (2018)
13. Z.L. Wang, Adv. Mater. **24**, 4632 (2012)
14. Z.L. Wang, *Piezotronics and Piezo-Phototronics* (Springer, Heidelberg, 2012)
15. N.M. Triet, T.Q. Trung, N.T.D. Hien, S. Siddiqui, D.-I. Kim, J.C. Lee, N.-E. Lee, Nano Res. **8**, 3421 (2015)
16. Y.-G. Ha, K. Everaerts, M.C. Hersam, T.J. Marks, Acc. Chem. Res. **47**, 1019 (2014)
17. S. Marauska, T. Dankwort, H.J. Quenzer, B. Wagner, Procedia Eng. **25**, 1341 (2011)
18. J.C. Doll, B.C. Petzold, B. Ninan, R. Mullapudi, B.L. Pruitt, J. Micromech. Microeng. **20**, 025008 (2009)
19. C. Fei, X. Liu, B. Zhu, D. Li, X. Yang, Y. Yang, Q. Zhou, Nano Energy **51**, 146 (2018)
20. C.M. Leung, J. Li, D. Viehland, X. Zhuang, J. Phys. D **51**, 263002 (2018)
21. S.J. Rupitsch, *Piezoelectric Sensors and Actuators: Fundamentals and Applications* (Springer, Berlin, 2019)
22. K. Uchino, *Advanced Piezoelectric Materials* (Elsevier, Kidlington, 2017)
23. P. Songsukthawan, C. Jettanasen, in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia)* (2017), pp. 2256–2259
24. S.H. Baek, J. Park, D.M. Kim, V.A. Aksyuk, R.R. Das, S.D. Bu, D.A. Felker, J. Lettieri, V. Vaithyanathan, S.S.N. Bharadwaja, N. Bassiri-Gharb, Y.B. Chen, H.P. Sun, C.M. Folkman, H.W. Jang, D.J. Kreft, S.K. Streiffer, R. Ramesh, X.Q. Pan, S. Trolier-McKinstry, D.G. Schlom, M.S. Rzchowski, R.H. Blick, C.B. Eom, Science **334**, 958 (2011)
25. Y.-R. Wu, J. Singh, Appl. Phys. Lett. **85**, 1223 (2004)
26. S. Gupta, H. Heidari, A. Vilouras, L. Lorenzelli, R. Dahiya, IEEE Trans. Circuits Syst. I Regul. Pap. **63**, 2200 (2016)
27. E. Yarar, V. Hrkac, C. Zamponi, A. Piorra, L. Kienle, E. Quandt, AIP Adv. **6**, 075115 (2016)
28. R. Takei, H. Okada, D. Noda, R. Ohta, T. Takeshita, T. Itoh, T. Kobayashi, Jpn. J. Appl. Phys. **56**, 04CC03 (2017)
29. J.-P. Colinge, C.A. Colinge, *Physics of Semiconductor Devices* (Springer, New York, 2002)
30. S.M. Sze, K.K. Ng, *Physics of Semiconductor Devices*, 3rd edn. (Wiley, Hoboken, 2007)
31. C.S. Smith, Phys. Rev. **94**, 42 (1954)
32. W.D. Brown, J. Brewer, in *Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices* (IEEE, 1998)
33. P. Pavan, R. Bez, P. Olivo, E. Zanoni, Proc. IEEE **85**, 1248 (1997)
34. V.D. da Silva, *Mechanics and Strength of Materials* (Springer, Berlin, 2006)
35. B. Bhushan, X. Li, J. Mater. Res. **12**, 54 (1997)
36. S. Gupta, N. Yogeswaran, F. Giacomozzi, L. Lorenzelli, R. Dahiya, in *2018 IEEE Sensors* (2018), pp. 1–4
37. A. Adami, R.S. Dahiya, C. Collini, D. Cattin, L. Lorenzelli, Sens. Actuators A **188**, 75 (2012)

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.