Journal of Electronic Testing
https://doi.org/10.1007/s10836-024-06108-8

A DfT Strategy for Guaranteeing ReRAM's Quality after Manufacturing

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Received: 20 November 2023 / Accepted: 19 February 2024

Abstract
Memristive devices have become promising candidates to complement the CMOS technology, due to their CMOS manufacturing process compatibility, zero standby power consumption, high scalability, as well as their capability to implement high-density memories and new computing paradigms. Despite these advantages, memristive devices are susceptible to manufacturing defects that may cause faulty behaviors not observed in CMOS technology, significantly increasing the challenge of testing these novel devices after manufacturing. This work proposes an optimized Design-for-Testability (DfT) strategy based on the introduction of a DfT circuitry that measures the current consumption of Resistive Random Access Memory (ReRAM) cells to detect not only traditional but also unique faults. The new DfT circuitry was validated using a case study composed of a 3x3 word-based ReRAM with peripheral circuitry implemented based on a 130 nm Predictive Technology Model (PTM) library. The obtained results demonstrate the fault detection capability of the proposed strategy with respect to traditional and unique faults. In addition, this paper evaluates the impact related to the DfT circuitry's introduced overheads as well as the impact of process variation on the resolution of the proposed DfT circuitry.

Keywords Manufacturing test · ReRAMs · Unique faults · DfT Circuitry

1 Introduction

During the last decades, CMOS technology miniaturized according to Moore's law, which predicted that the number of transistors per silicon chip doubles every two years [27]. However, its continuation became challenging, due to limitations on the transistor miniaturization and the increasing demand for emerging applications requiring high-performance systems with strict constraints, posing significant challenges to device technologies and computer architectures [18]. Regarding device technology, reliability, leakage, and cost are the identified walls [18]. Moreover, the memory, power, and Instruction Level Parallelism (ILP) walls are affecting computer architectures [18].

Memristive devices represent one of the most promising candidates to complement CMOS technology, or replace it, in certain applications such as Flash memory, mainly due to their CMOS manufacturing process compatibility, zero standby power consumption, as well as high scalability and density [6, 18, 26]. In addition, these devices can be used not only as memory but also as computing elements [18]. Memristive devices can be classified according to different criteria, such as the dominant physical switching mechanism. In this context, one of the most versatile types is the Redox-based one. In more detail, this kind of memristive device can be used for implementing Redox-based Resistive Random Access Memory (ReRAM). Note that ReRAMs are classified as non-volatile memory [2, 21, 32].

However, the use of these devices depends on being able to guarantee their quality after manufacturing as well as reliability during their lifetime. Despite the lack of information regarding realistic manufacturing deviations, literature already describes that ReRAMs can be affected by unique faults [14, 19, 20], consequently demanding the development of new manufacturing test procedures [15, 16].

In [28], the authors provide a review of the memristive device manufacturing process and a discussion related to possible defects that may affect these novel devices,

Responsible Editor: M. Taouil

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Published online: 23 March 2024

identifying the relation between manufacturing failure mechanisms and faulty behaviors. In addition, in the last few years, some new manufacturing test strategies were proposed in literature, since traditional March Tests, which explore the execution of predefined read and write operations applied at each ReRAM cell, are extremely time-consuming and further not able to guarantee the detection of all unique faults. In the following, some test strategies for manufacturing testing are presented. When considering strategies targeting passive crossbars, a scheme based on "sneak-path sensing" able to test multiple elements of Phase Change Memories at the same time was presented in [23]. The detection is based on a comparison between the output current related to a specific group of cells and the ideal current, accessed based on the execution of March elements. The main drawbacks are that it only works for ReRAMs that have sneak-paths as well as its limitation in terms of cells that can be tested in parallel. In [25], a review of the fault model related to 1R crossbars is presented. In addition, this work presents a March RC with new read operations and a DfT architecture. When considering 1T1R-based ReRAMs, in [19], two DfT schemes that exploit the access time duration and supply voltage level of ReRAM cells to facilitate the detection of unique faults were described. The main drawbacks of these techniques are the test time and the implementation effort required to guarantee high fault detection capability. Finally, in [30], low-cost DfT solutions that augment the testing process and improve the fault coverage of RRAMs are presented. In more detail, a Computation-in-Memory (CiM) based DfT is realized to expedite the detection and diagnosis of faults. Moreover, reconfigurable logic designs (programmable reference generations, period, and voltage of operation) are developed to detect unique RRAM faults.

In this context, this paper presents an extension of the work originally described in [9, 10], which despite being able to provide the required fault detection capability with respect to unique faults, introduced significant area and power overheads to the ReRAM as well as was significantly affected by process variation. In more detail, the main contributions of this paper are:

1. Propose an optimized DfT circuitry for testing ReRAMs after manufacturing aiming to reduce the introduced overheads as well as tolerate process variation;
2. Demonstrate the DfT strategy's detection capability with respect to unique faults caused by manufacturing defects;
3. Provide a discussion related to the main introduced overheads as well as the impact of process variation on the resolution of the DfT circuitry with respect to the previously presented solutions [9, 10];

It is important to note that this paper adopts a ReRAM composed of 1T1R (1 Transistor and 1 Memristor) cells, where the 1R is Bipolar-, Valence Change Mechanism (VCM)-based filamentary device.

The remainder of this paper is structured as follows. Section 2 presents the background related to ReRAMs, fault models, and defect injection schemes. Section 3 summarizes the strategy presented in [10] and describes the optimized DfT strategy based from [9]. In Section 4 the experimental setup is described and Section 5 summarizes the obtained results including a discussion about overheads and process variation impact. Finally, in Section 6 we conclude the paper.

2 Background

This Section introduces the main concepts regarding ReRAMs and summarizes the existing fault models as well as the defect injection schemes that can be adopted for modeling possible manufacturing defects.

2.1 Bipolar-, VCM-based Filamentary Memristive Devices

According to [8], a memristive device (also named Memristor) is a passive element that can be described by a relationship between the time integral of the current (charge q) and the time integral of the voltage (flux ϕ) across its two terminals. Figure 1(a) shows the two circuit symbol options adopted for representing memristive devices in general.

The redox-based resistive memory device consists of a metallic oxide (dielectric) in between a Top Electrode (TE) and a Bottom Electrode (BE), it is a Metal-Insulator-Metal (MIM) structure [33, 34]. Physically, the working principle of a resistive memory device can be based on the reversible formation of a Conductive Filament (CF) in the dielectric by a redox reaction (oxidation and reduction). As previously mentioned, the resistive memory device used in this work assumes as the switching mechanism the Valence Change Mechanism (VCM), which is based on the generation of a conductive filament created in the vicinity of one of the electrodes (active electrode), which is generated during the Forming Stage (FORMATION). The filament is generated by the redistribution of oxygen vacancies. In addition, this filament is a junction of a disc and plug region, whose disc, close to the active electrode, has the concentration of oxygen vacancies altered during the operations in the device [2]. It is important to mention that, the absence or presence and the size of this CF directly influences the current flow through the device [34]. Polarizing the device in one direction increases the CF, which is moving atoms between both

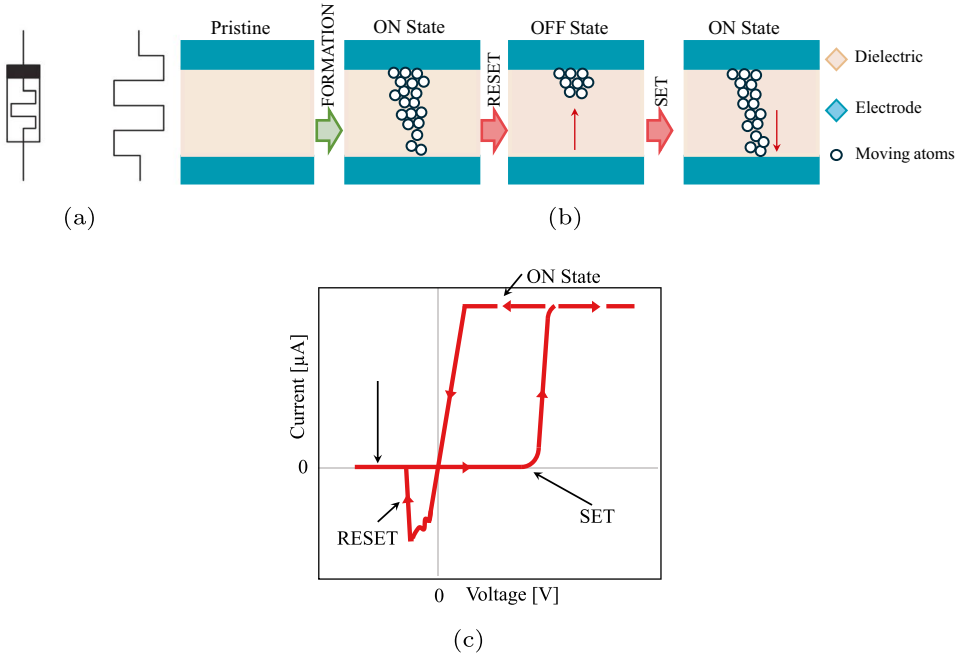


Fig. 1 ReRAMs: **a** Memristive device symbol; **b** formation of conductive paths [32]; and **c** I-V curve of a resistive memory [32]

electrodes and as a consequence the current flow, generating the Low Resistance State (LRS), also named ON State. Polarizing it in the opposite direction will reduce the CF and the current flow, generating the High Resistance State (HRS), or OFF State [34]. The operation that causes the switching from HRS to LRS is called SET and occurs when applying a voltage V_{SET} with an absolute value larger than its threshold voltage (V_{th}). The operation responsible for the LRS switch to HRS is called RESET, occurring when applying a V_{RESET} voltage of opposite polarity to the device [34]. In Fig. 1(b) it is possible to see the CF, furthermore, the Pristine state, which is the state just after the device's fabrication, before the Forming Stage, and in Fig. 1(c) the I-V curve of the bipolar resistive device [32]. To perform a read operation in the resistive memory, a small V_{READ} voltage that is lower than both thresholds is applied to not alter the state of the device, and the generated current is sensed, allowing the identification of the device's state. This voltage can be applied in any direction of electrodes [34]. The CF remains in the resistive memory even when no voltage is present, which categorizes the device as non-volatile [34]. Also, the need to use two opposite polarities in the device classified it as bipolar switching [33].

2.2 Fault Models for ReRAMs

Like any other device, resistive memories are prone to manufacturing deviations, including process variation and manufacturing defects, that may result in faults [5, 15, 28]. These defects need to be properly modeled in order to guarantee an accurate identification of possible faulty behaviors. According to [4] a defect in an electronic system is the unintended difference between the implemented hardware and its intended design. In addition, a representation of a defect at the abstracted function level is called a fault [4]. Thus, the difference between a defect and a fault is rather subtle. They are imperfections in the hardware and function, respectively.

Note that in [5], this definition was revisited and a fault was defined as any deviation from the memristor's expected behavior due to process variations, manufacturing defects, or design-induced anomalies. In addition, the authors established the idea that the fault size is related to the deviation's magnitude and categorized it into three different classes. A deviation above the tolerance limit is classified as catastrophic. However, if the deviation only degrades the performance but is within the tolerances, it is categorized as parametric. Finally, if the deviation's magnitude is insignificant, the fault is called benign [5].

Thus, a ReRAM cell (1T1R) can be affected by faults that are also seen in traditional memory technologies [19]. In more detail, the fault models related to ReRAMs can be initially classified into two categories: (a) Conventional and (b) Unique [16]. Figure 2 depicts the faulty resistance intervals of resistive memory that will be used in this work, as well as how each region is normally read. The regions highlighted in blue represent the area of the faults related to the unique fault model and in red the region associated with conventional faults related to logic '0', such as stuck-at and transition faults, and finally, in green those related to logic '1'.

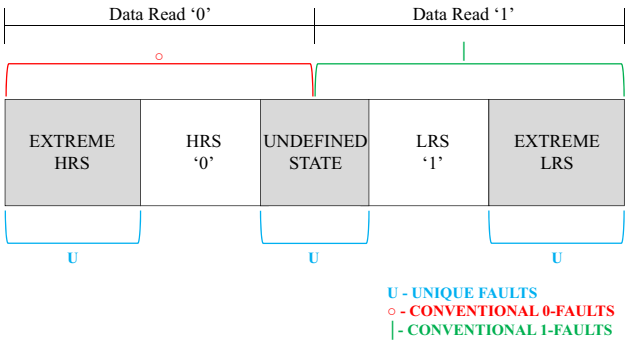


Fig. 2 Resistive states and faulty resistance intervals of ReRAM cells

According to the literature, the four unique faults that can affect ReRAMs are:

1. Undefined Write Fault (UWF) [15], whose definition, after a writing operation, the cell is brought into an undefined state 'U' between '0' and '1' (HRS and LRS);
2. Deep State Fault (DeepF) [23], the resistance in the cell is beyond the boundaries for each state (HRS and LRS), these boundaries are called Extreme High and Extreme Low State. Note that this fault can lead to a stuck-at-fault;
3. Unknown Read Fault (URF) [15, 23], the read operation output is not reliable, because it presents a random logic value as a result, independent from the reading conditions. A URF can occur when the resistive memory stores a resistance very close to or exactly the 'U' state. Note the need to detect the 'U' state because it indicates misbehavior in the resistive memory;
4. Intermittent Undefined State Fault (IUSF) [13], in which the device switches its mechanism intermittently from bipolar to complementary leading to a 'U' state after a write operation.

All unique faults are classified as hard-to-detect (HtD) faults, which means that traditional March tests can not properly detect them, being necessary to adopt new strategies [12]. Finally, it is important to mention that parametric faults, with resistive state values close to the state's margins, can degrade to UWFs, DeepFs, as wells as URFs, turning in catastrophic faults, since these faulty behaviors represent a change of electrical parameters' values associated with the resistive states of the ReRAM cell from nominal or expected values.

2.3 Defect Injection Scheme

In order to simulate all possible faulty behaviors associated to manufacturing deviations, methods for injecting defects in a ReRAM cell are needed. The closer the simulation is to the real behavior of the defect, the better the simulation results will match the final circuit. So a good defect injection scheme for a ReRAM cell is the key to usable simulation results. Currently, two defect models are established, the Resistive Defect (RD) and the Defect Oriented (DO) model. The RD model is based on the idea of introducing a resistor at one specific point in the cell to model a specific defect. A resistor in series with the ReRAM cell can change the resistive state of the cell to an undefined state, for example. Note that the resistance values correspond to the strength of the defects [16]. Unfortunately, this model is not able to represent the nonlinear behavior of ReRAM cells and will lead to imprecise simulation results [15]. In contrast, the DO model focuses on changing parameters in the resistive memory itself to simulate faulty behaviors, being able to represent the non-linearity of the resistive memory. Finally, it is important to mention that the DO model is the scheme that supports the development of Device-Aware Testing [15, 16].

3 The DfT Strategy

In the following will be presented the original DfT Strategy published in [10], then the Optimized DfT Strategy that will be explored in the rest of the paper.

3.1 The Original DfT Strategy

The test of ReRAMs after manufacturing demands new strategies, different from the ones used for testing CMOS-based memories, able to provide detection of not only traditional but also unique faults. A DfT strategy based on the introduction of an On-Chip Sensor (ON_CS) able to measure the current that flows through the ReRAM cells, while performing a predefined operating sequence was presented in [10]. Figure 3 depicts the block diagram of the proposed circuitry. In general terms, the ON_CS is composed of an access transistor, an operational amplifier (AMP), two comparators (Comp0 and Comp1), and a NOR logic gate. A small transistor used during read operations is connected to the Select Line (SL). A bigger transistor in parallel to the small one is introduced and used during write operations. The presence of the small transistor creates the required voltage variation associated to the memristor's current. This voltage variation is amplified and used by Comp0 and Comp1.

The detection capability of the strategy presented in [10] is based on the idea of comparing the current that flows through the ReRAM cell to reference voltage values representing the expected resistive state. In more detail, if the ReRAM cell stores the HRS, a low voltage variation with respect to Gnd will be observed. This voltage variation will be compared to Comp0 and Comp1 in order to indicate a possible faulty behavior that will be indicated in OutAmp. The non-inverted output of the two comparators will be '1' if the input voltage is higher than the reference voltage and

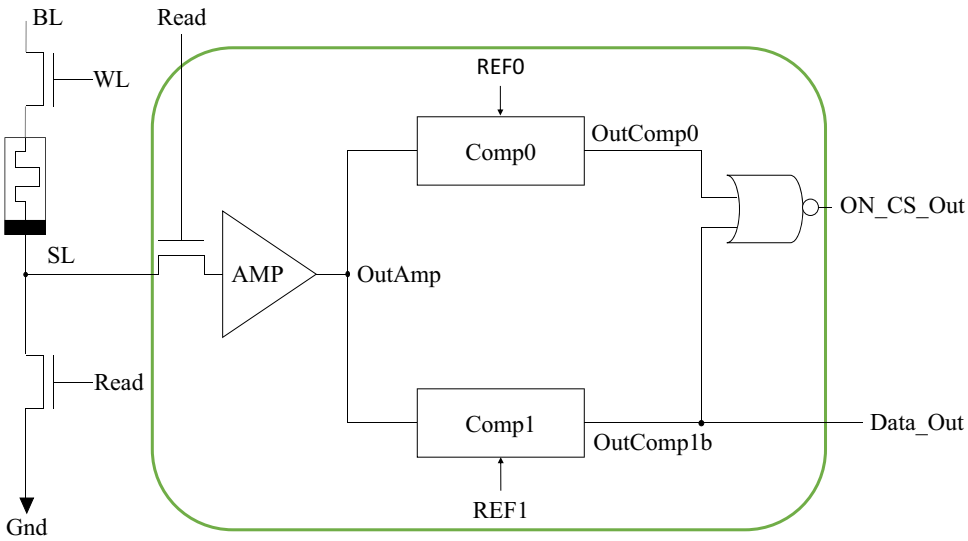


Fig. 3 Block diagram of the ON-CS including the read circuitry

'0' if the opposite situation occurs. For the detection of a UWF, the measured voltage has to assume a value between the two reference voltages (REF0 and REF1). In that case, OutComp0 and OutComp1b will both generate a '0'. The output of the NOR logic gate will assume a '1', indicating the detection of a UWF. Note that OutComp1b is also used as Data_Out.

The implementation of the AMP is based on these references [17, 24, 31]. Figure 4(a) shows the electrical schematic view of the implemented AMP. In general terms, AMP has three transistors on the left side that force the Ref_Amp node to a small voltage that is used as an internal reference for one side of the differential amplifier. The Input signal of the AMP arrives from SL through the access transistor. The higher the voltage difference between the Input and the Ref_Amp, the bigger the voltage connected to the gate of the nMOS that is connected to the output. The voltage in the gate will open the transistor and pull the output node to Gnd. The output voltage becomes close to Gnd with higher differences between the input voltage and the reference voltage (Ref_Amp). To resume, the input signal is inverted and amplified.

Finally, Comp0 and Comp1 are implemented based on a double-tail dynamic comparator [22]. Figure 4(b) depicts the comparators' electrical schematic view. During the pre-charge phase, when the Read signal is low, the pMOS transistors of the input stage are opened and will pre-charge the node connected to the inverters' gates between the input and the output stage. When the Read signal is '1' the capacitance of the node is discharged to the ground through the input transistors. Depending on the input voltage, one of the nodes will be forced to (V_{dd}-V_{th}) faster, which will turn off the inverter's nMOS. If the voltage in the Input is bigger than REF, Out will be pulled to V_{dd}, and Outb is forced to Gnd. If the input voltage is smaller than REF the outputs will have the opposite behavior. Once this output decision is made, the outputs will keep their respective output values until Read becomes '0' again. At this point, the comparator is back to the pre-charge phase. Since the comparator works dynamically, the input voltage must be in full swing at the moment the Read signal activates the decision phase of the comparator.

3.2 The Optimized DfT Strategy

Despite the effectiveness of the strategy presented in [10] to properly detect traditional and unique faults that may affect ReRAM cells due to manufacturing deviations, the adoption of the ON_CS introduces a significant area and power overhead. In addition, it was observed that the ON_CS suffers from a not neglectable process variation impact, reducing its detection resolution. In this context, this paper proposes an optimized version of the DfT strategy presented in [9]. The strategy is based on introducing a DfT circuitry that adopts the Sense Amplifiers (SAs) already present in the ReRAM block to provide fault detection. In more detail, by adopting the SAs used to read the memory block, the introduced overheads are reduced and the module most affected by process variation is eliminated, the AMP (see Fig. 3). Note that the adopted read circuit was developed based on [7].

It is important to mention that the main difference between the DfT strategy presented in this paper and the one described in [9] is related to the fact that the boundaries defining the unique faults were redefined in order to better represent the expected faulty behavior of ReRAM cells. In other words, a more realistic representation of the resistance interval associated to the undefined state was defined, see Fig. 2. Moreover, it is important to note that the four reference voltage blocks were properly implemented as part of the DfT circuitry, as opposing what was made in [9], leading to more realistic results, as can be verified in Section 5.

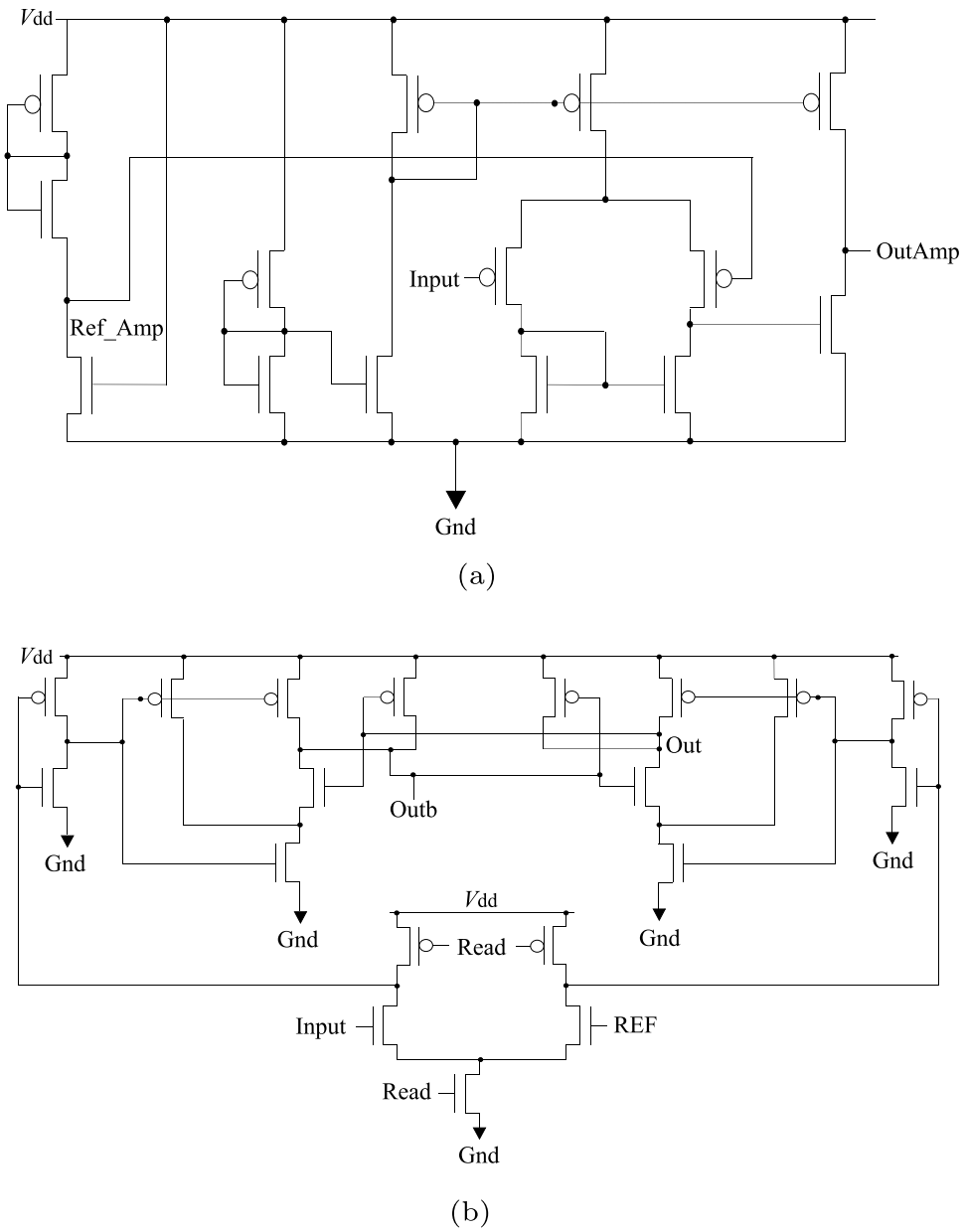


Fig. 4 Internal ON-CS designs: **a** Schematic view of the designed Amplifier (AMP); **b** Schematic view of the designed Comparator (*Comp0* and *Comp1*)

Figure 5(a) shows the read circuit adopted for reading ReRAM cells. In general terms, the circuit provides the result for each bit column and is a Latch SA that reads the voltage of the cell (V_{cell}) at the inverting input (-) during the read operation, comparing the read value with a reference voltage (V_{ref}), on the non-inverting output (+) to generate the column output data (Data_Out). During the read operation, the Read signal and WL are at the high logical level and BL is charged by the V_{cell}, creating a path through the memristive device by the SL, which is connected to the ground, forming the current over the cell (I_{cell}). A reference resistor (R_{ref}) is used to generate the reference voltage and the current over this resistor (I_{ref}). Note that if the ReRAM cell's voltage is higher than the reference, the Data_Out is logic '1'.

Figure 5(b) depicts the block diagram of the proposed DfT circuitry. The circuitry is composed of four extra read circuits that are activated for testing the ReRAM after manufacturing. Each extra SA compares the ReRAM cell voltage with a reference voltage, defined to properly detect one specific resistance interval that can be assumed by the ReRAM cell: the two boundaries of the Undefined State, the low boundary (V_{refLBU}) and high boundary (V_{refHBU}), Deep Low (V_{refDL}), and Deep High (V_{refDH}). Basically, two read circuits are used to determine the Undefined State, the comparison with the two boundaries will generate the

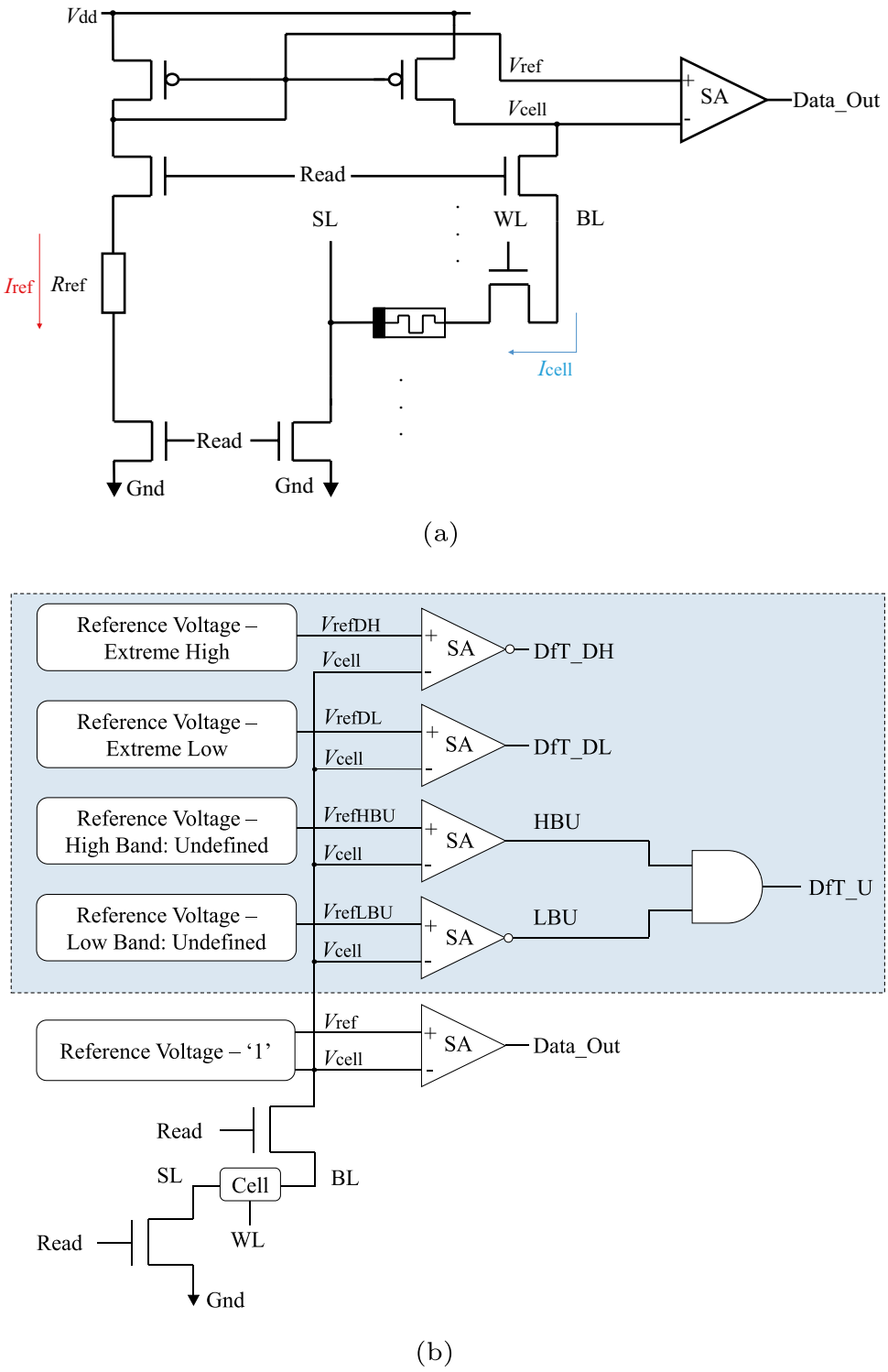


Fig. 5 **a** Read Circuit and **b** Optimized DfT circuitry

two signals LBU (inverted output) and HBU, which are connected with an AND gate, given the output detection of the undefined state. The outputs of DfT circuitry are DfT_U, DfT_DL, and DfT_DH. It is important to mention that for the DfT_DH, the SA's output is inverted. Further, the SA was implemented based on a traditional two-stage sense amplifier with D latches [29].

Resuming, the proposed DfT circuitry was specified to properly detect all unique faults that can affect ReRAM cells as well as traditional faults, such as Stuck-At Faults (SAFs).

In more detail, the fault detection capability of the proposed methodology is based on comparing the voltage value of the ReRAM cell to four distinct reference voltages. A high voltage in the cell is observed when a high current flows through the memristive device, indicating that the device is in LRS, or storing the value '1' (V_{READ_1}). Similarly, a low voltage in the ReRAM cell is measured when a low current flows through the novel device, indicating that the ReRAM cell is in HRS or storing the value '0' (V_{READ_0}). Thus, the DfT circuitry compares the voltages associated with LRS and HRS to the reference voltages. Note that V_{refDH} assumes a value higher than V_{ref}, V_{refHBU} assumes a value slightly higher than V_{ref}, V_{refLBU} assumes a value slightly lower than V_{ref}, and V_{refDL} assumes value lower than V_{ref} and V_{refU}. Exemplifying: $V_{refDH} > V_{refHBU} > V_{ref} > V_{refLBU} > V_{refDL}$. Finally, the AND gate is used to determine the DfT_U, given that case, the memristive device is in the undefined state, then the output LBU and the HBU will be logic high. Below the undefined region, LBU is logic low level, and the same happens for HBU over the undefined region. It is important to mention that the voltage references of the DfT circuitry are defined based on the resistive state values adopted to represent the HRS and LRS. Note that is expected that the proposed DfT circuitry could adapt the bias voltage as observed in [7], addressing possible variations.

4 Experimental Setup

In order to validate the optimized DfT strategy and demonstrate its fault detection capability, a case study composed of a 3x3 word-based ReRAM, where each word is composed of 3 ReRAM cells, including peripheral circuitry, was adopted. The case study and the DfT Circuitry were implemented using a 130 nm Predictive Technology Model (PTM) for the CMOS-based circuits and the ReRAM ($Pt/HfO_2/TiO_x/Pt$) compact model proposed in [2, 11]. Figure 6 shows the block diagram of the adopted case study including the DfT circuitry. Regarding the adopted implementation granularity, all words (Word00, Word10, and Word20, for example) present in the same column share the same DfT circuitry. In addition, all words (Word00, Word01, and Word02, for example) on one row share the Word Line (WL) and the Select Line (SL), while all words in one column share the Bit Line (BL). As previously mentioned every word consists of three 1T1R ReRAM cells, storing one bit of data, see Fig. 5(a). Each BL and SL is connected to a capacitance of 150 fF, emulating a larger ReRAM for more realistic simulation results. The peripheral circuitry implements the Read-and-Write Logic. The Column-Address-Decoder selects the desired column, Column Select (CS). Similarly, the WL-Decoder selects the WL that corresponds to the desired row address, once the WL enable (WL_EN) signal is set. BL and SL Drivers act to allow write and read operations on the block, varying its voltage accordingly with the target operation. Note that when a write operation (write '0' or write '1') is performed, a RESET operation is performed first on the selected word. This RESET operation is performed by driving the SL to V_{reset} and the corresponding BL to Gnd. When the data to be written is a '1', a SET operation is performed subsequently on that cell only. This is done by setting the BL to V_{SET} and the SL to Gnd. This writing scheme ensures that the cells are not over-SET, which may lead to low reliability [1]. For the read operation, it uses the Sense Amplifiers connected to the BLs, given a Data_Out for each bit line. Also, the DfT Circuitry is implemented in this point, generating the output signals DfT_Circuitry_Outs (DfT_DH, DfT_DL, and DfT_U) for each column, please check the explanation provided in Section 3.2. Finally, the adopted voltage for performing a write '1' operation, or in other words a SET

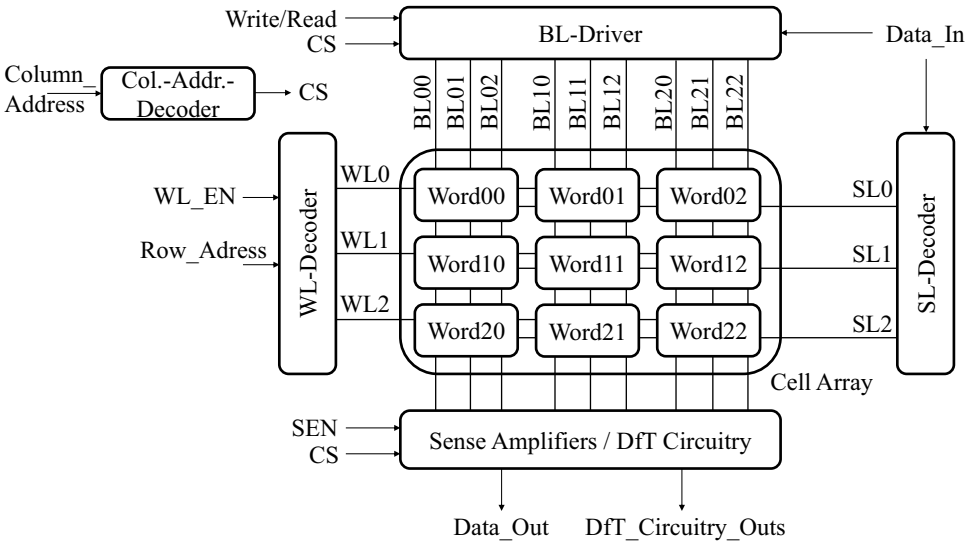


Fig. 6 Case Study: ReRAM Block

operation, is equal to 1.6 V, which is the nominal voltage adopted in the entire circuit. The RESET operation (write '0') is performed by applying a voltage of −1.7 V. Usually, a higher RESET voltage is adopted in order to minimize the required operation time. The room temperature used in this experiment was 27 °C.

It is important to point out that in this work, the faulty behavior of ReRAM cells was introduced by adopting the DO model based on the approach described in [13, 15, 16]. This model incorporates the impact of physical defects on the device's technology parameters and thereafter on its electrical parameters. In more detail, the defects were modeled by changing the values related to the oxygen vacancy concentration in the disk of the memristive device (N_{real}) according to [11]. By increasing the lowest possible concentration of oxygen vacancies ($N_{disc,min}$) the maximum resistance in the HRS is lowered because the current that can flow through the device is higher with a higher $N_{disc,min}$. The same principle is used but in an opposite way, when the highest possible concentration of oxygen vacancies in the disk ($N_{disc,max}$) is decreased, then the minimum resistance in LRS is increased. The current flowing through the device will decrease leading to higher resistance in LRS. This method makes the simulation of a device in an undefined state possible while keeping its memristive device-like behavior. Note that N_{real}, $N_{disc,min}$ and $N_{disc,max}$ are parameter names used in the JART model v1b [11], being measured in m^{-3} [2, 11].

5 Obtained Results and Discussion Regarding the Optimized DfT Strategy

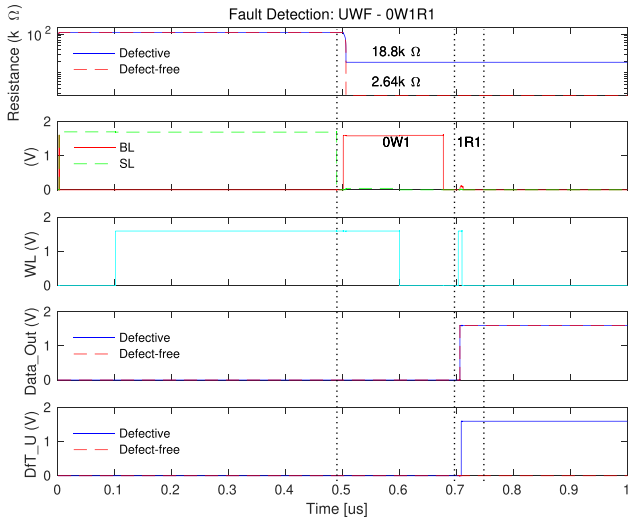
The detection capability of the proposed DfT strategy was evaluated through electrical simulations using Spectre (Cadence). The defects were injected using the DO model, where $N_{disc,min}$ and $N_{disc,max}$ values were modified to change the ReRAM cell resistive state in order to indicate all possible unique faults: the extreme HRS (DeepF High), the undefined state (UWF), and the extreme LRS (DeepF Low). For this work, the LRS is defined to be represented by a resistance in the range of 1.75 kΩ, and 10 kΩ. The HRS is defined to assume a value between 53.2 kΩ, and 110 kΩ. Thus, the undefined state is represented by resistance values between 10 kΩ and 53 kΩ. The extreme HRS is set to assume values above 111 kΩ, and, finally, the extreme LRS assumes values below 1.74 kΩ. These limits are represented by the N_{real} parameter that is limited by $N_{disc,min}$ and $N_{disc,max}$ parameters [11]. Table 1 summarizes the values of N_{real} parameter adopted to represent extreme HRS, HRS, undefined ('U') state, LRS, and extreme LRS in the ReRAM cell. Table 1 also includes the range of resistance value equivalent to each N_{real} value adopted for indicating all five possible states. When it is intended to simulate a unique fault, the $N_{disc,max}$ and $N_{disc,min}$ parameters are modified to the Upper and Lower Limit according to Table 1. Observing Table 1 it is possible to see that the variation of N_{real} is not linear when compared with the resistance value. Note that a variation of 0.007×10^{26} m^{-3}, starting from 0.008×10^{26} m^{-3}, is enough to cause a resistance variation from 110 kΩ to 53.2 kΩ. To resume, a small variation in the $N_{disc,min}$ value makes the device not able to switch to HRS. A complete study about the impact of electrical parameters variation on the memristive device behavior can be found in [3].

Table 1 Boundaries of States determined by N_{real}

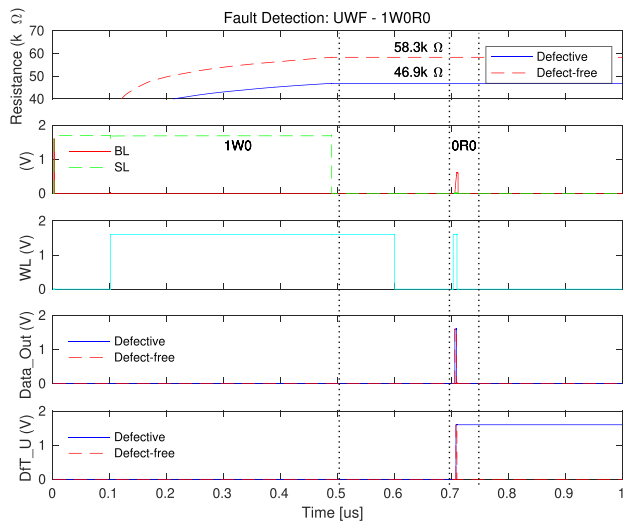
States	Parameters	Upper Limit	Lower Limit
Extreme HRS	$N_{real}(\times10^{26}\ m^{-3})$	0.0001	0.0079
	Resistance (kΩ)	108306	112
HRS	$N_{real}(\times10^{26}\ m^{-3})$	0.008	0.014
	Resistance (kΩ)	111	53.2
'U' State	$N_{real}(\times10^{26}\ m^{-3})$	0.015	0.065
	Resistance (kΩ)	53.1	10.1
LRS	$N_{real}(\times10^{26}\ m^{-3})$	0.066	3.22
	Resistance (kΩ)	10.0	1.75
Extreme LRS	$N_{real}(\times10^{26}\ m^{-3})$	3.23	20.00

The next four figures demonstrate the detection capability of the proposed approach with respect to the detection of UWF, URF, and DeepFs. In more detail, the figures show the comparison between defective and defect-free ReRAM cells while performing a pre-defined operating sequence. The ReRAM cell's resistance, the BL and SL's voltage over the cell, the WL's voltage as well as Data_Out and the DfT Outputs are presented. Figure 7(a) shows the detection of a UWF while performing the following operating sequence 0w1r1. In addition, the graph also demonstrates the operating behavior of the adopted 3x3 word-based ReRAM, where first a RESET operation is performed, by an active SL signal, then BL is activated making the SET operation (it should be inactive for write '0'), and the WL is active during the whole write operation, then it is briefly active during the READ. Also, the graph shows that the defective ReRAM cell assumes a resistance value of 18.8 kΩ, while the defect-free cell is at 2.64 kΩ. Note that the resistance value's axis is represented using a logarithm scale to provide a better visualization). The Data_Out signal from both cases is a logical '1', however, the DfT_U signal detects the 'U' state of the defective cell. Figure 7(b) depicts the detection of a UWF while performing a READ '0' operation, where the defective ReRAM cell has a resistance value of 46.9 kΩ after the write '0' operation. If considering only the read operation for the test analysis, it can be said that the circuit is detecting a URF.

In Fig. 8, the detection of DeepFs is depicted. Figure 8(a) shows the detection of a Deep Low Fault (DfT_DL). Note

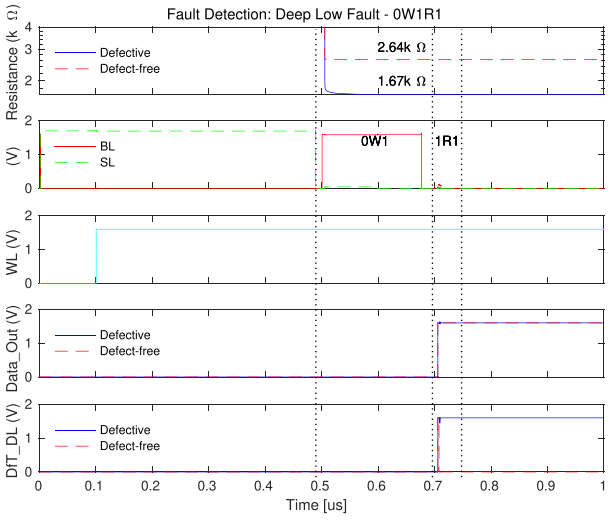


(a)

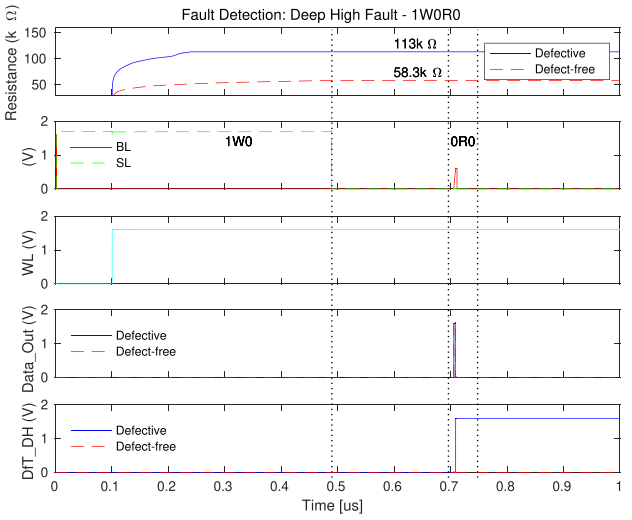


(b)

Fig. 7 UWF detection during **a** READ '1' and **b** READ '0'



(a)



(b)

Fig. 8 **a** Deep Low Fault detection and **b** READ Deep High Fault detection

that the defective ReRAM cell assumes the resistance value of 1.67 kΩ after the SET operation. In addition, the High Deep Fault detection depicted in Fig. 8(b), DfT_DH signal, shows the fault detection when the ReRAM cell assumes a value of 113 kΩ. The Data_Out for both cases indicates a correct logic value, demonstrating the parametric nature of DeepFs. Note that this specific type of fault changes the resistive state of the memristive device to levels above the nominal ones. This situation makes the device more resilient to transition resistance during the write operation, for example.

After evaluating the fault detection capability of the optimized DfT strategy, a further evaluation considering the impact of process variation on the resolution of the DfT circuitry was performed. For this purpose, Monte Carlo (MC) simulations were performed in the DfT circuitry. In more detail, channel length and width as well as oxide thickness were varied adopting a 3σ Gaussian distribution with a variation of 4% inter-die. Table 2 presents the percentage of incorrect detection, considering all unique faulty behaviors. A total of 1000 simulations for each unique fault were performed. The obtained results show that the DfT circuitry had only 4.0% of False Positive Detection when considering Deep High faults, and 3.8% of False Positive Detection for Deep Low faults. Note that no False Positive Detection was observed for UWFs. In addition, when considering defective ReRAM cells, the DfT circuitry was not able to properly

Table 2 Monte Carlo results

Incorrect Detection Case	Operation	Percentage
False Positive Detection Deep High Fault	1w0r0	4.0%
False Positive Detection Deep Low Fault	0w1r1	3.8%
Non-Detection Deep High Fault	1w0r0	4.3%
Non-Detection Deep Low Fault	0w1r1	0.3%
Non-Detection UWF	1w0r0	3.1%
Non-Detection UWF	0w1r1	1.1%

detect Deep High faults in 4.3% of the 1000 simulations, Deep Low faults in 0.3% as well as UWFs in 3.1%, when executing 1w0r0 (read '0'), and in 1.1% when performing 0w1r1 (read '1'). A further analysis of the possible false positive's causes was conducted and the conclusion was that the circuits that implement the reference voltages are considerably affected by process variation. An alternative implementation for the reference voltage's circuits is being currently investigated. One possible solution based on the use of a read circuit that can adjust the used reference voltage can be found in [7]. It is important to comment, that in the work published in [10], the evaluation of the process variation impact was performed assuming the reference voltages as constant sources.

Regarding the introduced overheads, the power consumption overhead in this case study is around 9% when the proposed DfT circuitry is added, considering that the implementation granularity is one DfT circuitry per BL. Table 3 presents the average power consumption related to the optimized DfT strategy compared with the write operations of one ReRAM cell. The DfT strategy power consumption is estimated at around 8.3 µW during the read operation, which is not so relevant when compared to the average power consumption of a ReRAM cell, of 79.2 µW during the write '0', and 610.8 µW during the write '1' operation. It is interesting to notice, that the power consumption is higher during the SET stage due to the increase in conductivity of the ReRAM cell. Note that by shortening the SET operation time this power consumption can be reduced.

Considering the area overhead, when compared with the previously published work [10], the optimized DfT strategy has a reduction of 25% in the number of transistors, since the transistors required for the implementation

Table 3 Power consumption estimation

Operation	Estimated Power
ReRAM cell - write '0'	79.2 µW
ReRAM cell - write '1'	610.8 µW
DfT circuitry	8.3 µW

Table 4 Detection capability of the proposed DfT strategy according to all unique faults

EtD	UWF	URF	DeepF	IUSF
✓	✓	✓	✓	X

of the previous AMP are not required anymore. Finally, the implementation granularity of the DfT strategy plays an important role related to overheads and consequently, different schemes can even further minimize the overheads. Another important aspect is that the proposed DfT strategy could be optimized in order to also be used during a lifetime to provide detection of in-field faults, increasing the reliability of ReRAMs.

In relation to the technology detection capability, Table 4 gives an overview of it. The methodology was developed to detect the unique states of memristor, which are HtD but can also detect easy-to-detect (EtD) faults as transition and stuck-at faults. For ReRAM architectures that use pulses of write and read for verification, the DfT can be active during the verification to detect the UWFs. The URFs and DeepFs can be detected during a normal read operation. For intermittent faults, it cannot be determined with only one operation.

6 Conclusion

This paper proposes an optimization of the DfT Strategy presented in [10] for performing high-volume manufacturing testing of ReRAMs. The proposed strategy is based on the introduction of a DfT circuitry able to provide the detection of unique faults in ReRAM cells. In more detail, the DfT circuitry measures the current that flows through the 1T1R ReRAM cells and compares the read value with four reference values. The strategy was validated using a case study composed of a 3x3 word array, where each word includes 3 1T1R ReRAM cells, including peripheral circuitry. The obtained results demonstrated that the DfT circuitry is able to provide the detection of unique faults associated to possible defects that can be introduced during manufacturing. Simulations also demonstrated that the optimized DfT strategy can better tolerate the impact of process variation when compared to the strategy presented in [10]. In addition, the proposed optimization was able to reduce the introduced area overhead by 25% and increase the power consumption by 9%. Note that the introduction of a variable reference voltage could also be an interesting solution for reducing the strategy's area overhead. As a future work, we intend to explore the DfT circuitry to also perform in-field on-line testing to improve ReRAM's reliability during its lifetime.

Funding Open Access funding enabled and organized by Projekt DEAL. This work was supported by the Federal Ministry of Education and Research (BMBF, Germany) within the NEUROTEC project (project numbers 16ES1134 and 16ES1133K). In addition, this work was funded by the Ministry of Culture and Science of the German State of North Rhine-Westphalia (MKW) under the Excellence Strategy of the Federal Government and the Länder.

Data Availability The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflicts of Interest The authors declare they have no financial interests.

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