Editorial

Vishwani D. Agrawal[1]

The topics discussed in the seven articles of this issue are memory testing, test education, scan testability, software test, analog and RF test, and hardware security.

The issue begins with a paper on radiation hardened by design (RHBD) memory cell. This dual interlocked storage cell (DICE) uses redundancy, transistor sizing and adjustment of doping parameters for low vulnerability to single event transients (SET) as the CMOS device features shrink. The paper describes the research of Pannu, a PhD scholar, and her professors Rup Prakash and Jasbir Kaur from the Panjab Engineering College, Chandigarh, India.

The second paper discusses the development of a test programming system for educating engineering students. The microcontroller-based system is described by Ndongmo from the University of Bamenda, Bemenda, Cameroon, and his five other scholar and teacher associates, Kevin, Ajesam, Adélaîde, René and Godpromesse from various universities in Cameroon.

The third paper discusses the testing of a reconfigurable scan network (RSN) used in an electronic system for tasks such as verification, debugging, and performance monitoring. The paper outlines the difficulties with thorough testing of an RSN and presents what they call "a complete DfT scheme." The authors are Lylina, Wang and Wunderlich from University of Stuttgart, Stuttgart, Germany.

The fourth paper optimizes software testing. It minimizes path activation tests to cover all nodes and edges in the control flow graph of the program. Interestingly, this work finds the paths using a nature-inspired smell detection agent (SDA) algorithm, which follows the behavior of a dog in finding a path to the source of smell. The complexity of the optimization process is shown to be significantly lower than that of other methods. Contributors are Chandra from University of Kerala, Thiruvananthapuram, Kerala, India, Sankar from Government polytechnic college, Punalur, India, and Anand from Muthoot Institute of Technology and Science, Kochi, India.

The fifth paper addresses the issue of multisite testing of analog and mixed-signal devices. In particular, the usual site-to-site variations make it difficult to set proper pass-fail thresholds on signals. The paper proposes a novel mathematical technique to supply corrections for such variations. Authors are Farayola, Bruce, and Chen from Iowa State University, Ames, IA, USA, and Chaganti, Sheikh and Ravi from Texas Instruments.

The last two papers deal with hardware security. Sixth paper is authored by Naveenkumar, Sivamangai, Napolean, and Sathya Priya from Karunya Institute of Technology and Sciences, Coimbatore, India. They discuss the implementation of a physical unclonable function (PUF) using field programmable gate array (FPGA) hardware.

Contributors of the seventh paper are R. Sharma, G. K. Sharma, and Pattanaik from ABV-Indian Institute of Information Technology and Management, Gwalior, India. They apply machine intelligence to detect Trojan hardware. A structural testability measure SCOAP (Sandia controllability observability analysis program) supplies the circuit features for use in the training of machine learning.

We end the year 2022 by closing the Volume 38 of *JETTA*. The six issues of this volume contain forty-three papers. Interesting observations can be made from the statistics of submissions. The annual manuscript submissions to JETTA during the past four years were 237 in 2019, 211 in 2020, 151 in 2021, and 223 in 2022. This expected slowdown caused by the world-wide pandemic shows a bottoming out of submissions in 2021 and recovery beyond. At the end of 2022, the journal has fifty-two members on its editorial board, as listed inside the front cover.

✉ Vishwani D. Agrawal
    agrawvd@auburn.edu

1   Auburn University, 36849 Auburn, Alabama, USA