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Editorial

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This issue contains ten articles, including three letters. The topics discussed are cell-aware testing, 3D-stacked device testing, test data compression, RF circuit testing, soft errors, and hardware security.

Three papers are derived from the *IEEE Latin-American Test Symposium* (LATS). The first paper received a Best Paper Award at the 20th LATS, Santiago, Chile, March 11–13, 2019. The fifth and eighth papers are expanded versions of those appearing at the 21st LATS, held during March 30 – April 2, 2020 in Jatiúca (Maceió), Brazil. *JETTA* Editor Leticia M. B. Poehls supervised the peer reviewing of the journal versions.

The first paper addresses cell-aware test. The authors characterize cells (building blocks) of a design library for testability of internal layout dependent defects. From analog simulation of large number of defects, they find a small representative set whose tests can detect most of the internal defects. Authors are Gao, Hu, Malagi, Swenton, Huisken, Goossens and Marinissen, representing IMEC, Belgium, Cadence Design Systems, Endicott, New York, USA, TU Eindhoven, The Netherlands, and National Tsing-Hua University, Hsinchu, Taiwan.

The second paper presents a method for testing resistive-open defect and short-to-ground defect in a through silicon via (TSV) of a 3D-stacked device. Variations in delay, width, and shape of clock pulses after they emerge from a TSV indicate the presence or absence of defects. Contributing researchers are Gerakis and Hatzopoulos from Aristotle University of Thessaloniki, Greece, and Tsiatouhas from University of Ioannina, Greece.

In the third paper we revisit the problem of data transmission between automatic test equipment (ATE) and device under test (DUT). Enormous amount of data is moved through a limited bandwidth channel between the ATE and DUT in real time and at high test clock rate. Tseng, from Yuan Ze University, Chung-li, Taiwan, reviews several methods used for test data compression in commercial CAD tools in which test data is broadcast to feed a group of scan chains. The focus, however, is on a new method called cascaded multicasting scan (CMS), where scan chains are grouped to minimize the number of broadcasts based on the chain compatibility with the given test data.

The fourth and fifth papers are on radio frequency (RF) circuit test. Authors, Sun, Li, Du and Liang from Xidian University, Xi'an, Shaanxi, China, and Nian from the 41st Research Institute of China, Electronics Science and Technology Group, Qingdao, China, study failures in RF low noise amplifier (LNA). They use machine learning techniques, support vector machine (SVM) and hidden Markov model (HMM), to analyze the operational data for identifying faults or predicting failures.

The fifth paper proposes a two-tier test cost reduction strategy for RF circuits. First, a low-cost indirect test, sometimes referred to as alternate test, is applied. A pre-trained machine intelligence system then evaluates the confidence in the test outcome. For low confidence, typically found in 25-percent cases, an elaborate specification test is applied. Authors are El Badawi, Azais, Bernard, Comte and Kerzerho from LIRMM, University of Montpellier, Montpellier Cedex, France, and Lefevre from NXP Semiconductors, Caen, France.

Sixth and seventh papers and the first two *JETTA Letters* address soft errors. The sixth paper provides a parity method to correct multiple bit flips in an N-by-N data block. The parity is derived from a chessboard on which N queens are strategically placed. Intriguing? Read on. The paper is authored by Sadi, Sumaiya, Dewan and Rahman from Khulna University of Engineering and Technology, Khulna, Bangladesh.

The seventh paper compares various types of SRAM cells using alpha particle and proton irradiation and concludes that the dual interlocked storage cell (DICE) provides the best soft error tolerance. Researchers contributing this work are Wang and Wu from the National Key Laboratory of Analog Integrated Circuits, China, Tian, Shi and Chen from University

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of Saskatchewan, Saskatoon, SK, Canada, and Li from Dalhousie University, Halifax, NS, Canada.

The last three articles are *JETTA Letters.* First two continue with the theme of soft errors and the third is related to research on hardware security.

The eighth article is contributed by Marques and Butzen from Universidade Federal do Rio Grande do Sul – UFRGS, Brazil, and Meinhardt from Universidade Federal de Santa Catarina – UFSC, Brazil. They examine soft error sensitivity of several types of SRAM cells including DICE for read, write, hold and half-selection operations.

The ninth article reports an experimental study of single event upsets (SEU) in an SRAM with triple modular redundancy (TMR), conducted by Shi, Tian and L. Chen from University of Saskatchewan, Saskatoon, SK, Canada, R. Chen from National Space Science Center, CAS, Beijing, China, Liu and Li from Microchip Technology, Saskatoon, SK, Canada, M. Chen from Space Star Technology Co. Ltd., Beijing, China, and Shen from Cogenda Electronics Co. Ltd., Suzhou, China. They designed a 32 kb SRAM with TMR embedded on ARM M0 processor test chip and fabricated it in 28 nm FDSOI technology. Then, a heavy ion irradiation experiment was carried out at the China Institute of Atomic Energy (CIAE).

The tenth article provides a method for concealing hardware Trojan (HT) with the objective of creating example circuits for research on HT detection. This involves resynthesizing a Trojan-modified truth-table into a circuit closely matching the original Trojan-free circuit in size and power consumption. Authors are Liu, T. Wang, and X. Wang from Army Engineering University, Shijiazhuang, China.